Characterization of the triple-gate flash memory endurance degradation mechanism

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Abstract: Write/erase degradation after endurance cycling due to electron trapping events in triple-gate flash memory have been detected and analyzed using a UV erasure method. Different from the commonly degradation phenomenon, write-induced electron trapping in the floating gate oxide, electron trapping in tunneling oxide is observed in triple-gate flash memory. Further, the degradation due to single-electron locally trapping/de-trapping in horn-shaped SuperFlash® does not occur in the triple-gate flash cell. This is because of planar poly-to-poly erasing in the triple-gate flash cell instead of tip erasing in the horn-shaped SuperFlash® cell. Moreover, by TCAD simulation, the trap location is identified and the magnitude of its density is quantified roughly.

Key words: Fowler-Nordheim tunneling; endurance; traps; UV erasure

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1. Introduction

Electron trapping in charge-transfer dielectrics is known to be a limiting factor of write/erase (W/E) cycling endurance of non-volatile floating-gate memories. In SSI flash memory, which uses enhanced channel hot-electron injection (CHEI) for programming and Fowler-Nordheim tunneling for erasing[1,2], electrons will be trapped in the tunnel oxide (TUNOX) or at the injection point of floating gate oxide (FGOX), resulting in gradual degradation of erase characteristics and leading to the closure of the memory cell threshold window. So, it is necessary to make sure that the trap location is accurately identified for the development of optimized program/erase schemes and memory cell design.

It is generally believed that charge trapping at the injection point of the device during programming is considered to dominate the weak erase failure. Houdt *et al.* put forward that charges trapping at the injection point dominate the endurance degradation of high injection MOS (HIMOS) flash memory which normally uses Fowler-Norheming (FN) tunneling at the source side for erase[4]. Hu and Wu *et al*. demonstrated similar results in the horn-shaped flash memory[5−9]. In contrast to the research above, Tkachev and Liu proved, when the poly-to-poly erasure was applied, that charges trapping in the tunnel oxide (TUNOX) exert much greater effect on the degradation in the horn-shaped dual-gate SuperFlash® cell[3,13]. With the cell size scaling down and the geometry complex, the endurance degradation monitoring directly is a great challenge in the triple-gate flash cell. So far, there lacks detailed analysis and characterization of oxide degradation in the triple-gate flash cell. In this paper, we will focus on clarifying the trap location being identified and analyze its effects on device characteristics using UV erasure. Further, TCAD simulation is applied to verify the results and approximately quantify the number of traps.

2. Device fabrication and experimental setup

Write/erase degradation after endurance cycling in SSI flash EEPROM devices is studied using the triple-gate flash transistor as a typical example (Fig.1). During erasing, instead of exploiting tunneling through FGOX at the

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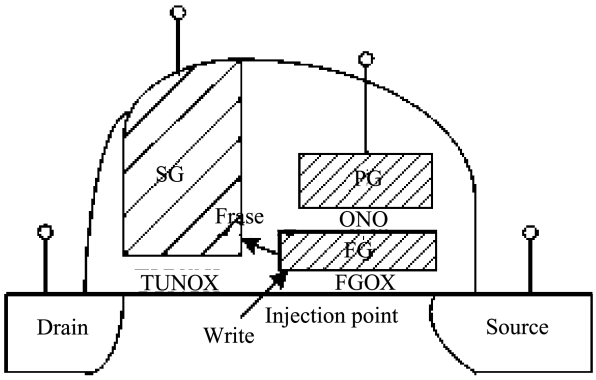

Figure 1: Schematic diagram of the triple-gate flash.

source side, as commonly adopted in HIMOS, the triple-gate flash utilizes FN tunneling of the electron from FG to SG. Programming is performed by enhanced CHEI at the injection point of the device. The detailed description of the operation and the underlying device physics is given in Refs.[10–12].

The cell was fabricated in a standard 0.12 μm self-aligned flash process. The oxide under the floating gate was thermal grown of 9 nm thick and the inter-poly dielectric layer under SG was about 12 nm grown by high temperature oxidation (HTO), with a N_2O anneal process post its formation. In this study, the threshold voltage (V_t) is always defined as the program gate voltage (V_{PG}) that corresponds to a fixed drain (BL) current (I_d.) of 1 μA at the BL bias of 0.1 V with a select gate (SG) voltage (V_{SG}) 2.5*V*.

In order to identify the mechanism of write/erase degradation, a technique of ultraviolet (UV)light is applied at various stages throughout the endurance measurement. A UV erase operation is self-limiting and the device always ends up in the same equilibrium state with the same reference charge on the FG. Thus, any change in cell characteristics after UV
erase will reveal only the damage in the oxide during W/E cycling, and will not be affected by changes in the amount of the stored FG charge.

The electric parameters were measured on HP4156. The measurement of V_t. kinetics during cycling included: regular programming and erase, and measurement of cell threshold voltage in program or erase status.

3. Results and discussion

3.1. Endurance characteristic

Figure 2 shows the endurance characteristic of the triple-gate flash memory cell. As can be seen, the erased threshold (V_{te}) shows a large increase (~2.5 V) with the number of W/E cycles, implying a large decrease of the read-out current, whereas the written threshold (V_{tp}) is lightly affected by repeated W/E operations. Since the cell is written by enhanced channel hot electron injection from channel to FG at the injection point through a thin oxide, the initial conclusion would ascribe this degradation behavior to electron trapping in FGOX[8−12]. However, in the following sections it will be shown that this conclusion is not reliable in triple-gate flash devices.

3.2. *I–V* characteristics

By comparing the *I–V* characteristics in a particular threshold state with the characteristics after UV erasure during W/E cycling, the change in the amount of FG charge can be monitored. Indeed, since the device is always back to a state with the same reference charge on the FG after UV erasure, V_t can be expressed as

$$V_t = V_{tuv} + \Delta V_{tq},$$

where V_{tuv} is the threshold voltage after UV erasure. The charge on the FG is always the same after UV erasure. ΔV_{tq} is the V_t shift induced by the additional charge on the FG with respect to the UV erased state. A change in ΔV_{tq} in

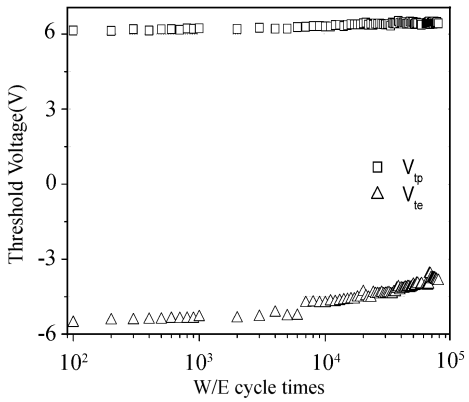

Figure 2: Endurance characteristic in triple-gate flash, showing a slightly shift in the written threshold (V_{tp}) but a deeper shift in the erased threshold (V_{te})

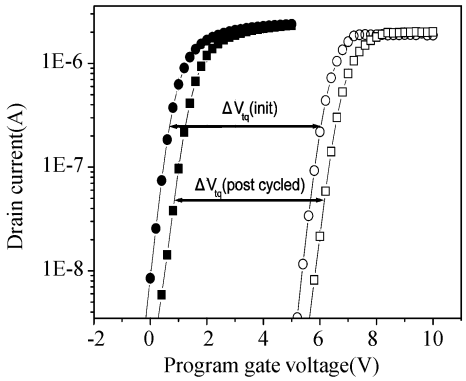

Figure 3: Drain current versus program gate voltage characteristics in the written state, showing nearly no charge amount change on the FG with W/E cycling. ΔV_{tq} is a measure of the charge on the FG. (Full dots: fresh device after UV erasure; Open dots: fresh device in written state; Full squares: 60000 cycles and UV erasure; Open squares: 60000 cycles and written state).

the written or the erased state is thus indicative of a change in the amount of charge transferred to or from the FG. Therefore, by evaluating the ΔV_{tq} during a degradation measurement, the V_t shift due to the charge amount change on the FG can be monitored as a function of the number of W/E cycles.

Figure 3 shows the I_d-V_{pg} curve of a written device combined with UV erasure, measured under read out conditions (V_{BL}=0.1 V, V_{SG}=2.5 V), before and after 60000 W/E cycles. As can be seen, $\triangle V_{tq}$ in the written state has no degradation even after 60000 W/E cycles. This implies that, after writing, the net charge amount on the FG remains at almost the same level in the states before and after W/E cycles. Moreover, after P/E cycling, no severe degradation of the sub-threshold slope is observed, impling that few negative trapping electrons exist at the injection point. The severe sub-threshold slope degradation can be caused by an interface trap density (D_{it}) or by highly localized negative oxide trapped charge in coupling oxide[8].

However, an obvious different phenomenon is observed in the erased state compared to that in the written state. As can be seen from Fig.4, ΔV_{tq} has decreased considerably after 60000 W/E cycles (~1 V), which means the degradation of the erase characteristic. If the weak erase issue is due to electrons trapped at the injection point in coupling oxide, then ΔV_{tq} in the written state should be decreased due to the suppression of channel hot electron injection efficiency. But this is inconsistent with the result shown in Fig.3. On the contrary, electrons
trapped in the tunneling oxide could explain it. After W/E cycling, electrons trapped in the tunneling oxide will block the tunneling of the electron on the FG, as well as decrease the field between SG and FG. Therefore, due to the decrease of the electrons amount transferred from FG, less positive FG voltage is achieved and it will lead to the lower

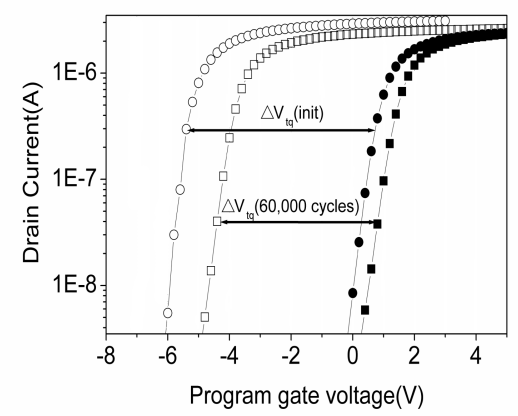

Figure 4: Drain current versus program gate voltage characteristics in the erased state, showing a changing amount of charge out of the FG with W/E cycling. $\Delta V_{\rm tq}$ is a measure of the charge out of the floating gate. (Full dots: fresh device after UV erasure; Open dots: fresh device in the erased state; Full squares: 60000 cycles and UV erasure; Open squares: 60000 cycles and erased state)

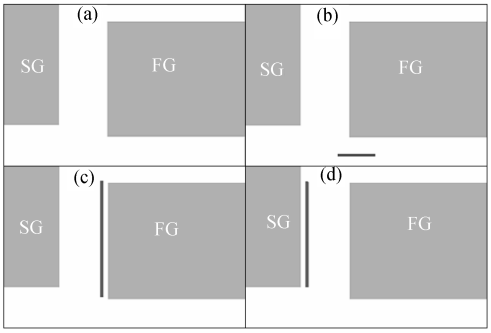

Figure 5: Electron trapping location simulated structure: (a) Without electron trapping; (b) Electron trapping at the injection point of FGOX; (c) Electron trapping in TUNOX at the FG side; (d) Electron trapping in TUNOX at the SG side.

write efficiency. But the net charge in the written state will remain nearly unchanged. Based on different phenomena between pre-cycling and post cycling electron amount alteration in the floating gate between the program state and the erase state, in combination with non-degradation of the sub-threshold slope, we can conclude that major oxide traps should exist in IPO between SG and FG.

Moreover, in this study, we did not see the single electron trapping/de-trapping events[7] in the triple-gate flash device. A possible reason should be planar shaped erasing mode in triple-gate flash compared to the horn-shaped erasing mode in the double poly SuperFlash flash cell.

3.3. Trap location simulation and mechanism analysis

Figures 5 and 6 give the electron trapping location TCAD identification structure and result W/O traps at different locations compared to the UV erasure results with/without 60000 W/E cycles. As can be seen from Fig.6, the curves with electron trapping in TUNOX show a similar sub-threshold slope as that without electron trapping. However, severe degradation is observed with electron trapping in FGOX. The simulation results are in agreement with the observation above. The magnitude of the tunneling oxide traps is approximate 10^{12} cm^{-3} after 60000 P/E cycles from the simulation result.

The endurance degradation mechanism in the triple-gate flash cell can be explained as below. Due to high electric field existence during erasure, as well as worse oxide integrity of tunneling oxide against coupling oxide, more traps will be generated in the tunneling oxide during W/E cycles. With the electrons trapped during the erasure procedure,

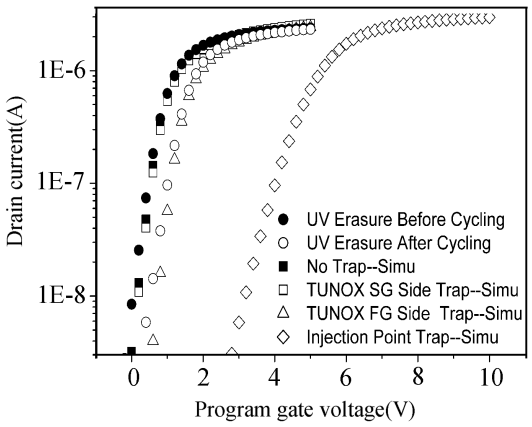

Figure 6: Electron trapping location simulation results, showing that the sub-threshold slope nearly does not degrade with electron trapping in TUNOX compared to severe degradation with electron trapping in FGOX.

the FN tunneling field will depressed and result in lower FG potential. Finally, the cell current will be degraded and lead to the failure of endurance.

4. Conclusion

In this paper, the endurance degradation after write/erase cycles in triple-gate flash memory have been detected and analyzed using UV erasure. Comparing the *I-V* curve with UV erasure before and after the cycling test, it is found the weak erase is dominated by the generation of electron traps in the tunneling oxide. This finding is contrary to the conventional point of view, which considers coupling oxide degradation after W/E cycling dominating the weak erase issue. Moreover, by TCAD simulation, the traps' location is identified again and the magnitude of their density is quantified roughly. So, in order to improve the endurance characteristic of triple-gate flash memory, optimizing the erase conditions and improving the tunnel oxide integrity is necessary.

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