

An Ultra-Low Power Embedded EEPROM for Passive RFID Tags

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Abstract: An ultra-low-power, 256-bit EEPROM is designed and implemented in a Chartered 0.35 μ m EEPROM process. The read state power consumption is optimized using a new sense amplifier structure and an optimized control circuit. Block programming/erasing is achieved using an improved control circuit. An on silicon program/erase/read access time measurement design is given. For a power supply voltage of 1.8V, an average power consumption of 68 and 0.6 μ A for the program/erase and read operations, respectively, can be achieved at 640kHz.

Key words: radio frequency identification; EEPROM; memory; charge pump; sense amplifier; low power

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1 Introduction

Recent advances in low-cost, low-power electronics and packaging have rapidly increased the area of applications for RFID, including automotive systems, supply chain management, access control, and public transport. Long-range passive tags for RFID systems do not have on-board batteries and therefore must draw power for operation from the electromagnetic field (EMF) emitted by the reader^[1]. To maximize the operating range, maximum DC power conversion (from the EMF) and minimum power consumption of the whole tag chip are desired (including the EEPROM, which is a superior nonvolatile storage solution^[2] for uniquely identifying each tag).

A distinct disadvantage of EEPROM is its large memory cell size. However, that is not important herein because the required data storage capacity in an RFID tag is small. The necessary 96-bit electronic product code (EPC) field corresponds to 10^{29} objects, which is approximately 2×10^{19} for every human now alive^[2].

This paper presents a set of design criteria for low-voltage, low-power EEPROM memory, referring to the architecture shown in Fig. 1. The focus is on the optimization of the read-out circuit and the high voltage generator. A new simple single-ended sense amplifier (SA) and an optimized pre-charging circuit are proposed for reducing the read-

ing power consumption. The EEPROM in this work can operate with only 0.6 μ A at a 1.8V supply voltage in all operations except the writing/erasing mode, where a 68 μ A current is needed.

The memory has been implemented in a Chartered 0.35 μ m EEPROM process. Testing was performed under a 1.8V power supply.

2 Memory architecture

A detailed EEPROM architecture is shown in Fig. 1. The EEPROM is composed of the input interface, the synchronous module, the memory array, and a block decoder, including block line drivers and a word decoder. The voltage switch and the

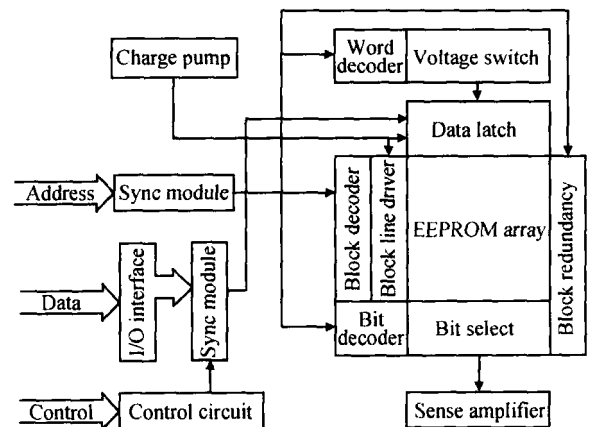


Fig. 1 Functional block diagram of the EEPROM memory

data latch module are for operation control and

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temporary data storage ,and will be programmed in parallel to the memory array. The charge pump is used to generate an internal high voltage for memory cell programming and erasing. In addition , a block including a bit decoder and sense amplifier is connected to the bit select module as the data out path. The block redundancy is for the purpose of future capacity extension. The control circuitry is necessary to manage the functional and testing operations.

The 256-bit memory array is organized into 16 blocks of 16 bits (2 bytes) . Of those ,96 bits are used to store the EPC code ,and the other bits are user-defined. A write/erase command will write/erase a whole block of 16 bits at once. Thus there are a total of 16 data latches included in this EEPROM. To minimize the power consumption ,data is read out serially. Thus only one set of read out circuits is needed.

3 Memory design optimization

3.1 Block line driving

According to the EEPROM bit cell specifications ,the block line signals must be driven above 14V in the program and erase mode ,while in the read mode ,they must be equal to the power supply voltage V_{dd} . The corresponding block line driver is shown in Fig.2. The block line driver is controlled by the read signal ,the Hven signal (which is high in the write/erase operation) ,and the output of the block decoder. The transistors (M1 ~ M4) are high voltage devices ,acting as a level shifter to drive the

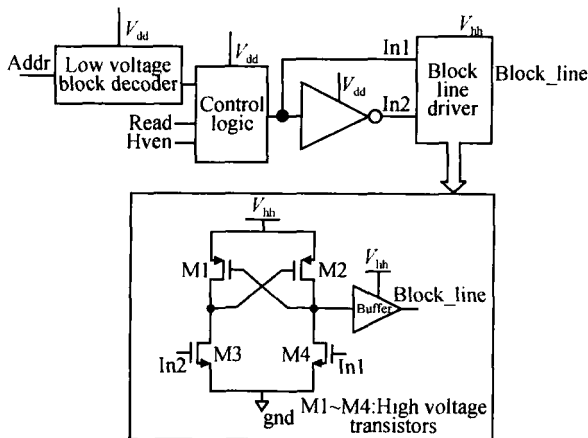


Fig.2 Block line driver description

high voltage buffer.

3.2 Read power consumption optimization

The sense amplifier is one of the most critical blocks in the peripheries of a memory ,related to the read access time. It is used to retrieve stored data from memory by amplifying small signal variations on the bit-lines^[3]. In this work ,a new single-ended sense amplifier is used ,which is shown in Fig.3 (a) . I_{cell} and C_b represent the equivalent current of the retrieved cell and the parasitic capacitance at the bit line ,respectively. I_{ref} and I_{pre} represent the reference current and the pre-charge current ,respectively. The timing diagram of the read , the pre-charge and the datasyn signal is illustrated in Fig.3 (b) .

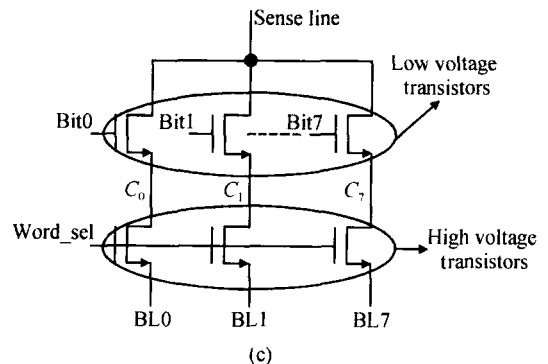
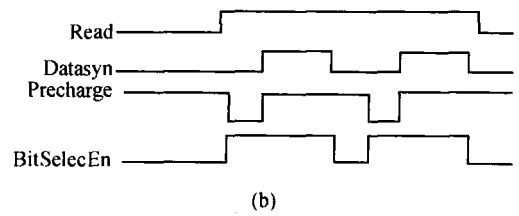
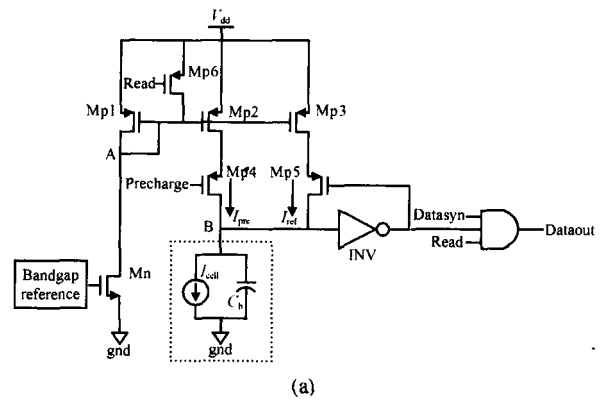


Fig.3 (a) Circuit diagram of the new single-ended sense amplifier ;(b) Timing diagram for the operation of the new sense amplifier ;(c) Schematic of the bit line select

The operation of the SA can be divided into

two phases: pre-charge and sense. When read = '0', the voltage of node A is drawn up to V_{dd} by transistor Mp6, so the SA stops working. When pre-charge = '0', the SA is in the pre-charge phase. The bit line (node B) is pre-charged to a clamped value V_{pre} , which must be higher than the input threshold voltage of the inverter. When data-syn = '1' and precharge = '1', the SA is activated to enter the sense phase. According to the specifications of this work, the simulations were performed using an I_{cell} of $10\mu A$ for the ON cell and of $10nA$ for the OFF cell, while I_{ref} was $1\mu A$ and I_{pre} was $0.6\mu A$ for limitation of the memory speed. When the sensing bit is an OFF cell ($I_{off} \ll I_{ref}$), node B is charged to V_{dd} and the data-out is '0'. When the sensing bit is an ON cell ($I_{on} \gg I_{ref}$), node B is discharged to ground and the data-out is '1'. I_{ref} and I_{cell} act as a current comparator. The transistor Mp5 and the inverter INV form a feedback loop, which is used to end the sense phase after the right output is achieved. The threshold voltage of inverter INV should be carefully designed.

The important techniques for reducing the power dissipated in the bit lines is to minimize the parasitic capacitance and limit the voltage swing. Figure 3(c) shows the optimized bit line selection circuit used in this design. Bit i is enabled by BitSelectEn, which is a combination of the datasyn and precharge signals, and Word_sel is synchronized

with the signal datasyn. Thus in the precharge phase, the parasitic capacitor in node C_i is charged, substituting the large bit line capacitor. The read power consumption is reduced because of the much smaller pre-charged parasitic capacitor, while the performance of the sense phase remains constant. In addition, those high voltage selected transistors also act as common-gate amplifiers to limit the voltage swing in node C_i .

3.3 High voltage generator

The high programming/erasing voltage used in this EEPROM is generated by a high voltage generator which consists of a charge pump and some auxiliary circuits, including a ring oscillator, a four-phase clock generator, and a discharge circuit.

Most charge pumps are based on the circuit proposed by Dickson^[4]. In recent years, several attempts have been made to minimize the body effect of the charge-transfer transistors to improve the power efficiency of the charge pump^[5,6]. Figure 4 shows the positive charge pump circuit and four-phase input clocking scheme in this EEPROM design. The positive charge pump consists of twelve stages. Each stage has an nMOS transfer gate, and one auxiliary clock and one auxiliary transistor are used to boost the gate voltage during the charge transfer operation. The pumping gain can be improved because of the lower source-drain voltage of the

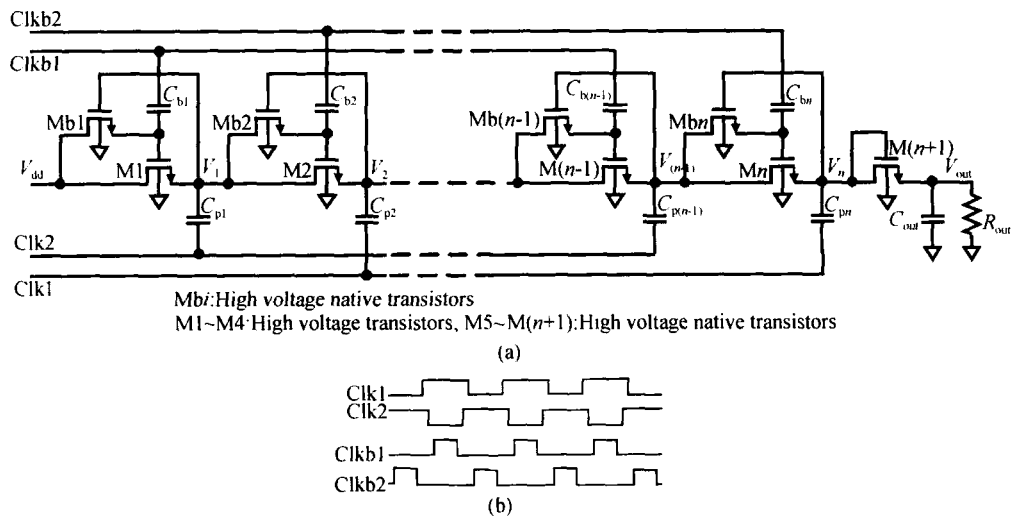


Fig. 4 (a) An n stage boosted charge pump ; (b) Four-phase clocking scheme

charge-transfer transistors. All the block lines are rapidly charged to 15V in 300μs, which is negligible compared to the program/erase pulse width of 2.5ms (shown in Fig. 5). Due to the body effect, transistors M1 ~ M4 in the charge pump are high voltage transistors and the others are all high voltage native transistors.

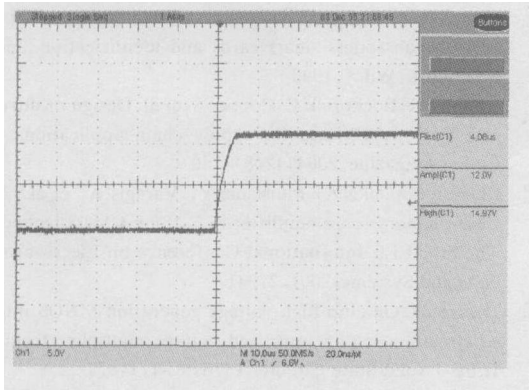


Fig. 5 Measured output waveform of the positive charge pump

The output voltage of the charge pump can be calculated by the following equations:

$$V_{out} = V_{dd} + n V - V_t = V_{dd} + n [V_{dd} - I_o R_{on} - \frac{I_o}{f(C_s + C_b)}] - V_t \quad (1)$$

$$= \frac{C_p}{C_p + C_s + C_b} \quad (2)$$

Here, V_{dd} is the power supply and also the input voltage of the charge pump circuit, C_s is the sum of the parasitic capacitors associated with each pumping node V_i , C_p is the pump capacitor, C_b is the gate-couple capacitor, I_o is the load current, f is the clock frequency, and V_t is the threshold voltage of the pass transistor caused by the body effects.

Because a high voltage is used to drive larger capacity EEPROM memory, the circuit must have a large enough I_o . The largest current load should be calculated under the chip program/erase situation^[7]. The total current consumption of an n stage charge pump is given by

$$I_{p-all} = I + I + I_{power} = (n + 1) I_o + nf(C_s + C_b) V \quad (3)$$

Thus the area of the auxiliary transistors and the boost capacitor should be designed as small as possible to minimize the power consumption. The charge pump in this paper has the advantages of relatively lower parasitic capacitors and higher voltage gain at each pumping node than other

structures listed in Refs. [5, 6].

To discharge the high voltage in a limited time regulated by the EEPROM process, a discharge circuit is added to the charge pump. The circuit diagram is shown in Fig. 6, in which transistors M1 ~ M5 are all high voltage devices. It operates as a level-shift circuit. When the discharge = '1', V_{hh} is drawn to the power supply V_{dd} in 5μs. The aspect ratio of transistor M5 is designed to be 20μm/1.5μm.

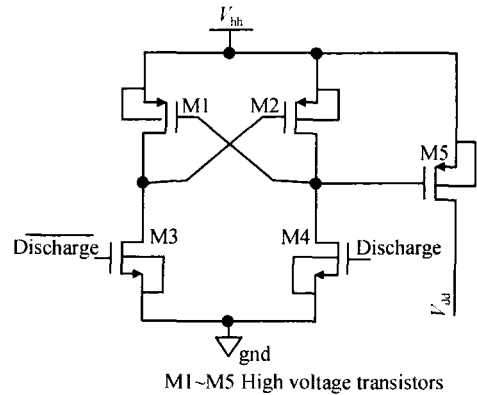


Fig. 6 Schematic of discharge unit

4 Memory testing

A micrograph of the chip is shown in Fig. 7. The cell size is 4μm × 8μm, and the core size is about 0.42mm × 0.43mm. A set of test patterns was applied to characterize the EEPROM memory. All EEPROM input signals were generated from a field programmable gate array (FPGA) and sent to a logic analyzer. The first step was the functional test. The memory testing was limited to simple

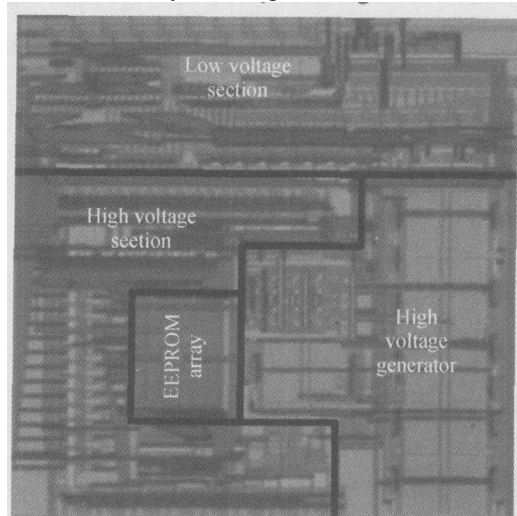


Fig. 7 Microphotograph of the 256-bit EEPROM

patterns such as all '0', all '1', random, and diagonal^[8]. Chip-erase and block-write were implemented. Chip-erase put the complete array to all '0' and was followed by the programming of a random pattern. All block programming/erasing times are 2.5ms in order to achieve the optimized retention and endurance. Because of the small capacity, time consumption is not a severe problem. The second step is the performance test. All the test patterns were programmed for a power supply of 1.8V. Different data rates were tested in the read mode. According to the test, when the data rate is 640kbps, the read and write/erase currents are only 0.6 and 68 μ A for a power supply voltage of 1.8V, respectively. The design of the read control circuit and sense amplifier is important for reducing the EEPROM reading power consumption.

5 Conclusion

In this paper, a 256-bit ultra-low-power embedded EEPROM memory suitable for RFID tags has been presented and implemented in a Chartered 0.35 μ m 2P3M EEPROM process. Designed for 1.8V operation, all standard modes of operation have been verified in this EEPROM. A novel single-ended sense amplifier with a feedback loop was

proposed for power consumption optimization. The program and erase functions have been successfully performed with an inner generated high voltage. The measurements verify the design.

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一种适用于射频电子标签的超低功耗嵌入式 EEPROM

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摘要: 采用 Chartered 0.35 μ m EEPROM 工艺设计并实现了一个适用于无源射频电子标签的 256 位超低功耗 EEPROM 存储器. 芯片实现了块编程和擦写功能, 并通过优化敏感放大器和控制逻辑的结构, 实现了读存储器时间和功耗的最优化. 最后给出了芯片在编程/擦写/读操作情况下的功耗测试结果. 在电源电压为 1.8V, 数据率为 640kHz 时, EEPROM 编程/擦写的平均功耗约为 68 μ A, 读操作平均功耗约为 0.6 μ A.

关键词: 射频识别; EEPROM; 存储器; 电荷泵; 敏感放大器; 低功耗

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