A Novel Clock Feedthrough Frequency Compensation for Fast-Settling of Folded-Cascode OTA *

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Abstract: Based on the minimum settling time (MST) theory and step-response analysis of the second order system in active switched capacitor (SC) networks, a novel clock feedthrough frequency compensation (CFFC) method for a folded-cascode OTA is proposed. The damping factor η is adjusted by using MOS capacitors to introduce clock feedthrough so that the OTA can obtain the MST state and thus achieve fast settling. Research results indicate that the settling time of the compensated OTA is reduced by 22.7%; as the capacitor load varies from 0.5 to 2.5pF, the improved settling time increases approximately linearly from 3.62 to 4.46ns; for VGA application, fast settling can also be achieved by modifying the MOS capacitor value accordingly when the closed loop gain of the compensated OTA varies.

Key words: clock feedthrough frequency compensation; fast settling; folded-cascode OTA; minimum settling time; VGA

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1 Introduction

With the rapid development of micro-processing techniques and CMOS manufacturing, active switched capacitor (SC) systems have been widely implemented in ADCs[1], active filters[2], and communication networks. In SC circuits, settling performance is the most important parameter since the settling time of the OTAs determines the maximum clock frequency. At the same time, the DC gain of the OTAs decides the output accuracy. The folded-cascode amplifier, due to its high gain and fast settling property, has been a major basic element in SC networks.

The settling time of an OTA is strongly dependent on the phase margin[3]. In order to realize the desired fast settling characteristics, accurate frequency shaping must be employed. Several conventional approaches to shaping frequency response have been implemented, which include adding an active circuit to provide a feed-forward path[4], introducing a miller capacitance for pole-zero cancellation[5], adjusting the value of the load capacitance[6], and increasing the power dissipation of the op-amp itself. However, these methods add to the complexity of op-amp circuits, the difficulties of circuit design, and the uncertain load capacitance or bias current. It is also difficult for them to get the right phase margin for which the optimally-damped state can be achieved.

According to MST theory and the step-response analysis of second-order systems, a novel CFFC method for a folded-cascode amplifier is presented. Without compromising any other specifications, this compensation improves the OTA's settling feature by precisely adjusting the damping factor η. The detailed theoretical analysis and CFFC implementation are discussed.

2 Theoretical analysis

For a general second order system, the open-loop transfer function is $A(s) = A_0/(1 + s/\omega_1)(1 + s/\omega_2)$. Here A_0 is the low-frequency gain, and ω_1 and ω_2 stand for the dominant and the first non-dominant poles of the system, respectively.

The closed-loop feedback structure of the

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second order system is shown at the bottom right in Fig. 1. The transfer function is

$$H_{\text{closed}}(s) = -\frac{C_1}{C_2} \times \frac{\omega_1 \omega_2 A_0 \beta}{s^2 + (\omega_1 + \omega_2) s + \omega_1 \omega_2 (1 + A_0 \beta)} \tag{1}$$

where $\beta = C_2/(C_1 + C_2 + C_{\text{in}})$ is the feedback factor and C_{in} denotes the input parasitic capacitance.

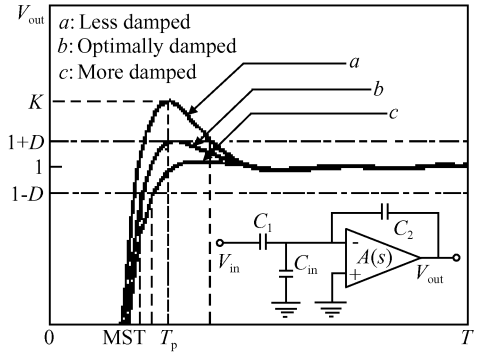

Fig. 1 Three underdamped step-responses for a second order feedback system

Since the step-response of the second order system is restricted by phase margin, which is directly reflected by ω_1/ω_2, the damping factor η of the system can be modified as

$$\eta = \frac{1}{2\sqrt{1 + A_2\beta}} \times \frac{\omega_1/\omega_2 + 1}{\sqrt{\omega_1/\omega_2}} \tag{2}$$

Let $\chi = (\omega_1/\omega_2)^{1/2}$, and assume that $A_0\beta$ is constant. Then the derivative of Eq. (2) is

$$\frac{\partial \eta}{\partial \chi} = \partial\left(\frac{1}{2\sqrt{1 + A_0\beta}} \times \frac{\chi^2 + 1}{\chi}\right) \Big/ \partial\chi$$
$$= \frac{1}{2\sqrt{1 + A_0\beta}} \times \left(1 - \frac{1}{\chi^2}\right) \tag{3}$$

Since $\omega_2 \gg \omega_1 > 0$, χ is limited between zero and one ($0 < \chi < 1$). According to Eq. (3), η will decrease as χ increases. Considering $\chi = (\omega_1/\omega_2)^{1/2}$, we can obtain the relation that η increases when we reduce $(\omega_1/\omega_2)^{1/2}$.

From the system step-response plotted in normalized amplitude versus time, as shown in Fig. 1, the following circumstances can be seen: a: less damped; b: optimally damped (MST state); c: more damped. D is the permitted gain error of this system. The settling time increases when the damping increases or decreases. When K, the voltage at the overshoot point $T = T_P$, equals $(1 + D)$, the curve for an optimally-damped state can be obtained, which minimizes the settling time. K can be adjusted by optimizing η.

As shown in Eq. (2), η is related to ω_1, ω_2, and $A_0\beta$. Given a certain gain error, $A_0\beta$ stays approximately constant. Hence, ω_1/ω_2 can be changed by introducing frequency compensation to optimize K with an appropriate phase margin so that the settling time decreases accordingly.

3 The CFFC method

Based on the theories above, a novel CFFC method for a folded-cascode amplifier is proposed. As illustrated in Fig. 2, by introducing clock feedthrough by MOS capacitors MC1 and MC2, the gate bias voltages of M0, M7 and M8 are rectified, and the branch currents are altered as well. Thus, the positions of ω_1 and ω_2 can be controlled to optimize the damping factor η for fast settling. PH1D and PH2D are a pair of opposite phase clocks, while BN1, BN2, BN3, BP2, and BP1 are all bias voltages. The OTA's overall current, which is equal to the sum of the current through M9 and M10, remains constant throughout the whole clock period. Employment of MOS capacitors is propitious for process integrating.

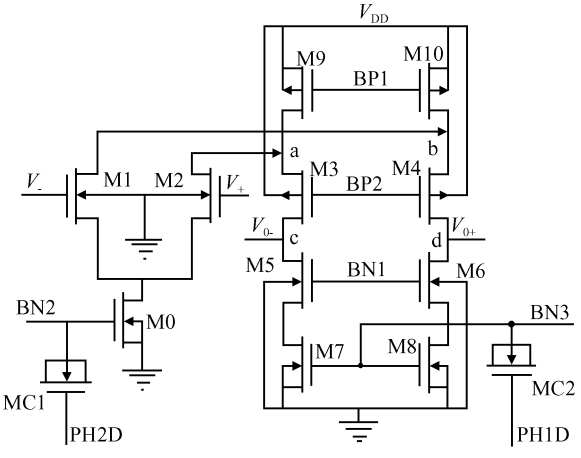

Fig. 2 Op-amp topology employing the CFFC method

The dominant pole $\omega_{c,d}$ and the first non-dominant pole $\omega_{a,b}$ are contributed by nodes c (or d) and a (or b), respectively, which can be deduced from the system transfer function

$$\omega_{c,d} \approx [(g_{ds1,2} + g_{ds9,10})(g_{ds3,4}/g_{m3,4}) + (g_{ds7,8}g_{ds5,6}/g_{m5,6})]/C_{c,d} \tag{4}$$

$$\omega_{a,b} \approx g_{m3,4}/C_{a,b} \tag{5}$$

where $C_{a,b}$ and $C_{c,d}$ represent the total capacitances at nodes a (or b) and c (or d), respectively.

$\omega_{c,d}$ and $\omega_{a,b}$ correspond to ω_1 and ω_2 in

Eq.(1), respectively. Substituting $g_{ds1-10}=\lambda_{1-10}I_{1-10}$, $g_{m1-6}=(2\alpha_{1-6}I_{1-6})^{1/2}$ into Eqs.(4) and (5) (defining α_{1-6} as the transconductance coefficient of M_1-M_6, λ_{1-10} and I_{1-10} as the channel modulation coefficient and drain-source currents of $M_1\sim M_{10}$) and solving for ω_1/ω_2 gives

$$\frac{\omega_1}{\omega_2}=\frac{1}{2}\times\frac{C_{a,b}}{C_{c,d}}\times\frac{1}{\sqrt{\alpha_{3,4}}}\left[\left(\frac{\lambda_{1,2}\lambda_{3,4}}{\sqrt{\alpha_{3,4}}}-\frac{\lambda_{5,6}\lambda_{7,8}}{\sqrt{\alpha_{5,6}}}\right)I_{1,2}+\left(\frac{\lambda_{3,4}\lambda_{9,10}}{\sqrt{\alpha_{3,4}}}+\frac{\lambda_{5,6}\lambda_{7,8}}{\sqrt{\alpha_{5,6}}}\right)I_{9,10}\right] \quad (6)$$

However, Equation (6) is too complex for us to see how to modify the value of ω_1/ω_2. It needs to be explored further. Keeping bias BP1, $I_{9,10}$, and the parameters of M_9, M_{10} invariable, the voltages at nodes a and b are constant, so that $C_{a,b}$ remains constant for all time due to the relation $C_{a,b}\propto(1+V_{a,b}/\Psi_0)^{1/2}$, where Ψ_0 is the built-in potential. As the load capacitance is much larger than the parasitical one at the output, $C_{c,d}$ approximately equals the load capacitance. Therefore, $C_{a,b}/C_{c,d}$ remains constant. Thus the relation $(\omega_1/\omega_2)\propto I_{1,2}$ is satisfied.

Now let us take account of the less damped and analyze how the settling time of OTA is optimized with the CFFC method.

In Fig.2, the clock feedthrough of MC2, coupled to the gate bias BN3, triggers an up-pulse so that the currents $I_{7,8}$ through M7 and M8 are enhanced. Meanwhile, the clock feedthrough is coupled to BN2 by MC1, producing a down-pulse that reduces the current I_0 of M0. Since I_0 is the sum of I_1 and I_2, the latter two decrease. According to Eq.(6) and Eq.(2), if $I_{1,2}$ falls, ω_1/ω_2 will decrease and η will increase. As a result, K is optimized accordingly, which ensures the optimized damped state. Since the currents through M9 and M10 remain constant, no extra power is dissipated.

As to the more damped state, the same compensation approach can be employed to achieve fast settling.

4 Simulation results and discussion

Cadence EDA simulation is done with a 0.35μm 3.3V AMS Si CMOS model. Let both C_1 and C_2 be 1.5pF. The total current of this OTA is 6.04mA, the input being a step signal with a 1V magnitude. The system gain error is set to $\pm0.1\%$ with a fixed load capacitance of 1.5pF.

As described in Table 1, ω_1/ω_2 is reduced from 0.333×10^{-3} to 0.307×10^{-3} by employing CFFC compensation, which results in the decrease of the settling times from 5.12 to 3.96ns, while $A_0\beta$ nearly remains constant.

Table 1　Comparison of the specifications without/with compensation

Item	Without Comp.	With Comp.
ω_1/kHz	173.61	179.59
ω_2/MHz	522.01	584.26
ST/ns	5.12	3.96
$A_0\beta$/dB	63.74	63.95
η	0.699	0.718
Phase margin/(°)	58.5	61.9
Power/mW	19.93	19.94

In Fig.3, the two settling signals are both between the allowed gain errors (dashed lines). This shows that CFFC shortens the settling time by 1.16ns, or 22.7%. The glitches at the end of the two curves are due to the clock feedthrough. As shown in this figure, by setting the sampling clock edge of the latter circuits before the glitch state, the settled signals can be obtained with no influence from glitches. When the power supply equals 3.0, 3.3, and 3.6V, respectively, the settling times of the OTA with CFFC are 4.18, 3.96, and 3.98ns correspondingly as shown in curves *a*, *b*, and *c* of Fig. 3. Based on the CFFC mechanism, we can find that these compensation effects are immune from environment variables, such as temperature and bias deviation.

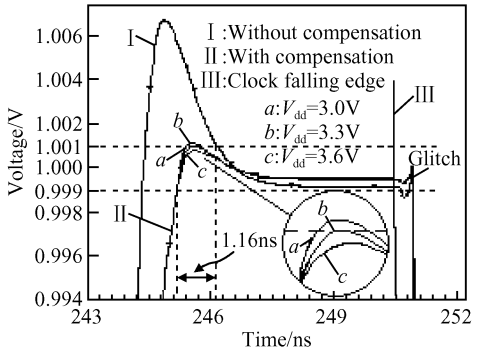

Fig.3　System step-responses with/without compensation

Figure 4 shows the settling characteristics related to variable load capacitances. Only when the load capacitance is 1.95pF is the amplifier without CFFC situated in the MST state. On the other

hand, the amplifier achieves fast settling at each value of the load with the CFFC method.

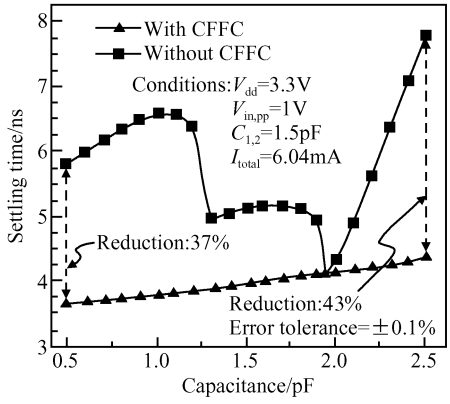

Fig. 4 Settling time of the OTAs versus the capacitance load for common values of the error tolerance ±0.1%

As the capacitance load varies from 0.5 to 2.5pF, the improved settling time increases approximately linearly from 3.62 to 4.46ns, while the unoptimizable settling time alters irregularly from 5.75 to 7.82ns. This characteristic can be applied to high speed SC circuits with variable load capacitances.

5 Application

Based on the above theoretical analysis and simulation, the CFFC structure satisfies frequency compensation for the system in different states, and the settling performance optimization.

The proposed folded-cascode OTA with CFFC can be used in a variable gain amplifier VGA, which is realized by the changes of input or feedback impedance modules. A VGA realized by changes of input capacitances is shown in Fig. 5,

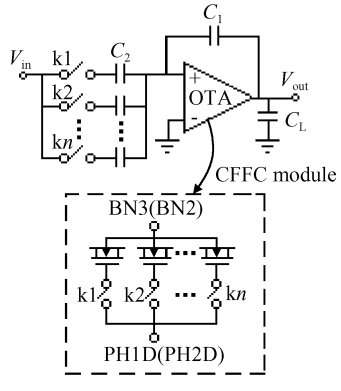

Fig. 5 VGA with capacitance array and OTA CFFC module

controlled by analog switch arrays, which are selected by a clock.

With different modes of VGA, the feedback factor β is changed, followed by shifting poles and a degraded phase margin. Thus, in order to optimize the frequency performance, the compensative circuit should be adjusted.

Table 2 compares the settling performance with and without compensation of VGA, which is shown in Fig. 5, assuming $C_1 = C_2 = C_L = 1.5$pF. The results show that the frequency performance and response speed are improved in different gain states by multiples of 1, 2 and 4.

Table 2 Comparison of ST without/with compensation

Item	Settling time/ns		
	×1	×2	×4
Without Comp.	5.12	6.47	10.26
With Comp.	3.96	5.04	7.52

Normally, the inner cells can not be adjusted after the product is finished; thus, the traditional compensation method can do nothing with it. However, according to the changes of β, the CFFC structure with a MOS capacitor array can improve the settling performance of the VGA through clock selection. The method has certain flexibilities and broader applications.

6 Conclusion

According to theoretical analysis and simulation verification, the CFFC method has been obtained. Research results indicate that CFFC shortens the settling time of a folded-cascode OTA without sacrificing other specifications; the OTA's settling time is nearly a linear function of the load capacitance from 0.5 to 2.5pF; the compensated OTA can also achieve fast settling by modifying the MOS capacitor value accordingly for VGA application.

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实现 Folded-Cascode 放大器快速建立的时钟馈通频率补偿*

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摘要：基于有源开关电容网络二阶系统最小建立时间(MST)理论和阶跃响应分析，提出了一种用于 Folded-Cascode 放大器的频率补偿新方法，即通过 MOS 电容引入时钟馈通以调整电路阻尼因子 η，使其达到 MST 状态，从而实现快速建立.研究结果表明，补偿后放大器的建立时间缩短了 22.7%；当负载电容从 0.5 变化至 2.5pF，其建立时间从 3.62ns 近似线性地增长到 4.46ns；将采用该补偿方法的放大器应用于可变增益（VGA）系统，当闭环增益变化时，仅需调整 MOS 电容值仍可实现对应状态下的快速建立.

关键词：时钟馈通频率补偿；快速建立；Folded-Cascode 放大器；最小建立时间；VGA
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