Design and Implementation of a Novel Area-Efficient Interpolator *

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Abstract: This paper presents the design considerations and implementation of an area-efficient interpolator suitable for a delta-sigma D/A converter. In an effort to reduce the area and design complexity, a method for designing an FIR filter as a tapped cascaded interconnection of identical subfilters is modified. The proposed subfilter structure further minimizes the arithmetic number. Experimental results show that the proposed interpolator achieves the design specification, exhibiting high performance and hardware efficiency, and also has good noise rejection capability. The interpolation filter can be applied to a delta-sigma DAC and is fully functional.

Key words: delta-sigma digital-to-analog converter; interpolator; halfband filter
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1 Introduction

Sigma-delta (ΣΔ) digital-to-analog converters (DACs) offer a way to achieve high resolution and low distortion with relaxed post-analog filter requirements at a lower cost than conventional Nyquist converters[1~9]. This benefit has long been recognized and utilized in digital audio systems, in which a large (16～24bits) dynamic range is required at relatively modest signal bandwidths of less than 20kHz. A typical ΣΔ DAC, as shown in Fig. 1, consists of a digital interpolation filter to bring the input sample rate up to the modulator rate, a modulator to reduce the word width by trading off the out-of-band noise, and a 1bit D/A for out-of-band noise filtering and analog signal reconstruction.

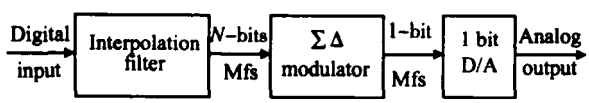

Fig. 1 Block diagram of sigma-delta DAC

In mixed digital/analog (D/A) integrated systems, digital signal processing (DSP) takes the majority of the silicon area, while the analog circuitry is limited to a very small portion. Therefore, the main obstacle in a sigma-delta DAC is the low efficiency of the area integration of the interpolator.

In this paper, we present a high performance interpolator structure that can be easily implemented in a small area. The optimization is performed so that the overall interpolator contains no general multipliers. This is achieved by using hardware-efficient FIR filters in a tapped cascaded interconnection of identical sub-filters[10], which requires no multipliers. Furthermore, as each pair of sub-filters is replaced by one of our proposed novel structures, the number of adders required further decreases.

2 Architecture

In sampled-data systems, interpolators are used to increase the sampling rate of a signal. When a high oversampling ratio is required, a cascade of interpolation stages is generally used[1]. This results in a significant reduction in overall hardware complexity as compared to a general single-stage design. The digital filter can be programmed to implement the three-stage 128-times interpolation filter that is shown in Fig. 2 (M1 = 2, M2 = 2, M3 = 32).

A cascade of two stages increases the sampling rate by a factor of 4. The use of two half-band filters for this purpose provides increased efficiency as compared to a similar design employing only one

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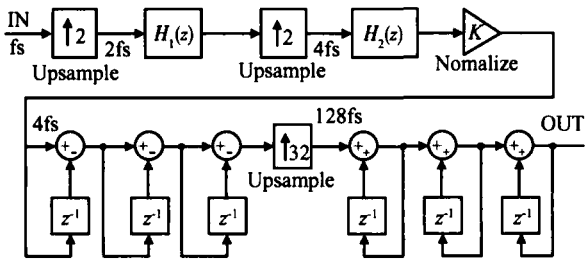

Fig. 2 Block diagram of interpolation filter

half-band filter. They are characterized by the same stop-band and pass-band ripples and symmetric cutoff frequency at around $\pi/2$. Approximately half of the coefficients in the two halfband filters are zero, thereby reducing their computational complexity by nearly 50 % as compared to a general direct-form filter architecture. This reduction, together with their symmetric impulse responses, allows the first and second halfband filters to be specified by only 13 and 6 non-zero coefficients, respectively.

A comb filter provides the remaining factor-of-32 increase in the sampling rate. The advantage of comb filters is their simple structure, which does not require any multiplier or coefficient storage, as compared with traditional FIR filters[11]. They are most efficiently implemented by cascading L stages of differentiators operating at low sample rates $(4f_s)$, followed by L stages of cascaded accumulators operating at high sample rates $(128f_s)$. Such architecture utilizes wrap-around arithmetic and is inherently stable. The transfer function for a comb filter has the general form:

$$H_3(z) = \left(\frac{1}{K} \times \frac{1 - z^{-K}}{1 - z^{-1}}\right)^L \tag{1}$$

where

$$K = M/4 \tag{2}$$

The filter has a sinc-shaped frequency response, with notches at integer multiples of f_{in} to reject images. Here a sinc filter of second order is sufficient, because high frequency images are not critical to the performance of the subsequent sigma-delta modulator. By changing K, the same interpolator structure can be used for many interpolation ratios M. In other words, the architecture of the comb filter is fixed and independent of the interpolation ratio. The detailed specifications of the halfband and sinc filters discussed in this paper are shown in Table 1.

Table 1 Specification of halfband and sinc filters

Stage	Type of filter	OSR	Passband frequency / kHz	Sampling frequency / kHz	Stopband attenuation / dB
1	Halfband	2	20	96	120
2	Halfband	2	20	192	60
3	Sinc	32	20	6144	40

3 Implementation of the interpolator

3.1 Modified halfband filter topology

This section presents the design of $H_1(z)$ and $H_2(z)$, which was accomplished by adopting the method proposed in Ref. [10] for optimally designing an FIR filter as a tapped cascaded interconnection of identical subfilters. Such a filter's main advantage lies in the fact that it has lower sensitivity to finite word length effect than traditional FIR filters do. If a traditional halfband FIR filter is used to meet the specification of $H_1(z)$, it would be nearly impossible to achieve a stopband attenuation of 120dB, assuming the coefficients are quantized to 8bits. If the coefficients are quantized to 20bits, the required filter order in this instance is more than 100, which is not an efficient and multiplier-less filter.

The transfer functions of halfband filters are:

$$H_1(z) = c(0)\, z^{-105} + F_1(z^2) \tag{3}$$

where

$$F_1(z) = \sum_{k=0}^{k=3} c(2k+1)\,(H_{11}(z))^{2k+1}\, z^{-(45-15k)} \tag{4}$$

with

$$H_{11}(z) = \sum_{n=0}^{7} h(2n)\,(z^{-n} + z^{-(15-n)}) \tag{5}$$

$$H_2(z) = d(0)\, z^{-9} + F_2(z^2) \tag{6}$$

where

$$F_2(z) = \sum_{k=0}^{1} d(2k+1)\,[H_{12}(z)]^{2k+1}\, z^{-(3-3k)} \tag{7}$$

with

$$H_{12}(z) = \sum_{n=0}^{1} g(2n)\,(z^{-n} + z^{-(3-n)}) \tag{8}$$

Coefficients $h(n)$, $g(n)$, $c(n)$, and $d(n)$ are shown in Tables 2 and 3, respectively.

Table 2 Coefficients of the first halfband filter $H_1(z)$

	Fixed coefficients	CSD encoding
$h(0) = h(30)$	- 0.0078125	-2^{-7}
$h(2) = h(28)$	0.015625	2^{-6}
$h(4) = h(26)$	- 0.0234375	$-2^{-5}+2^{-7}$
$h(6) = h(24)$	0.0390625	$2^{-5}+2^{-7}$
$h(8) = h(22)$	- 0.0625	-2^{-4}
$h(10) = h(20)$	0.109375	$2^{-3}-2^{-6}$
$h(12) = h(18)$	- 0.203125	$-2^{-2}+2^{-4}-2^{-6}$
$h(14) = h(16)$	0.6328125	$2^{-1}+2^{-3}+2^{-7}$
$H(2k+1)$	0	0
$c(7)$	- 0.15625	$-2^{-3}-2^{-5}$
$c(5)$	0.65625	$2^{-1}+2^{-3}+2^{-5}$
$c(3)$	- 1.09375	$-2^{0}-2^{-3}+2^{-5}$
$c(1)$	1.09375	$2^{0}+2^{-3}-2^{-5}$
$c(0)$	0.5	2^{-1}
$c(2k)\ (k>0)$	0	0

Table 3 Coefficients of the second halfband filter $H_2(z)$

	Fixed coefficients	CSD encoding
$g(0) = g(6)$	- 0.0859375	$-2^{-3}+2^{-5}+2^{-7}$
$g(2) = g(4)$	0.578125	$2^{-1}+2^{-4}+2^{-6}$
$g(2k+1)$	0	0
$d(3)$	- 0.5	-2^{-1}
$d(2)$	0	0
$d(1)$	1.5	$2^{1}-2^{-1}$
$d(0)$	1	2^{0}

As illustrated in Fig. 2, the input signal is upsampled by the oversampling ratio 2, and then a cascaded halfband filter is used to remove spectral images of the baseband input centered at multiples of f_s. In order to further minimize the number of registers, the traditional topology is modified by combing the upsample with the halfband filter. By putting the operation of filtering before upsampling, the basic delay element $F_1(z^2)$, z^{-2}, can be replaced by z^{-1}. Therefore, the number of registers is reduced by half. The structures resulting by properly sharing the delays between the two branches are shown in Fig. 3. Figure 3(a) gives the structure for $H_1(z)$, and Figure 3(b) for $H_2(z)$. One of the branches is a pure delay term. For $H_1(z)$, the other branch is a tapped cascaded interconnection of seven identical subfilters of order 15, and for $H_2(z)$, the other branch consists of three identical subfilters of order 3. These subfilters can be implemented effectively using a polyphase structure based on the commutative model.

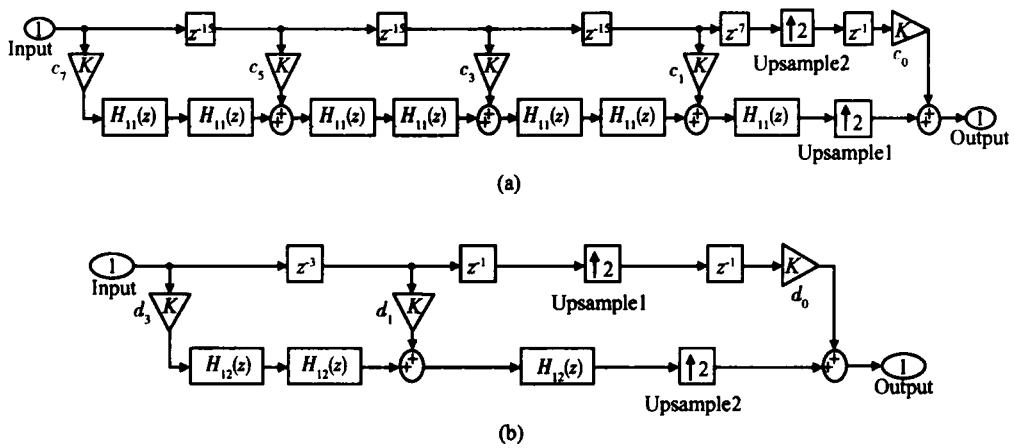

Fig. 3 Proposed structure of first-stage interpolator M1 = 2 (a) and second-stage interpolator M2 = 2 (b)

3.2 CSD coding

The subfilter coefficients and tapped coefficients for $H_1(z)$ and $H_2(z)$ are given in the left part of Tables 2 and 3, respectively. Any fraction can be expressed as[12]

$$x = \sum_{k=1}^{L} s_k 2^{-p_k} \tag{9}$$

where $s_k \in \{-1, 0, 1\}$ and $p_k \in \{0, 1, \cdots, M\}$. The representation given by Eq. (9) has $M+1$ total (ternary) digits and L nonzero digits. The CSD representation is defined as the minimal representation in which no two nonzero digits s_k are adjacent. Thus the number of adders required to realize a CSD coefficient is one less than the number of nonzero digits in the fraction. For any coefficient in FIR filters that can be translated into a CSD coefficient, we develop a MATLAB program to generate and optimize the CSD coefficients of general FIR filters. The CSD coefficients for halfband filters $H_1(z)$ and $H_2(z)$ are shown in the right part of Tables 2 and 3, respectively.

3.3 Proposed subfilter algorithm

The key block in the modified halfband topology is the identical subfilter. Optimizing this subfilter structure is critical in decreasing the area and power consumption of the entire halfband filter. In this study, a novel subfilter topology is proposed for reducing the number of adders and multipliers without sacrificing performance.

As noted in Fig. 3(b), there are three identical subfilters $H_{12}(z)$ in the implementation of $H_2(z)$. The first two subfilters can be integrated into a novel structure as shown in Fig. 4(b). With this structure, the number of adders and multipliers is reduced by 50 %.

The traditional structure for two cascaded identical filters $H_{12}(z)$ is shown in Fig. 4(a), and the equivalent structure is shown in Fig. 4(b). In Fig. 4(a), the intermediate signal $Y_1(n)$ can be expressed as

$$Y_1(n) = \sum_{j=0}^{3} g(2j) \times x_1(n-j) \tag{10}$$

and

$$Y_2(n) = \sum_{j=0}^{3} g(2j) \times Y_1(n-j) \tag{11}$$

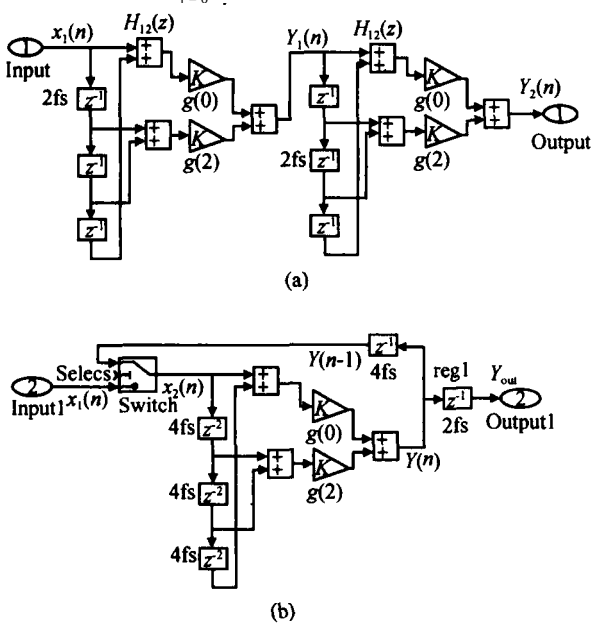

Fig. 4　Traditional and proposed structures for cascaded subfilters

The main part of the equivalent filter can be seen as an FIR filter with a length of 7. The input and output of this FIR filter are $x_2(n)$ and $Y(n)$, respectively. Its coefficient is $b(n)$, and its clock frequency is first assumed to be $2f_s$ (the sampling frequency of the stage two interpolator). The relationship between $b(n)$ and $g(n)$ is given as follows.

$$\begin{cases} b(2m) = g(2m) \\ b(2m+1) = 0 \end{cases} \quad m = 0,1,2,3 \tag{12}$$

The input signal $x_2(n)$ is the output of the switch. It functions as follows: When $n = 2k$, the switch selects signal $x_1(n)$ as its output, and when $n = 2k+1$, the switch selects the signal $y(n-1)$ as its output. Thus, $x_2(n)$ can be expressed as:

$$\begin{cases} x_2(2k) = x_1(k) \\ x_2(2k+1) = y(2k) \end{cases} \tag{13}$$

The output signal of this equivalent FIR filter can be expressed as

$$Y(n) = \sum_{j=0}^{7} b(j) \times x_2(n-j) \tag{14}$$

Substituting Eqs. (12) and (13) into Eq. (14) gives

$$\begin{aligned} Y(2k) &= \sum_{j=0}^{3} g(2j) \times x_1(k-j) \\ Y(2k+1) &= \sum_{j=0}^{3} g(2j) \times Y_1(k-j) \end{aligned} \tag{15}$$

Comparing Eq. (15) with Eqs. (10) and (11) gives

$$\begin{aligned} Y(2k) &= Y1(k) \\ Y(2k+1) &= Y2(k) \end{aligned} \tag{16}$$

The output signal $Y(n)$ is desired to be the same as the traditional cascaded filter output $Y_2(n)$. The above Equation (16) show that when $n = 2k+1$, the signal $Y(n)$ has the same value as $Y_2(k)$. Thus $Y(n)$ can be viewed as simply inserting one invalid value between each pair of adjacent values in $Y_2(n)$. The clock frequency of the registers in the equivalent filter is then increased to $4f_s$, and the signal $Y(n)$ is connected to an additional register (reg1) that operates at the frequency of $2f_s$. Thus the output of reg1 will yield the desired signal, which is the same as $Y_2(n)$.

In practice, the register that operates at a frequency of $4f_s$ is replaced by a set of double-edged registers proposed in Refs. [13,14], which can reduce the clock frequency to $2f_s$ and lower the power consumption of the circuits.

By using the type of structure illustrated in Fig. 4(b), two subfilters are replaced by the proposed structure with the number of required adders and multipliers reduced by half, simply at a cost of one selector and two registers. This greatly aids in reducing the area and power dissipation of the dig-

ital interpolator.

The first halfband filter can also be implemented using a similar structure to Fig. 4(b), although more coefficients and delay terms are required. The magnitude responses of each stage of the interpolation filter are shown in Fig. 5. It can be easily seen that the specifications stated in Section 2 are fully met with this reduced area consumption. In hardware implementations of digital filters, ripple-carry adders were used, while the multiplexers and the shifters were implemented with simple pass transistor logic.

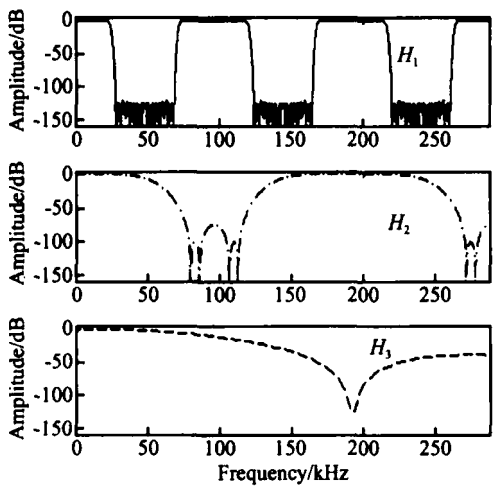

Fig. 5 Magnitude responses of the three stages of the interpolation filter

4 Experiment results

The digital interpolation filter depicted in Fig. 2 and the singleloop five-order sigma-delta modulator have been implemented and also targeted to an FPGA device provided by Xilinx™ with the XC2V2000 device chosen. Together with the 1-bit D/A fabricated in SMIC 0.18 μm mixed-signal CMOS technology, the three blocks are integrated to implement a whole delta-sigma DAC. The delta-sigma DAC has been tested and found to be fully functional. Compared to the conventional halfband filter implemented with a general direct-form topology, the area of our proposed interpolation filter is reduced by 40 % as the number of adders and shifters required to meet the filter specifications is decreased by half through adopting the proposed halfband filter topology, while the number of registers remains nearly the same. Figure 6 shows the measured output spectrum of the interpolator excited by a 0.9375kHz sinusoidal input. The interpolator was clocked by the FPGA board itself. The output of the interpolation filter was acquired with Tektronix 715 logic analyzer to verify the functionality. The spectrum was obtained by Hanning windowed 2^{10}-point FFT. It can be observed from Fig. 6 that the noise floor maintained in the filter is about 120dB. Both simulation and experiment results confirm the 120dB attenuation of stopband. The interpolation filter has already been applied into a delta-sigma DAC, and found to be fully functional.

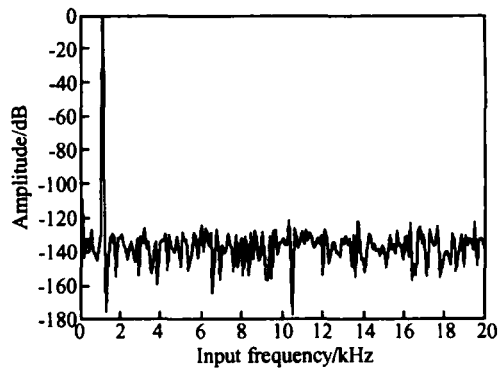

Fig. 6 Measured baseband output spectrum

5 Conclusion

A low area has been achieved in a digital interpolation filter by means of reducing computational complexity. The use of multistage architecture comprising halfband and sinc filters reduces the number of arithmetic computations to the extent that they can be performed with simple logic elements instead of a dedicated multiplier. A halfband filter topology is modified to reduce the number of adders and therefore the area. Furthermore, the proposed subfilter structure greatly aids in reducing the area and power dissipation of the digital interpolator. Simulations and measurements confirm the suitability of the proposed architecture for the implementation of an area-efficient digital interpolation filter.

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一种新型节省芯片面积的数字插值滤波器的设计与实现 *

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摘要: 提出了一种插值滤波器的设计与实现的新方法,并最终将其实现. 该方法适合于过采样数模转换器. 为减小芯片面积及设计复杂度,采用一种等同子滤波器级联设计方法,并对其改进. 同时,提出了一种新型的等同子滤波器实现结构,进一步减少了芯片实现所需的硬件. 测试结果表明,芯片达到了设计指标,节省了芯片面积,并显示出良好的噪声抑制性能. 该数字插值滤波器已经被成功应用于一款过采样数模转换器.

关键词: 过采样数模转换器; 数字插值滤波器; 半带滤波器

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