第27卷 第9期
2006年9月

半 导 体 学 报
CHINESE JOURNAL OF SEMICONDUCTORS

Vol. 27 No. 9
Sep., 2006

Study on the Characteristics of SOI DTMOS with Reverse Schottky Barriers*

Bi Jinshun† and Hai Chaohe

(Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)

Abstract: Silicon-on-insulator dynamic threshold voltage MOSFETs with $TiSi_2/p^-Si$ as reverse Schottky barriers (RSB) are presented. With this RSB scheme, DTMOS can operate beyond 0.7V, thus overcoming the drawback of DTMOS with the gate and body connected. The experimental results demonstrate that the threshold voltage in DT mode with an RSB is reduced by about 200mV at room temperature. SOI MOSFETs in DT mode with an RSB have advantages such as excellent subthreshold slope and high drivability over those under normal mode operation. The breakdown characteristics of SOI MOSFETs in the off-state are compared for the DT mode with RSB, floating body mode, normal mode.

Key words: SOI; dynamic threshold; Schottky barrier
EEACC: 2560
CLC number: TN386 **Document code:** A **Article ID:** 0253-4177(2006)09-1526-05

1 Introduction

As the critical dimensions of devices are scaling down, supply voltage must be reduced to achieve good device performance and low power dissipation. For circuit speed considerations, the threshold voltage must be dropped as well. However, the reduction of threshold voltage gives rise to another problem, the increase of off-state current, which can consume more standby power in a static circuit and increase the possibility of failure in dynamic circuits and memory arrays[1~3].

The dynamic threshold voltage MOSFET (DTMOS) proposed by Assaderaghi *et al.*[1] resolves the above problems. By shorting the gate to the body, the threshold voltage under DT mode operation is reduced due to the forward biasing of the body/source junction, so the drivability is drastically improved in the on state. Since the device exhibits the same normal mode threshold voltage in the off state (because $V_{GS} = V_{BS} = 0V$), low standby power consumption is retained. Subthreshold slope and short channel effects are also significantly improved due to the dynamic body potential[4~6].

However, the pn diode between the body and source turns on if $V_{GS} = V_{BS} > 0.7V$ for n-channel DTMOS. A considerably large leakage current due to the turn-on diode current between body and source is a disaster in DT mode. Therefore, the power supply voltage for DTMOS is restricted to 0.7V[1]. Ways to raise the power supply of DTMOS have been studied, such as a planar double gate DTMOS structure[7,8] and a shallow source/drain junction[9]. But these methods increase process complexity. In this paper, DTMOS with a $TiSi_2/p^-$ Si reverse Schottky barrier on the body contacts is proposed. Using this structure, DTMOS can be operated beyond 0.7V and exhibit excellent device performance. As much as we know, this is the first time that SOI DTMOS with a $TiSi_2/p^-$ Si reverse Schottky barrier is presented.

2 Device fabrication

The 8μm/0.8μm DT nMOSFETs with reverse Schottky barriers were fabricated on 150mm SIMOX (separation by implanted oxygen) wafers from Simgui Corp. The material parameters are as follows: p (100), 10~20Ω·cm, 500nm-thick top silicon film, and 375nm-thick BOX (buried oxide). Initially, the thickness of the top silicon film was reduced to 400nm by growing and stripping sacrifice oxide. Then LOCOS (local oxidation of silicon)

* Project supported by the State Key Development Program for Basic Research of China (No. 2006CB3027-01)
† Corresponding author. Email: bravehawk@126.com
Received 21 February 2006, revised manuscript received 24 April 2006
© 2006 Chinese Institute of Electronics

technology was used to isolate devices followed by field implantation of B^+ ions. Back channel implantation of B^+ ions and front channel implantation of BF_2^+ ions were performed to avoid leakage through the back channel and adjust the threshold voltage of the front channel. A 0.8μm-length gate was formed with 18nm gate oxide followed by LDD implantation. Arsenic and phosphorus ions were implanted to form an n^+ source/drain and a poly-gate, respectively. In order to activate the impurities that implanted in the silicon film, a rapid thermal processing (RTP) at 1000 ℃ was performed. A 30nm Ti film was sputtered followed by a 20nm capping layer of TiN. Two-step RTA was used for Ti-silicidation. After the silicidation, the devices were metallized using a typical back-end flow. SOI normal mode, floating mode, and DT mode with GBC nMOSFETs were also fabricated through the same process. The only difference in layout between the DTMOS with GBC and DTMOS with RSB structures shown in Fig. 1 below is whether the body contact region was implanted with a high dosage of boron ion. If p^+ implantation was performed, then ohmic contact is formed between the gate and body. If not, the gate and body are connected by a reversed Schottky barrier. Figure 2 gives a schematic cross sectional view of the SOI DT nMOSFETs with GBC and RSB ($TiSi_2/p^-$ Si) structures in this paper.

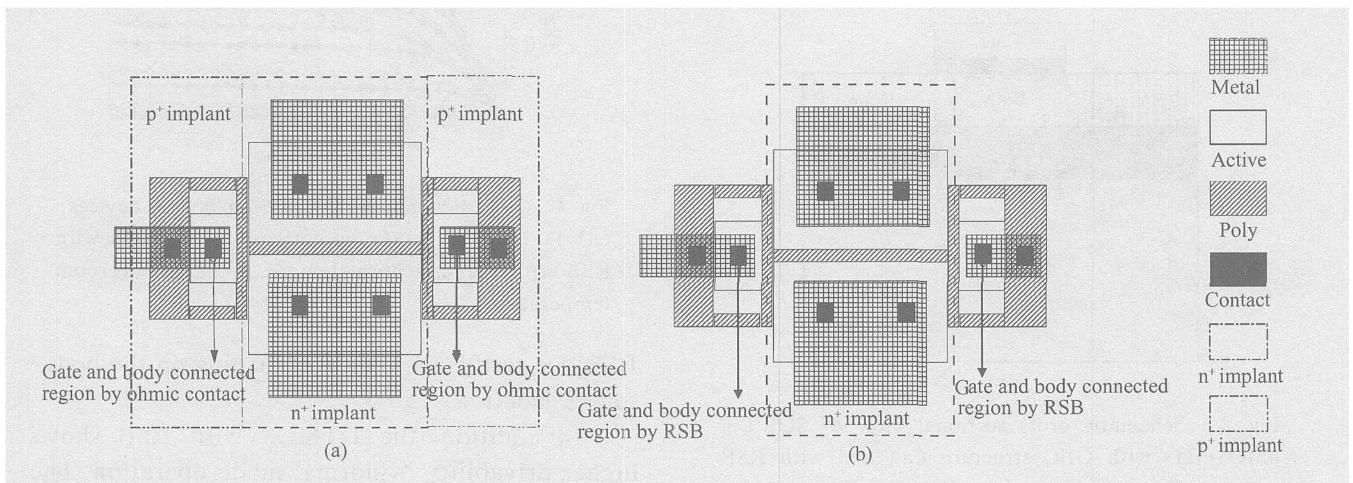

Fig. 1 Layouts of DTMOS with gate and body connected directly (a) and DTMOS with gate and body connected by reversed Schottky barrier (b)

3 Results and discussion

After the formation of 8μm/0.8μm devices, electrical characterizations were carried out with a Keithley 4200SCS semiconductor characteristics system. The drain currents of 1×10^{-6}A and 1×10^{-5}A are defined as threshold voltage and breakdown voltage points, respectively.

The gate-to-body connection of the DTMOS with RSB was through an n^+ polysilicon gate, $TiSi_2/p^-$ Si Schottky barrier and p^- body. The basic principle of DTMOS with RSB is the dynamic potential of the body that changes with the gate voltage to vary the threshold voltage. Since the $TiSi_2/p^-$ Si Schottky barrier is reverse-biased, the pn junction of the body/source will not turn on when $V_{GS} > 0.7$V. This is the reason why SOI DTMOS with RSB can work beyond 0.7V. Figure 3 illustrates the characteristics of the 2μm × 2μm Schottky barrier diode in this study.

The *I-V* function of the Schottky diode can be expressed as $I = I_s\exp(qV/nkT)$, $I_s = ST^2 \times A^*\exp(-\phi_B/kT)$. A^* is the effective Richardson constant, V is the bias voltage, I_s is the saturation current, S is the area of the Schottky diode, ϕ_B is the potential barrier height, and n is the ideality factor. From calculation, ϕ_B and n in this work are about 0.52V and 1, respectively.

Figure 4(a) shows the output characteristics of DTMOS with GBC. It is obvious that as $V_{GS} > 0.7$V, significant leakage occurs through the turn-on of the body/source junction. This is the reason that DTMOS with GBC only works under 0.7V in

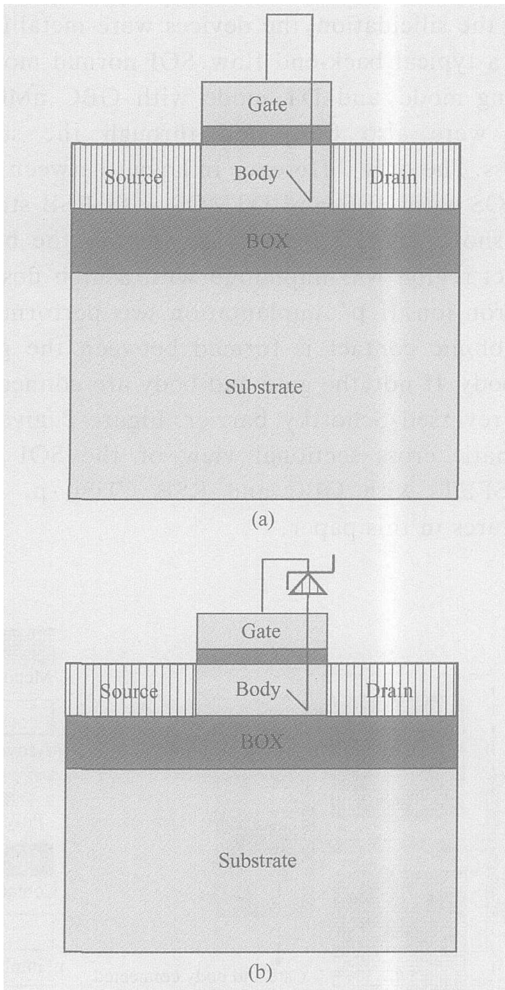

Fig. 2 Schematic cross sectional view of SOI DT nMOSFETs with GBC structure (a) and with RSB structure (b)

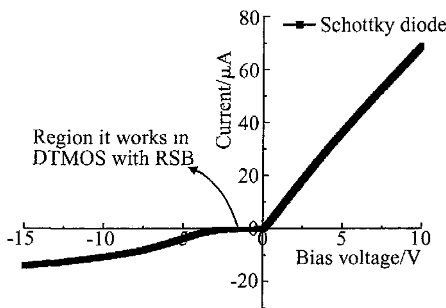

Fig. 3 Characteristics of the 2μm ×2μm Schottky barrier diode in this study with $TiSi_2$ portion fixed at 0V and sweeping the voltage of p-body

many reports. Figure 4(b) gives the output characteristics of normal mode operation (H-gate and body contacts are fixed at 0V) and a DTMOS with RSB at room temperature, where V_{GS} varies from 0.5 to 3V, with a 0.5V step. No obvious leakage current was observed in the DTMOS with

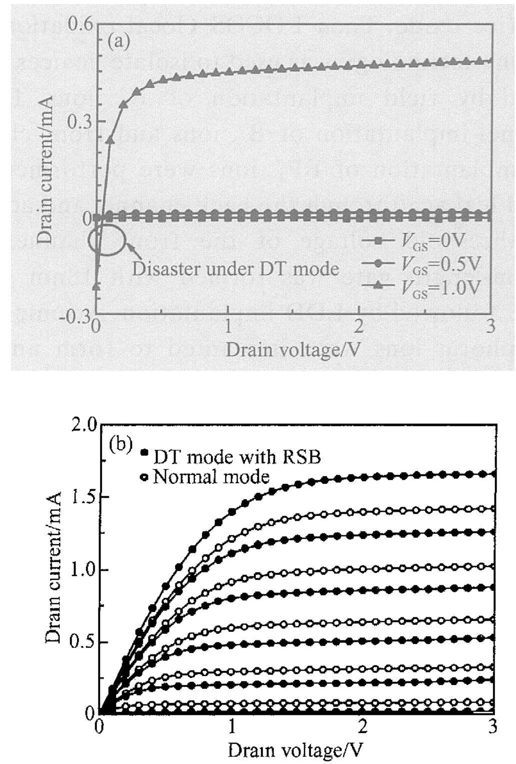

Fig. 4 Output characteristics of 8μm/0.8μm devices (a) DTMOS with GBC structure; (b) DTMOS with RSB structure and normal mode operation at room temperature

RSB due to the avoidance of turning on the body/source junction.

In addition, the DTMOS with RSB shows higher drivability in normal mode operation. The threshold voltage of the DTMOS with RSB drops when the gate voltage rises, so the difference of drive current between the DTMOS with RSB and normal mode operation is greater. But the ratio of I_{on} (DTMOS with RSB) and I_{on} (normal mode operation) decreases. The ratio is 3 when V_{GS} = 1V, 1.4 when V_{GS} = 2V, and 1.22 when V_{GS} = 3V.

Figure 5 gives a comparison of subthreshold characteristics between the DTMOS with RSB structure and normal mode operation at room temperature. The leakage currents of these devices in the off state are almost the same. For normal mode operation, V_{DS} = 0.1V, the SS (subthreshold slope) = 100mV/dec, and the threshold voltage V_T = 580mV, while V_{DS} = 3V, the SS = 97.5mV/dec, and the threshold voltage V_T = 560mV. For the DTMOS with RSB, V_{DS} = 0.1V, the SS = 67.2 mV/dec, and the threshold voltage V_T = 380mV while V_{DS} = 3V, the SS = 65.3mV/dec, and the

threshold voltage $V_T = 370mV$. We assume that the subthreshold slope has a value near the ideal subthreshold slope (60mV/dec) at room temperature, which indicates good device performance.

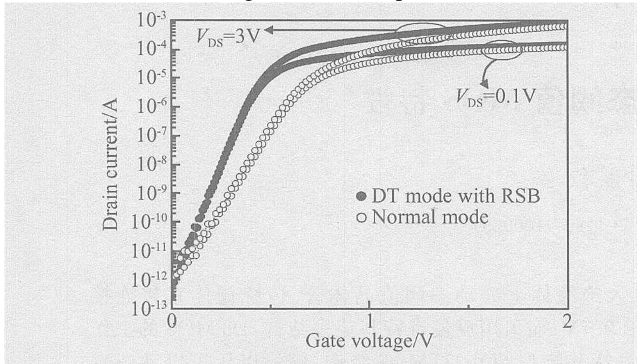

Fig. 5　Subthreshold characteristics of normal mode operation and DTMOS with RSB under drain bias of 0.1 and 3V for comparison

Here we consider the reason why the subthreshold slope of the DTMOS with RSB is so perfect. As described in Ref. [10], the subthreshold slope is equal to nkT/qln10 under normal mode operation. But in DTMOS, the SS equation is changed to be:

$$SS = \left(\frac{\partial \lg I_D}{\partial V_{GS}}\right)^{-1} = \frac{n(V_{GS})kT\ln 10}{q\left[1 - \frac{\partial V_{TH}}{\partial V_{GS}}\right]}$$

Also, $n = 1 + \frac{C_D}{C_{OX}} + \frac{C_{it}}{C_{OX}}$. Here C_D is the depletion layer capacitance, $C_{it} = qD_{it}$, D_{it} is the interface-trap density, and C_{OX} is the gate capacitance. Reference [1] points out the fact that in DT mode, the reduced threshold voltage is due to the reduction of the body charge and C_D. When the threshold voltage becomes minimal, the body charge is totally eliminated. Therefore n is reduced with the rise of V_{GS}. On the other hand, $\frac{\partial V_{TH}}{\partial V_{GS}}$ is negative, as mentioned in Ref. [7]. As a result, the DTMOS with RSB shows perfect subthreshold characteristics.

The off-state breakdown characteristics are illustrated in Fig. 6. The breakdown voltage of floating body mode operation is 6.2V because of the influence of FBE (floating body effect), while the breakdown points of normal mode operation and the DTMOS with RSB reach 11.7 and 11.8V respectively. The breakdown curve of the DTMOS with RSB is a bit steeper than that of normal mode operation, as shown in Fig. 6.

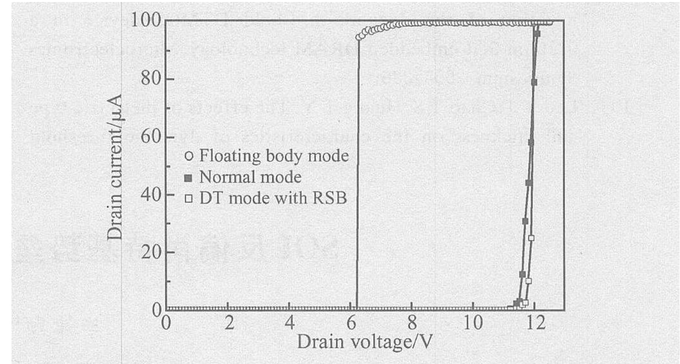

Fig. 6　Off-state breakdown characteristics of floating body mode operation, normal mode operation and DTMOS with RSB

4　Conclusion

DTMOS with a $TiSi_2/p^-$ Si reverse Schottky barrier on the body contacts is proposed. This type of device structure does not require extra process steps and is compatible with SOI technology. A DTMOS with RSB extends the power supply voltage of DTMOS with GBC beyond 0.7V. Both the saturation current and subthreshold slope can be improved by this scheme.

References

[1] Assaderaghi F, Hu C M, Ko P K, et al. Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI. IEEE Trans Electron Devices, 1997, 44(3):414
[2] Roy K, Mukhopadhyay S, Mahmoodi-Meimand H. Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. Proceedings of the IEEE, 2003:305
[3] De la Hidalga-W F J, Deen M J. The dynamic threshold voltage MOSFET. Devices, Circuits and Systems, 2000:D63/1
[4] Lin S C, Yuan K H, Kuo J B. Short-channel effects of SOI partially-depleted (PD) dynamic-threshold MOS (DTMOS) devices. Electron Device Meeting, 2000:48
[5] Chang S J, Chang C Y, Chen C, et al. High-performance and high-reliability 80-nm gate-length DTMOS with indium super steep retrograde channel. IEEE Trans Electron Devices, 2000:23794
[6] Chang S J, Chang C Y, Chao T S, et al. High performance 0.1μm dynamic threshold MOSFET using indium channel implantation. IEEE Electron Device Lett, 2000, 21(3):127
[7] Bi Jinshun, Wu Junfeng, Hai Chaohe. Simulation of a double-gate dynamic threshold voltage fully depleted silicon-on-insulator nMOSFET. Chinese Journal of Semiconductors, 2006, 27(1):35
[8] Yamaoka M, Osada K, Itoh K, et al. Dynamic-V_t, dual-power-supply SRAM cell using D2G-SOI for low-power SoC application. IEEE International SOI Conference, 2004:109
[9] Burke F, Rambhatla A, Zahurak J, et al. Source/drain opti-

mization of the dynamic-threshold DTMOS device in a 0.15μm SOI embedded DRAM technology. Microelectronics Symposium,2003:336

[10] Lee YJ,Chao TS,Huang T Y. The effects of dielectric type and thickness on the characteristics of dynamic threshold metal oxide semiconductor transistors. Jpn J Appl Phys, 2003,42:5405

[11] Bi Jinshun, Hai Chaohe, Han Zhengsheng. An overview of SOI DTMOS (dynamic-threshold MOSFET). Chinese Journal of Electron Devices,2005,28(3):111

SOI 反偏肖特基势垒动态阈值 MOS 特性*

毕津顺† 海潮和

(中国科学院微电子研究所, 北京 100029)

摘要: 将 Ti 硅化物-p 型体区形成的反偏肖特基势垒结构引入绝缘体上硅动态阈值晶体管. 传统栅体直接连接 DTMOS,为了避免体源二极管的正向开启,工作电压应当低于 0.7V. 而采用反偏肖特基势垒结构,DTMOS 的工作电压可以拓展到 0.7V 以上. 实验结果显示,室温下采用反偏肖特基势垒 SOI DTMOS 结构,阈值电压可以动态减小 200mV. 反偏肖特基势垒 SOI DTMOS 结构相比于传统模式,显示出优秀的亚阈值特性和电流驱动能力. 另外,对浮体 SOI 器件、传统模式 SOI 器件和反偏肖特基势垒 SOI DTMOS 的关态击穿特性进行了比较.

关键词: SOI; 动态阈值; 肖特基势垒

EEACC: 2560

中图分类号: TN386 **文献标识码**: A **文章编号**: 0253-4177(2006)09-1526-05

* 国家重点基础研究发展计划资助项目(批准号:2006CB3027-01)

† 通信作者. Email:bravehawk@126.com

2006-02-21 收到,2006-04-24 定稿

© 2006 中国电子学会