A Low-Power High-Frequency CMOS Peak Detector

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Abstract: A low-power, high-frequency CMOS peak detector is proposed. This detector can detect RF signal and base-band signal peaks. The circuit is designed using SMIC 0.35μm standard CMOS technology. Both theoretical calculations and post simulations show that the detection error is no more than 2% for various temperatures and processes when the input amplitude is larger than 400mV. The detection bandwidth is up to 10GHz, and its static current dissipation is less than 20μA.

Key words: CMOS; peak detector; lower power; high frequency
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1 Introduction

Peak detectors are widely used in different circuits and systems, such as AGCs (automatic gain controls)[1], oscillators[2], and power amplifiers[3]. Generally, a peak detector uses a diode as its detection component, and its accuracy is limited by the uncertainty in the turn-on characteristic of the diode. This problem can be overcome by adding an operational amplifier, but the operational amplifier must consume extremely large current in order to operate at high frequencies. Meyer[4] reported a low-power high-frequency bipolar peak detector. However, it can only be used for RF signal peak detection. In this paper, a low-power high-frequency CMOS peak detector, which can detect both RF signal and base-band signal peaks, is proposed. It is designed using SMIC 0.35μm standard CMOS technology. Both theoretical calculations and post simulations show that it operates at frequencies up to 10GHz, and the detection error is less than 2% when the input amplitude is larger than 400mV.

2 Detection principle

Figure 1 shows a schematic of the proposed peak detector. The input MOS transistor M1 acts as a nonlinear rectifying element. If the ratio of I_S to C is small enough, the voltage at node S will follow the peak of the input signal. Unfortunately, there is an inherent voltage drop V_{GS1} that is dependent on process and temperature. The MOS transistor M2 is introduced to compensate this voltage drop so that the output voltage can detect the input peak accurately. In order to eliminate the effect of channel length modulation of M1 and M2, an operational amplifier composed of MA1～MA4 is added.

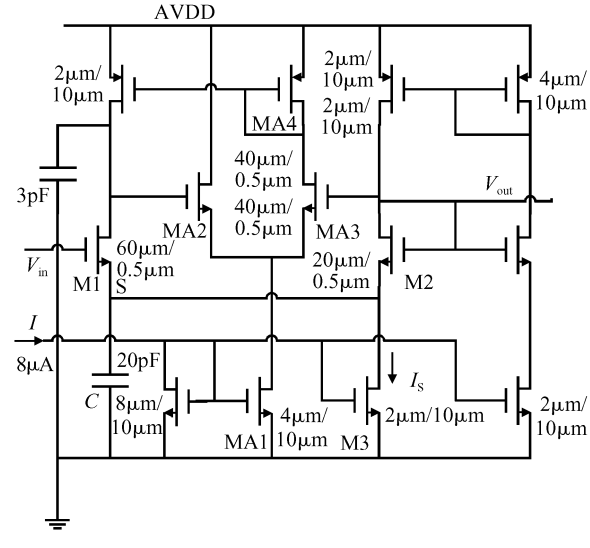

Fig. 1 Schematic of the proposed peak detector with detailed bias circuit

Transistors M1 and M2 equally share the tail current I_S. Because the tail current is small, both of them operate in the subthreshold region. With the addition of the operational amplifier, M1 and

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M2 have the same drain-source voltage; therefore, their source currents can be given by

$$I_1 = I_{SO} \times \left(\frac{W}{L}\right)_1 \times \exp[(V_{GS1} - V_{T1})/(nU_T)] \times [1 - \exp(-V_{DS}/U_T)] \quad (1)$$

and

$$I_2 = I_{SO} \times \left(\frac{W}{L}\right)_2 \times \exp[(V_{GS2} - V_{T2})/(nU_T)] \times [1 - \exp(-V_{DS}/U_T)] \quad (2)$$

where $(W/L)_1$ and $(W/L)_2$ are the aspect ratios of M1 and M2, respectively, I_{SO} is a process parameter, n is the slope factor, which is about 1.58 in the technology we used, and U_T is the thermal voltage given by

$$U_T = \frac{kT}{q} \quad (3)$$

According to Kirchhoff's current law, the average current of M1 equals I_S-I_2. Therefore

$$I_S - I_2 = \frac{1}{T}\int_0^T I_1(t)\mathrm{d}t \quad (4)$$

where T is the period of the input signal. We assume that the input voltage has the form of

$$V_{GS1} = V_B + A \times \sin\left(\frac{2\pi}{T}t\right) \quad (5)$$

Combining Eqs. (1)～(5) yields

$$V_O = V_B + nU_T \times \ln\left[\frac{(W/L)_1}{(W/L)_2}\right] + nU_T \times \ln\left\{\int_0^1 \exp\left[\frac{A}{nU_T}\sin(2\pi r)\right]\mathrm{d}r\right\} \quad (6)$$

The integral in Eq. (6) can be approximated for a large input amplitude as[4]

$$\int_0^1 \exp\left[\frac{A}{nU_T}\sin(2\pi r)\right]\mathrm{d}r \approx \sqrt{\frac{nU_T}{2\pi A}} \times \exp\left(\frac{A}{nU_T}\right) \quad (7)$$

From Eqs. (6) and (7), we can derive that the output voltage is

$$V_O = V_B + A - nU_T \times \ln\left[\frac{(W/L)_2}{(W/L)_1} \times \sqrt{\frac{2\pi A}{nU_T}}\right] \quad (8)$$

The DC component of the input signal is reserved; therefore, the proposed peak detector can be used to detect base-band signal and RF signal peaks.

As shown in Eq. (8), the output voltage has an error term dependent on the input amplitude; as a result, it is difficult to cancel the detection error for different input amplitudes. Fortunately, an accurate peak can be obtained for a specified input amplitude by setting

$$\frac{(W/L)_1}{(W/L)_2} = \sqrt{\frac{2\pi A}{nU_T}} \quad (9)$$

3 Detection error

Because both U_T and n are temperature dependent, it is reasonable to determine the device dimension according to

$$\frac{(W/L)_1}{(W/L)_2} = \sqrt{\frac{2\pi A}{n_0 U_{T0}}} \quad (10)$$

where n_0 and U_{T0} are the slope factor and thermal voltage at room temperature, respectively. Substituting Eq. (10) into Eq. (8) and neglecting the input bias voltage V_B for the sake of simplicity, the output voltage can be rewritten as

$$V_O = A + \frac{nU_T}{2} \times \left[\ln\left(\frac{U_T}{U_{T0}}\right) + \ln\left(\frac{n}{n_0}\right)\right] \quad (11)$$

The temperature coefficient of the detected peak is given by

$$\mathrm{TC}(T) = \frac{1}{V_O} \times \frac{\partial}{\partial T} V_O(T) = \frac{nU_T}{2TV_O}\left[1 + \ln\left(\frac{U_T}{U_{T0}}\right)\right] \quad (12)$$

The detection result will undergo a change of 8mV when the temperature varies from −40℃ to 85℃.

Furthermore, the detection result is affected by process parameters since the slope factor is process dependent. Fortunately, because the slope factor is relatively stable in a given process[5,6], its effect on the detected peak is negligible.

The detection error formed by the DC offset voltage of M1 and M2 is given by

$$\mathrm{Error} = \frac{A_{VOS}}{\sqrt{WL}} \quad (13)$$

where A_{VOS} is a constant. Assuming A_{VOS} equals 10mV/μm, the detection error is about 2.2mV in this design.

A bias current mismatch of M1 and M2 also results in detection error. If $I_1 = I(1-\sigma)$ and $I_2 = I(1+\sigma)$, we can approximate the detection error as

$$\mathrm{Error}(\delta) = 2\delta nU_T \quad (14)$$

Assuming the current mismatch is 1%, the detection error is about 0.8mV.

4 Detection bandwidth

The 3dB bandwidth of the proposed peak detector is given by

$$f_{-3\mathrm{dB}} = \frac{9}{4\pi R_{SQ} C_{ox} W^2} \quad (15)$$

where R_{SQ} is the square resistance of the poly-

gate, which is less than 10Ω/square in the technology we used. C_{ox} equals 5fF/μm^2.

Assuming that the channel width of the input transistor is 10μm, the detection bandwidth is calculated up to 180GHz. The detection bandwidth has no relationship with the transconductance of the input transistor. Therefore, we can obtain large bandwidth with low power dissipation. The gate-distributed resistance of a large input device can be diminished by folding.

5 Post simulation results

The proposed peak detector is designed using SMIC 0.35μm standard CMOS technology. The dimension ratio of M1 to M2 is set to 8 according to Eq. (10). In order to diminish the gate-distributed resistance, both M1 and M2 are broken into several parallel transistors with a channel length of 10μm. Figure 2 shows the layout of the proposed peak detector. The distributed parasitic capacitors and resistors are extracted by Mentor Calibre.

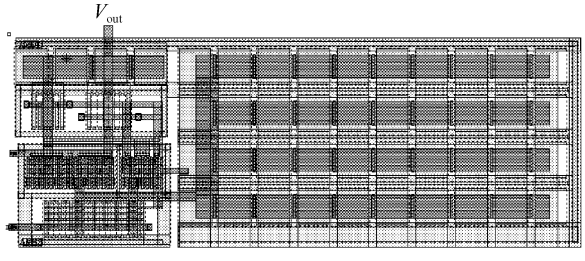

Fig. 2　Layout of the proposed peak detector

Figure 3 shows the post simulation results for TT, SS, and FF process corners, where the calculation result is also plotted. These process corners are provided by the foundry. In SMIC 0.35μm technology, the gate oxide thickness increases by 17%, the threshold voltage increases by 6%, and some other parameters such as junction capacitors also increase in the SS process corner. On the contrary, the process parameters decrease in the FF process corner. The simulation results are nearly in accordance with the theoretical analysis.

Figure 4 shows the post simulation results of the detection error versus temperature at the TT, SS, and FF corners with an input amplitude of 400mV. It is clear that the detection error is mainly caused by temperature instead of process deviation, as predicted in the preceding analysis. The

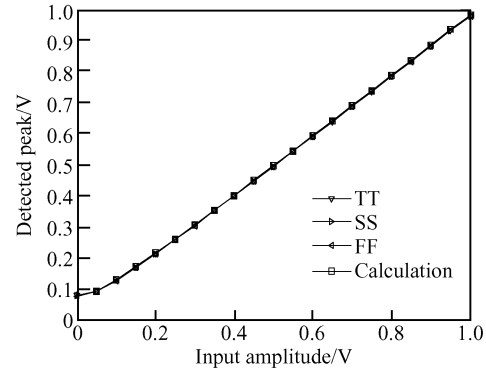

Fig. 3　Detected peak versus input amplitude

post simulation result of the normalized detected peak versus frequency for a 400mV input signal at the TT process corner at 27℃ is plotted in Fig. 5.

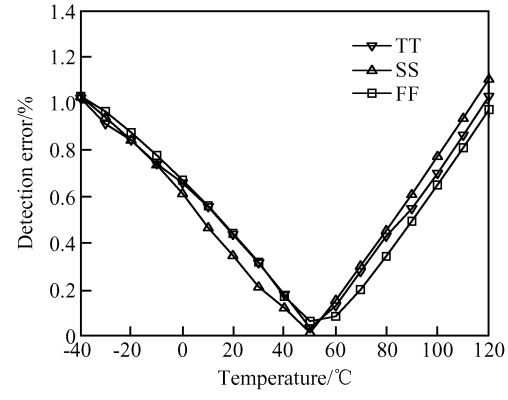

Fig. 4　Detection error versus temperature

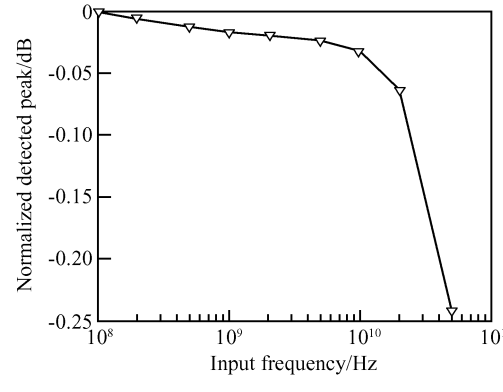

Fig. 5　Normalized detected peak versus input frequency

6 Conclusion

A low-power high-frequency CMOS peak detector is proposed in this paper. The detector is designed using SMIC 0.35μm standard CMOS technology. Both theoretical analysis and post simulations show that the detection error is no

more than 2% with the effects of process parameter and temperature when the input amplitude is larger than 400mV. The detection bandwidth is up to 10GHz, and the static current dissipation is less than 20μA.

References

[1] Khoury J M. On the design of constant settling time AGC circuits. IEEE Trans Circuits and System-II: Analog and Digital Signal Processing, 1998, 45(3): 283

[2] Lee T H. The design of CMOS radio-frequency integrated circuits second edition. Cambridge University Press, 2004: 630

[3] Cripps S C. Advanced techniques in RF power amplifier design. Artech House, 2002: 111

[4] Meyer R G. Low-power monolithic RF peak detector analysis. IEEE J Solid-State Circuits, 1995, 30(1): 65

[5] Godfrey M D. CMOS device modeling for subthreshold circuits. IEEE Trans Circuits and Systems, 1992, 39(8): 532

[6] Chen M J, Ho J S. A three-parameters-only MOSFET subthreshold current CAD model considering back-gate bias and process variation. IEEE Trans Computer-Aided Design, 1997, 16: 343

一种低功耗高频 CMOS 峰值检测电路

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摘要：给出了一个低功耗、高频 CMOS 峰值检测电路，可以用于检测射频信号和基带信号的峰值. 该电路的设计基于中芯国际 0.35μm 标准 CMOS 工艺. 理论分析和后仿真结果都表明，在工艺偏差以及温度变化条件下，当输入信号幅度在 400mV 以上时检测的误差小于 2%，检测带宽可达 10GHz 以上，整个检测电路的静态电流消耗低于 20μA.

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