A Novel Sampling Switch Suitable for Low-Voltage Analog-to-Digital Converters

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Abstract: A novel, highly linear sampling switch suitable for low-voltage operation is proposed. This switch not only eliminates the nonlinearity introduced by gate-source voltage variation, but also reduces the nonlinearity resulting from threshold voltage variation, which has not been accomplished in earlier low-voltage sampling switches. This is achieved by adopting a replica transistor with the same threshold voltage as the sampling transistor. The effectiveness of this technique is demonstrated by a prototype design of a sampling switch in 0.35μm. The proposed sampling switch achieves a spurious free dynamic range of 111dB for a 0.2MHz, 1.2Vp-p input signal, sampled at a rate of 2MS/s, about 18dB over the Bootstrapped switch. Also, the on-resistance variation is reduced by 90%. This method is especially useful for low-voltage, high resolution ADCs, which is a hot topic today.

Key words: sampling switch; nonlinearity; low-voltage; analog-to-digital converter; switched-capacitor circuits
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1 Introduction

Because of its low power consumption and reliability, the required operating voltage for CMOS technology has been decreasing significantly. This trend has resulted in enhanced performance of digital circuits through device scaling. However, the reduction in supply voltage presents formidable challenges for analog circuit design[1]. Therefore, circuit techniques that do not require process enhancements are very popular. As a critical component of analog-to-digital converters (ADCs) and switch-capacitor filters, the sampling switch (a switch on the signal path, often in front of a sampling capacitor) always determines the input signal swing and the linearity of the whole SC circuit. Achieving high linearity and a high dynamic range simultaneously under low supply voltages in deep-submicron CMOS technology has thus far been extremely challenging.

There are two main problems in low-voltage sampling switches, which we discuss in detail here. First, when the supply voltage is less than the sum of the threshold voltages of the pMOS and the nMOS, there is a large range in which the input signal cannot be well conducted by the switch. Second, the nonlinearity of the sampling switch due to gate-source voltage variation and threshold voltage variation poses fundamental limits to the achievable distortion levels of SC circuits.

Two methods have been proposed to deal with these problems without using low threshold voltage devices. One adopts a switched-op-amp[2], which avoids the use of critical switches to pass voltages in the mid-range by turning on or off the op-amps. However, the switch at the front end of the switched-op-amp cannot be avoided. Another solution uses bootstrapping techniques[3~7], either to boost the gate voltage to $2V_{dd}$ or to raise it to $V_{dd}+V_{in}$. Usually, the latter scheme is preferred since it eliminates the nonlinearity introduced by the gate-source voltage variation. However, both methods fail to eliminate the variation of the threshold voltage with respect to the input signal level. But the threshold voltage variation must be taken into account, especially for high resolution ADCs.

In this paper, a novel sampling switch is proposed, not only feasible for low-voltage applications but also with a significantly higher linearity than the previously proposed solutions.

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2 Challenge in low-voltage sampling switch design

2.1 Low-voltage operations

With the reduction of the supply voltage, the overdrive voltage of the MOS switches is lowered, inhibiting the proper operation of classical CMOS switches. The dependence of the switch conductance on the input voltage under different supply voltages is shown in Fig. 1. When the input signal V_{in} is in the range of $[0, V_{dd} - V_{thn}]$, the nMOS transistor conducts; When V_{in} is in the range of $[V_{thp}, V_{dd}]$, the pMOS transistor conducts (V_{thn} and V_{thp} are the threshold voltages of the nMOS and the pMOS, respectively).

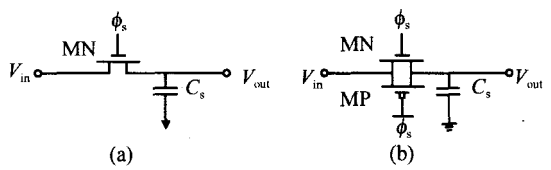

Fig. 1 (a) nMOS transistor switch; (b) CMOS transistor switch

As can be seen from the bottom case of Fig. 1, when V_{DD} is less than the sum of the two threshold voltages, there is an input signal range in which none of the transistors conduct. Therefore $V_{thn} + V_{thp}$ is the fundamental limit of the minimum supply voltage for rail-to-rail operation in CMOS switches.

2.2 Nonlinearity in a single MOS switch

Besides the difficulty in low-voltage operation mentioned above, another challenge appearing in low-voltage switches stems from the nonlinearity, which is due to the gate-source voltage variation and the threshold voltage variation[8]. This can be easily illustrated with a single nMOS switch as shown in Fig. 1(a). The dashed line in Fig. 2 shows the individual conductance of the nMOS:

$$g_{ds,n} = \mu_n C_{ox} \left(\frac{W}{L}\right)_n (V_{dd} - V_{in} - V_{thn}) \quad (1)$$

for square-law devices that operate in the linear region, the third term

$$V_{thn} = V_{th0} + \gamma_{sub} \left(\sqrt{2|\phi_f| + V_{sb}} - \sqrt{2|\phi_f|} \right) \quad (2)$$

where V_{th0} is the threshold voltage at $V_{sb} = 0$, γ_{sub} is the substrate-bias coefficient, and ϕ_f is the Fermi potential, all of which are technology-dependent parameters. g_{ds} is influenced by the input signal level in two aspects according to Eqs. (2) and (3). One is the gate-source voltage, and the other is the dependence of the threshold voltage on the source-bulk voltage. It should be noted that V_{thn} is in fact related to V_{ds}, which is not reflected in the above first-order expressions.

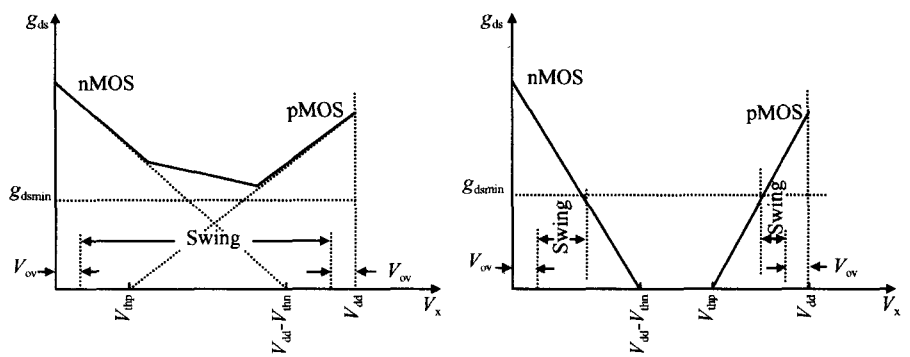

Fig. 2 CMOS switch conductance for supply voltage more than or less than $V_{thn} + V_{thp}$ respectively

2.3 Overview of the bootstrap technique

Due to the incompatibility of low-threshold-voltage devices with standard CMOS technology, circuit techniques are required to allow the sampling switch to operate at low supply voltages while achieving high-linearity. Usually the bootstrap technique is used. The main idea behind this technique is to boost the gate voltage to $V_{dd} + V_{in}$[4~6]. The conceptual representation of a bootstrapped switch is illustrated in Fig. 3. It functions as follows. During phase ϕ_1, C is charged to V_{DD} and M1 is off, while during phase ϕ_2, the precharged capacitor C is connected between the gate and the source of M1. The V_{gs} of M1 stays constant and equal to V_{DD}, independent of the in-

put signal level. Thus a rail-to-rail input range is allowed.

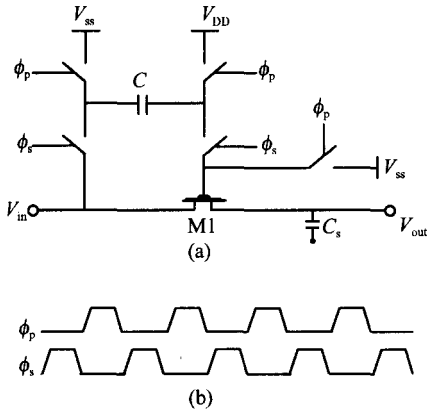

Fig. 3 (a) Simplified bootstrapped switch[5,6]; (b) Its timing diagram

The on-resistance of M1 can be written as

$$R_{on} = \frac{1}{\mu_n C_{ox} (\frac{W}{L}) (V_{dd} - V_{thn})} \quad (3)$$

In this way, a sampling switch with a constant on-resistance is established, with the assumption that V_{thn} stays fixed. However, V_{thn} varies with V_{bs}, as shown in Fig. 6(a). Thus the dynamic range of the sampling switch is still limited. New techniques are needed to respond to the increasing demand for high resolution ADCs.

3 Proposed sampling switch

The main idea of the proposed technique is to boost the gate voltage of the sampling transistor to a particular level above $V_{in} + V_{th}$, thus a rail-to-rail input range is achieved. At the same time, the nonlinearity due to both gate-source voltage variation and threshold voltage variation is eliminated.

Figure 4 shows a conceptual representation of our sampling circuit. The battery voltage at the output of the op-amp is used to adjust the output common mode of the op-amp. It is implemented with the same method as in Section 2.3. During phase ϕ_s, the sampling transistor switches on, and the gates of M1 and M2 are connected ($V_{g1} = V_{g2}$); during phase ϕ_p, the sampling switch is off while the dummy switch MD switches on to balance the load of the op-amp. It should be noticed that at the start of the sampling mode, M1 is

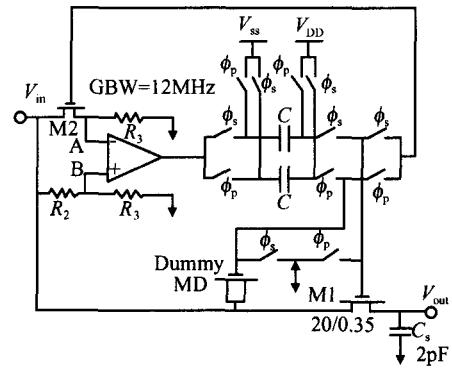

Fig. 4 Conceptual representation of the proposed switch

turned on before the dummy transistor MD is turned off so that the dummy switch provides the initial charge to turn on M1 quickly. In either phase, the op-amp is always in negative feedback with the same load, and it forces node A to be equal to node B, where

$$V_A = \frac{R_3}{R_{onM2} + R_3} V_{in} \quad (4)$$

and

$$V_B = \frac{R_3}{R_2 + R_3} V_{in} \quad (5)$$

Thus a constant resistance of transistor (M2) is achieved:

$$R_{onM2} = R_2 = \frac{1}{\mu_n C_{ox} (\frac{W}{L})_2 (V_{gs2} - V_{th2})} \quad (6)$$

It can be easily concluded from this equation that the gate voltage of M2 is

$$V_{g2} = V_{in} + V_{th2} + \frac{1}{\mu_n C_{ox} (\frac{W}{L})_2 R_2} \quad (7)$$

Therefore, the on-resistance of M1 can be written as

$$R_{onM1} = \frac{1}{\mu_n C_{ox} (\frac{W}{L})_1 (V_{th2} - V_{th1} + \frac{1}{\mu_n C_{ox} (\frac{W}{L})_2 R_2})} \quad (8)$$

As mentioned in Section 2.2, the threshold voltage depends not only on the source-bulk voltage, but also on the drain-source voltage[9,10]. An increase of the drain-source voltage will cause a reduction in the threshold voltage. Hence, we choose $R_2 \ll R_3$ to guarantee that M2 operates in the non-saturation region since the drain-source voltage, $V_{ds2} = V_{in} \times R_2 / (R_2 + R_3)$, is much smaller than $V_{gs2} - V_{th2}$. Although V_{dsM1} and V_{dsM2} are

not absolutely equal, they are very close. As shown in Fig. 6(b), the difference of the threshold voltage between M1 and M2 can be neglected. Thus, V_{th1} and V_{th2} in Eq. (8) cancel each other and R_{onM1} has no relationship with the input signal level. If we make $(W/L)_1 = (W/L)_2$, then from the above equations, it can be easily concluded that

$$R_{onM1} = R_{onM2} \tag{9}$$

Therefore, a constant on-resistance of the sampling transistor is obtained since M2 has a fixed resistance of R_2. Meanwhile, a rail-to-rail input is also achieved according to Eq. (7).

Note that the input swing of the proposed switch is limited to the op-amp input swing. To achieve a low supply voltage with rail-to-rail signal swings, op-amp input stages with rail-to-rail input common-mode ranges have been developed[11~14] in standard CMOS technology in the range of 1.2 ~3V. In our design, to obtain a constant g_m over the full common mode input range, a special biasing scheme[12] is adopted, as shown in Fig. 5. The whole op-amp was designed based on a standard 0.35μm CMOS process. The unit-gain bandwidth was simulated to be 12MHz with a 2pf capacitance load. The dc gain is 70dB and the power consumption for a 1.5V supply is about 146μW.

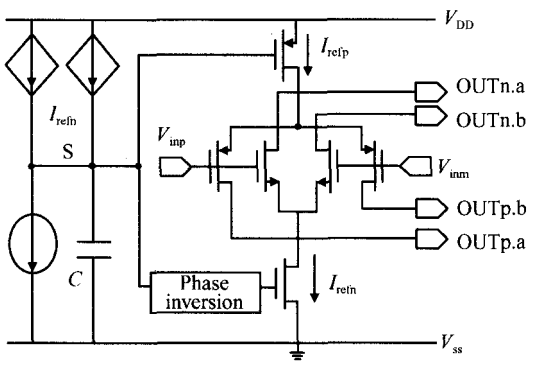

Fig. 5 Simplified schematic of rail-to-rail input stage[12]

In summary, the proposed technique is an effective approach to realize low voltage, high resolution switches. However, this is achieved at the cost of power consumed by the op-amp to ensure high open-loop gain and unit gain bandwidth.

4 Simulation results

The circuits are simulated in HSPICE using Chartered's 0.35μm CMOS BSIM3 models. The threshold voltages are 0.62 and 0.83V for nMOS and pMOS transistors, respectively. Poly-poly resistors are used in the implementation of resistors R_2 and R_3. For comparison with the conventional sampling switches, the equivalent parameters have been chosen for the proposed sampling switch. The supply voltage is 1.5V. The size of the sampling transistor is set to $W = 20\mu m$ and $L = 0.35\mu m$, and the value of the sampling capacitor, $C_s = 2pf$. Resistors (R_2 and R_3), replica and sampling transistors (M2 and M1), and capacitors including 1% random mismatches, are used for simulation.

The first simulation shows the variation of $V_{th1} - V_{th2}$ with respect to the input signal level, V_{in} (Fig. 6). The variation of $V_{th1} - V_{th2}$ is approximately zero in the proposed switch, though the variation of V_{th1} is the same as the bootstrapped switch. This verifies the effectiveness of the proposed technique in suppressing the difference between the threshold voltages of the sampling MOS and the replica MOS.

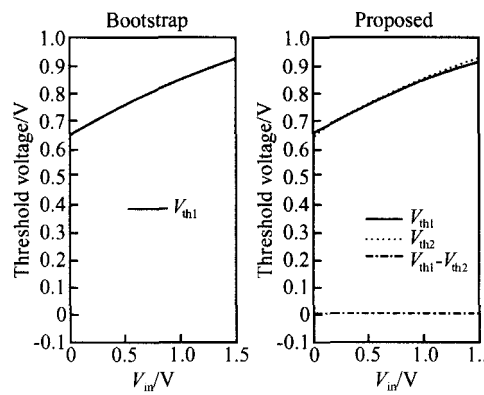

Fig. 6 Threshold voltage variation

The second simulation shows g_{ds} versus V_{in} for three switches (a regular CMOS, a bootstrapped switch from Ref. [6] and the proposed switch), targeting a g_{ds} of approximately 5mS. It can be seen from Fig. 7 that the conductance of the CMOS switch varies with respect to the input signal dramatically while the conductance variation of the proposed switch is less than 0.1mS. This is 90% less than that of the bootstrapped switch.

The third simulation shows an FFT plot of the bootstrapped switch and the proposed switch, respectively. A sinusoidal input signal of 0.2MHz, 1.2V peak-peak voltage is sampled at a frequency of 2MHz. The output spectral contents of the switches are shown in Figs. 8 and 9, respectively. It is

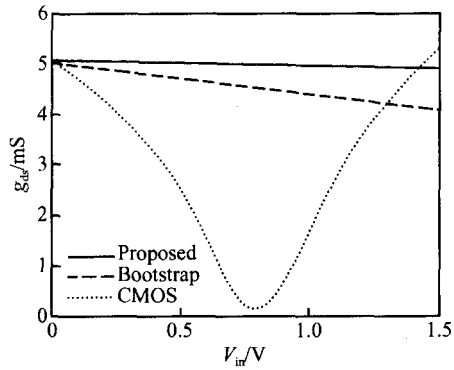

Fig. 7 On-conductance of CMOS switch, bootstrapped switch, and the proposed switch

obvious that both the odd and even harmonics produced by the proposed sampling switch are reduced. There is little variation of SFDR when the input signal is swept over the entire Nyquist bandwidth.

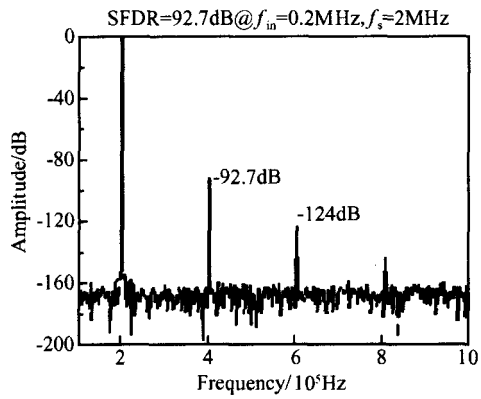

Fig. 8 Output spectrum for the bootstrapped switch

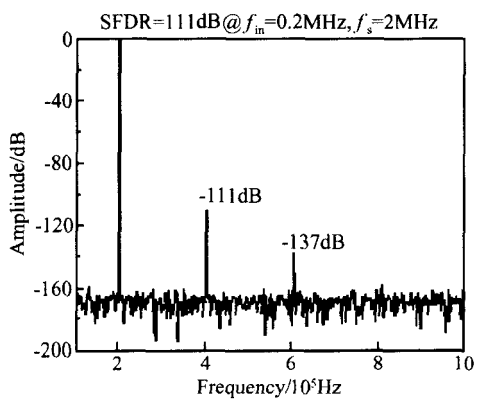

Fig. 9 Output spectrum for the proposed switch

The layout has been completed and submitted for fabrication. The proposed sampling switch has also been integrated into a whole ADC and found to be fully functional.

5 Conclusion

A novel technique is proposed to improve the linearity of a sampling switch. The nonlinearity due to variation of the threshold voltage is further eliminated by adopting a replica transistor with the same threshold voltage as the sampling transistor. This new scheme constitutes a robust circuit for providing a constant on-resistance switch and significantly high SFDR. The proposed technique can be used for low-voltage high resolution SC filters and ADCs.

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References

[1] Mastuzawa A. Low-voltage and low-power circuit design for mixed signal/digital systems in portable equipment. IEEE J Solid-State Circuits, 1994, 29(4): 470

[2] Crols J, Steyaert M. Switched-op-amp: an approach to realize full CMOS switched-capacitor circuits at very low supply voltages. IEEE J Solid-State Circuits, 1994, 29(8): 936

[3] Grilo J, Mac Robbie E, Halim R, et al. 1.8V, 94dB dynamic range Delta-Sigma modulator for voice applications. Proc Int Solid-State Circuits Conf, 1996: 232

[4] Brooks T L, Robertson D H, Kelly D F, et al. A cascaded sigma-delta pipeline A/D converter with 1.25MHz signal bandwidth and 89dB SNR. IEEE J Solid-State Circuits, 1997, 32(12): 1896

[5] Abo A M, Gray P R. A 1.5-V 10-bit 14.3-MS/s CMOS pipeline analog-to-digital converter. IEEE J Solid-State Circuits, 1999, 34(5): 599

[6] Dessouky M, Kaiser A. Input switch configuration suitable for rail-to-rail operation of switched-capacitor circuits. Electron Lett, 1999, 35(1): 8

[7] Steensgaard J. Bootstrapped low-voltage analog switches. Proc IEEE Int Symp Circuits Systems, 1999, 2: 29

[8] Wambaq P, Sansen W. Distortion analysis of analog integrated circuits. Boston, MA, USA: Kluwer Academic Publishers, 1998

[9] Sze S M. Physics of semiconductor devices. Wiley, 1981

[10] Troutman R R. VLSI limitations from drain-induced barrier lowering. IEEE Trans Electron Devices, 1979, 26: 461

[11] Duque-Cario J, Perez-Aloe R, Valverde J M. Biasing circuit for high input swing operational amplifiers. IEEE J Solid-State Circuits, 1995, 30: 156

[12] Peeters E, Steyaert M, Sansen W. A fully differential 1.5V low-power CMOS operational amplifier with a rail-to-rail current regulated constant-g_m input stage. Proc IEEE CICC, 1996: 75

[13] Ferri G, Sansen W. A rail-to-rail constant-gm low-voltage CMOS operational trans-conductance amplifier. IEEE J Solid-State Circuits, 1997, 32: 1563

[14] Lu G N, Sou G. 1.3V single-stage CMOS op-amp. Electron Lett, 1998, 34: 2073

一种适用于低电压模数转换器的新型采样开关

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摘要: 提出了一种适用于低电源电压的新型高线性度采样开关. 与传统低电压采样开关相比, 这种新型采样开关不仅消除了 MOS 开关由于栅源电压随输入信号变化所引入的非线性, 而且进一步消除了 MOS 开关由于阈值电压随输入信号变化引入的非线性. 这是通过采用一个与采样 MOS 开关具有相同阈值电压的"复制"开关得以实现的. 基于 Chartered 0.35μm 标准 CMOS 工艺, 文中设计了一个此类新型 MOS 采样开关, 在输入信号为 0.2MHz 正弦波, 峰峰值为 1.2V, 采样时钟频率为 2MHz 时, 无杂散动态范围达到 111dB, 比栅压自举开关提高了 18dB; 同时导通电阻的变化减小了 90%. 这种新型采样开关特别适用于低电压, 高精度模数转换器.

关键词: 采样开关; 非线性; 低电压; 模数转换器; 开关电容电路

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