Automatic IQ Phase Calibration Design in a 2.4GHz Direct Conversion Receiver *

Liu Ruifeng†, Li Yongming, Chen Hongyi, and Wang Zhihua

(*Institute of Microelectronics, Tsinghua University, Beijing* 100084, *China*)

Abstract: An automatic IQ phase calibration method implemented in a 2.4GHz direct conversion receiver is proposed. It uses a delay locked loop (DLL) with a proposed quadrature phase detector to greatly reduce the phase error. The receiver is fabricated in a 0.18μm CMOS process. Measurements show that the IQ phase error can be calibrated within 1°, which satisfies the system requirement.

Key words: direct conversion receiver; IQ phase calibration; CMOS process; quadrature phase detector
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1 Introduction

Direct conversion transceivers have become increasingly popular in recent years for their high integration ability. Direct conversion is the natural approach to translate a signal band from RF to baseband or from baseband to RF. The image problems in superheterodyne and low intermediate frequency (IF) conversion architectures are circumvented because the IF is zero. The LNA does not need to drive a 50Ω load because no image rejection filter is required[1]. All of these advantages make direct conversion transceivers easy to integrate on a chip with less power and area consumption.

However, there are still some drawbacks to the direct conversion architecture, such as IQ mismatch. IQ mismatch is mostly caused by imbalance between I and Q local oscillator (LO) signals. In heterodyne transceivers, the LO signals for IQ generation or summation are IF signals. The IQ imbalance can be made negligible. However, the LO signals in direct conversion transceivers are RF signals. Owing to the limitations of LO generation circuits and parasitics, the IQ performance cannot be very good, resulting in a reduced signal-to-noise ratio (SNR) and hence performance degradation[2]. In complex modulation schemes, such as 64-QAM, an IQ phase accuracy better than 1° and an amplitude accuracy better than 1% are required to guarantee that the inaccuracy does not limit the overall performance[2]. To reach such a goal, a good circuit and layout are usually insufficient. Calibration should be performed to guarantee good IQ performance.

In this paper, an automatic IQ phase calibration method implemented in a direct conversion receiver is presented. The receiver has been fabricated in a 0.18μm CMOS process. Measurements are also presented to verify the calibration effect.

2 Receiver architecture

The direct conversion receiver with automatic IQ phase calibration is shown in Fig. 1. A low noise amplifier (LNA) is placed as the first block of the receiver chain to amplify the small RF signal without adding much noise. The amplified RF signal is mixed down by two IQ mixers to generate IQ baseband signals. The variable gain amplifiers (VGAs) adjust the amplitude of the received signals. The channel filtering is done by the channel filters. Output buffers are designed to drive the off-chip impedances. A delay line (DL) is inserted into the Q side to generate an IQ phase error for measurement. The DL is composed of a resistor (R_{d2}), a ca-

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† Corresponding author. Email: pinnaxuan97@mails.tsinghua.edu.cn
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pacitor (C_{d2}), and a unity gain buffer. The unity gain buffer is used to drive the off-chip load.

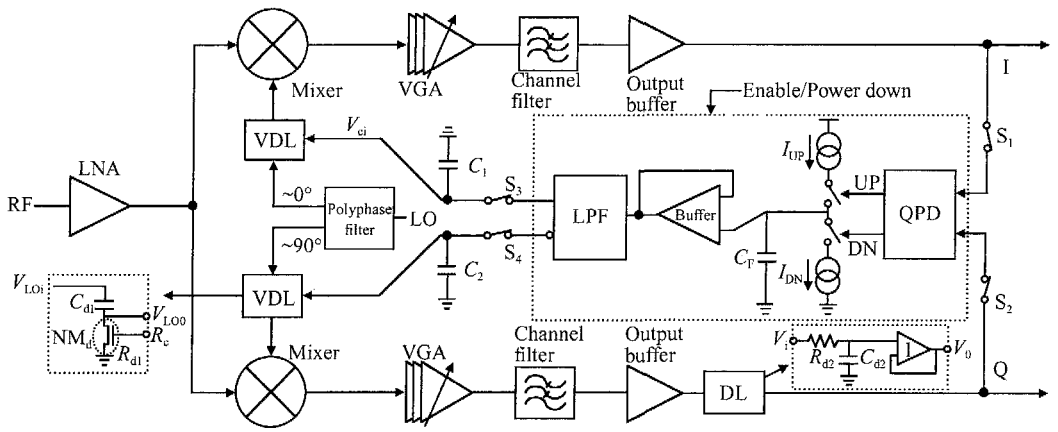

Fig. 1 Direct conversion receiver with automatic IQ phase calibration

The IQ LO signals are generated by a two-stage passive polyphase filter with an external input[3]. Perfect quadrature performance is only obtained at a certain frequency point, which is usually located at the center point of the operating band. IQ mismatch is thus unavoidable.

3 IQ phase calibration

3.1 Calibration loop design

The IQ phase calibration loop is based on a delay locked loop (DLL)[4] using a quadrature phase detector (QPD), as shown in Fig. 1. In the calibration mode, the switches ($S_1 \sim S_4$) are turned on. The quadrature phase error between I and Q is translated to a DC voltage through the QPD, charge pump, and loop capacitor (C_F). A unity-gain buffer is inserted between the loop capacitor and the low-pass filter (LPF) for isolation. The low-pass filtered DC voltages (V_{ci} and V_{cq}) adjust the phase shifts of the variable delay lines (V_{DL}) so that the phase difference between the I and Q signals approaches 90°. At the end of the calibration, all switches are turned off. The circuits in the dashed square are powered down. The proper control voltages are stored in the capacitors C_1 and C_2.

3.2 VDL design

The VDL is composed of a capacitor (C_{d1}) and an nMOS transistor (NM_d) as a variable resistor[5], as shown in Fig. 1. NM_d works in the linear region. Thus the variable resistor value (R_{d1}) is inversely proportional to the gate voltage of NM_d (V_c). The transfer function of the VDL is

$$\frac{V_{LOo}}{V_{LOi}} = \frac{j\omega_{LO} R_{d1} C_{d1}}{1 + j\omega_{LO} R_{d1} C_{d1}} \quad (1)$$

where ω_{LO} is the LO signal frequency.

Thus the phase difference between V_{LOo} and V_{LOi} is

$$Ph_{dif} = 90° - \tan^{-1}(\omega_{LO} R_{d1} C_{d1}) \quad (2)$$

Since R_{d1} is controlled by V_c, the phase difference between V_{LOo} and V_{LOi} can be adjusted by changing V_c. In this design, C_{d1} is set to be 0.6pF and the transistor NM_d size is 20μm/0.35μm.

3.3 QPD design

The QPD schematic is shown in Fig. 2(a). Amplifiers A_1, A_2, and A_3 convert sinusoidal inputs into square waves (I_p, Q_p, and Q_n). To minimize common mode effects on the duty cycle of the square waves, these amplifiers are designed with differential inputs. The UP signal is simply the product of I_p and Q_p, and the DN signal is the product of I_p and Q_n. Because the transition edge of AND gates AN_1 and AN_2 cannot be a step change, there exists a positive pulse overlap of the UP and DN signals. NAND gates N_1, N_2, and N_3 are used to eliminate this pulse overlap, so that the up and down current sources in the charge pump will not be turned on simultaneously. Inverters (I_1 and I_2) and transmission gates (T_1 and T_2) convert single-ended inputs to differential outputs to minimize the effects of switches on current sources in the charge

pump. A phase difference between the I and Q signals results in unequal positive pulse widths of the UP and DN signals[4].

Figure 2 (b) shows the simulation waveforms when the signal frequencies of I and Q are 10MHz and the quadrature phase error is about 5°. The positive pulse width of UP + is smaller than that of DN^+, resulting in a decrease in the charge pump output voltage.

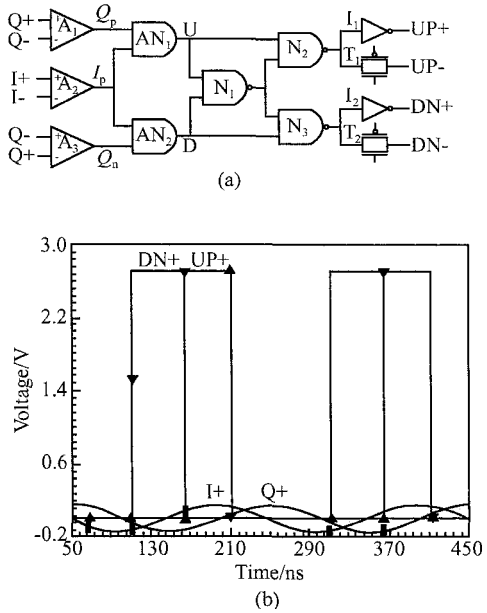

Fig. 2　Quadrature phase detector　(a) Schematic diagram; (b) Waveforms with 10MHz inputs

3.4 Charge pump design

Figure 3 gives a simplified schematic of the current charge pump. The sizes of transistors PM_c and NM_c are set to be 23. 16μm/ 3μm and 11. 4μm/ 3μm. The channel length of the transistor is chosen to be 3μm to make the ratio of transistor width to length less sensitive to process variance. A smaller size of 2μm/ 0. 35μm is chosen for all of the switching transistors to minimize capacitive coupling between UP (DN) and V_{CP}.

Because SW_{U1} and SW_{D1} are turned on alternately, V_U (V_D) does not follow V_{CP} when SW_{U1} (SW_{D1}) is off. This results in glitches in the charge current at the moment when SW_{U1} (or SW_{D1}) is turned on. SW_{U2}, SW_{D2}, and a unity gain buffer are used to reduce the glitches. For example, when SW_{D1} is turned on, SW_{U2} is on and SW_{U1} and SW_{D2} are off. Thus, V_U varies with V_S. Since V_S is almost identical to V_{CP}, V_U thus equivalently follows V_{CP}. Therefore, V_U does not experience a

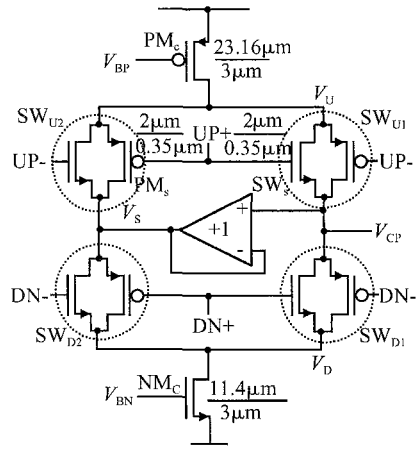

Fig. 3　Simplified schematic of the charge pump

step change when SW_{U1} is turned on. The glitches in the current through SW_{U1} are consequently reduced. Figure 4 shows that the current glitches are reduced from nearly 300 to 30μA.

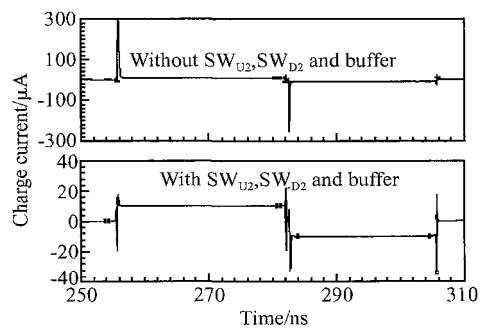

Fig. 4　Reduction of charge pump current glitches

3.5 Resolution analysis

In a real QPD circuit, there exists a width mismatch between the positive pulse widths (T_{UP} and T_{DN}) of the UP and DN signals when I and Q are exactly in quadrature. There is also a mismatch between I_{UP} and I_{DN}. For a phase error of $d\phi_{er}$ between I and Q, the voltage increment of V_{ci} or V_{cq} after n signal cycles is

$$dV_n = \frac{TI_0}{4C_F}\left(\delta + \varepsilon - \frac{-d\phi_{er} + d\phi_1 + \cdots + d\phi_{n-1}}{90^\circ}\right) \tag{3}$$

where δ is the mismatch between T_{UP} and T_{DN}, ε is the mismatch between I_{UP} and I_{DN}, T is the signal cycle of I and Q, I_0 is the ideal charge pump current, and $d\phi$ is the phase shift between I and Q caused by dV_i. If dV_n equals zero, the loop locks. Thus the residual phase error after calibration is

$$(-d\phi_{er} + d\phi_1 + \cdots + d\phi_{n-1}) = 90^\circ \times (\delta + \varepsilon) \tag{4}$$

Equation (4) shows that the residual phase error (namely calibration resolution) is directly proportional to the QPD and charge pump mismatches. Ideally, δ and ε are both zero, which means the calibration resolution is 0°. Careful design of the QPD and charge pump reduces $\delta+\varepsilon$ to be about 0.4% on average, resulting in a 0.36° residual phase error[4].

4 Simulation results

The receiver with the calibration loop is simulated using Cadence Spectre RF with a 0.18μm CMOS process and a 2.7V supply voltage. The RF input signal and the LO signal are set at 2.41GHz and 2.4GHz, respectively. Thus the baseband signal for calibration is 10MHz. The loop filter C_F is set at 3.6pF. The resistor R_{d2} and capacitor C_{d2} in the DL are set at 1.4kΩ and 1pF to generate a 5° quadrature phase error between I and Q. Figure 5 plots the waveforms of V_{ci} and V_{cq} during the calibration process. Figure 6 plots the waveforms of I and Q before and after calibration. The initial 5° phase error is reduced to only 0.18°.

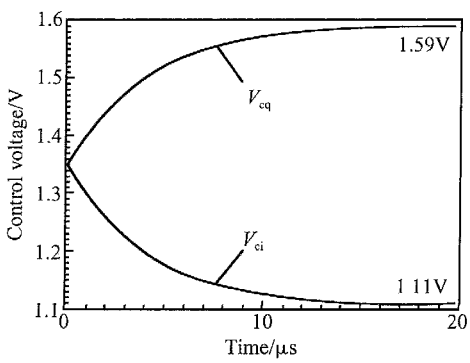

Fig. 5 V_{ci} and V_{cq} lock-in process

5 Layout design and measured results

This design has been fabricated in a 0.18μm CMOS process. The chip was bonded in a 24-pin QUAD package. A photo of the chip is shown in Fig. 7, including the receiver and some other test circuits. The receiver size is about 2.3mm^2.

5.1 Layout design

The receiver layout is made as symmetrical as possible to improve its quadrature performance, as shown in Fig. 7. The IQ phase detection blocks, including the QPD, charge pump, loop filter, buffer, and LPF, are placed between the I and Q baseband paths to maintain the layout symmetry. The two VDLs are also placed symmetrically on the LO signal paths.

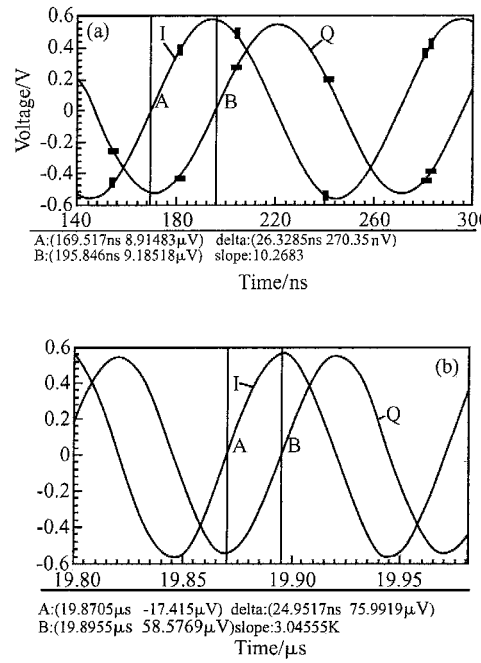

Fig. 6 Waveforms of I and Q (a) Before calibration; (b) After calibration

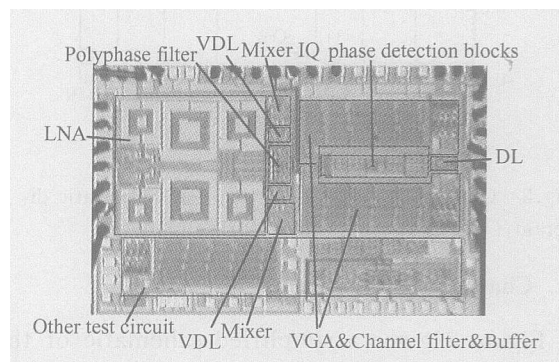

Fig. 7 Chip photo

5.2 Measured results

The whole calibration circuit consumes about 1.8mA in calibration mode and less than 2nA in power-down mode from a 2.7V supply. The RF signal is 2.41GHz and the LO signal is 2.4GHz.

The IQ signals are measured using an Agilent 54622D 100MHz mixed signal oscilloscope. Figure 8(a) shows that the time difference between I and Q before calibration is about 28ns. Thus the IQ phase error is 28/100 ×360°- 90°= 10.8°. In addition to the 5° phase error of the DL, the receiver

contributes an extra 5. 8 °phase error. Figure 8(b) shows that the time difference after calibration is about 25. 2ns. The IQ phase error is thus 25. 2/100 ×360 ° - 90 ° = 0. 72 °. The measured results show that the calibrated IQ phase error is smaller than the requirement of 1 °.

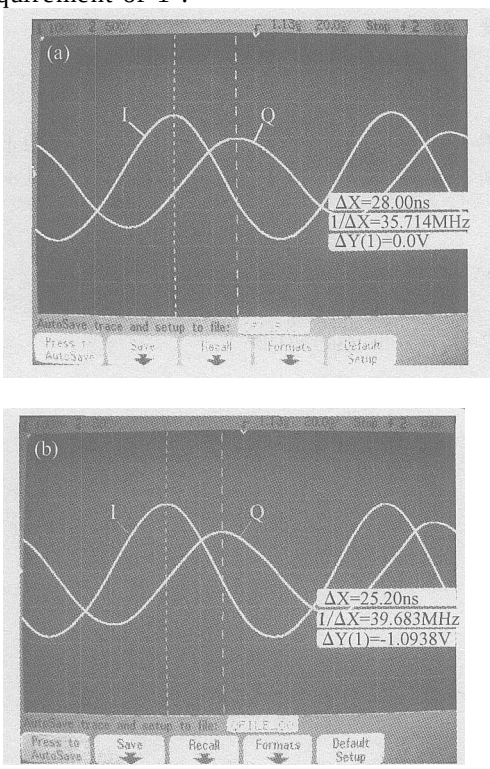

Fig. 8　Measured I/Q waveforms　(a) Before calibration; (b) After calibration

The measured performance departs somewhat from the simulation result. The possible reason is that the QPD and charge pump performances are not as good as in the simulation. Figure 8 also shows that the IQ amplitude error is a bit large, which needs to be eliminated in future design.

6　Performance comparison

The receiver IQ phase calibration methods can be classified into categories: (1) digital calibration implemented in the baseband DSP chip[6,7]; (2) mixed method of analog and digital calibration with the help of the DSP chip[8]; (3) calibration integrated in the transceiver chip[9,10]. Calibration methods of (1) and (2) rely on the baseband DSP chips, which increases the complexity of the baseband DSP chips and lowers the compatibility between the transceiver chips and the baseband DSP chips. The selection range of DSP chips for transceiver providers is also reduced. Thus method (3) is preferred for both transceiver and baseband DSP chip providers. The IQ phase calibration method proposed in this design is classified into method (3).

The calibrated IQ phase errors are 0. 3 °in Ref. [9] and 1 °in Ref. [10]. Thus the measured performance of this design is between the results of Refs. [9] and [10], all satisfying the system requirement of 1 °.

7　Conclusions

An automatic IQ phase calibration method implemented in a 2. 4GHz direct conversion receiver is presented. The calibration loop is based on a delay locked loop using a proposed quadrature phase detector (QPD). The QPD schematic and the loop resolution are given and analyzed. The receiver has been fabricated in a 0. 18μm CMOS process. Measurements show that the IQ phase error after calibration is less than 1 °, which satisfies the system requirements.

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2.4GHz 零中频接收机中正交相位的自校准设计*

刘瑞峰† 李永明 陈弘毅 王志华

(清华大学微电子学研究所, 北京 100084)

摘要: 提出了实现在一个 2.4GHz 零中频接收机中的一种正交相位自校准方法. 这种方法基于一个采用提出的正交相位检测器的延迟锁定环路来大大减小正交相位误差. 该接收机采用 0.18μm CMOS 工艺实现. 测试结果显示正交相位误差可以被校准到 1°以内, 满足了系统的要求.

关键词: 零中频接收机; 正交相位校准; CMOS 工艺; 正交相位检测器
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†通信作者. Email: pinnaxuan97@mails.tsinghua.edu.cn
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