2D Threshold-Voltage Model for High-k Gate-Dielectric MOSFETs*

Ji Feng[1], Xu Jingping[1,†], Lai P T[2], Chen Weibing[1], and Li Yanping[1]

(1 *Department of Electronic Science & Technology, Huazhong University of Science and Technology, Wuhan 430074, China*)
(2 *Department of Electrical & Electronic Engineering, University of Hong Kong, Hong Kong, China*)

Abstract: New boundary conditions and a 2D potential distribution along the channel of a high-k gate-dielectric MOSFET, including both the gate dielectric material region and the depletion region, are given. Based on this distribution, a 2D threshold-voltage model with the fringing-field and short-channel effects is developed for a high-k gate-dielectric MOSFET. The model agrees well with experimental data and a quasi 2D model, and is even more accurate than the quasi 2D model at higher drain voltages. Factors affecting the threshold behavior of the high-k gate-dielectric MOSFET are discussed in detail.

Key words: high-k gate dielectric; MOSFET; threshold voltage; fringing field; short-channel effect
PACC: 7340Q; 1240Q
CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2006)10-1725-07

1 Introduction

The increasing need for smaller and more powerful microprocessors has created the impetus to reduce feature size[1]. It is well known that the channel length, gate-oxide thickness, and depletion width must be simultaneously shrunk to maintain proper device characteristics[2]. However, a thinner gate oxide introduces an exponential increase of the gate leakage current. To decrease the gate leakage current and standby power, high-dielectric-constant (high-k) materials have been explored to replace the conventional SiO_2 with gate dielectric[3]. Recently, the effects of high-k gate dielectric on the electrical characteristics of deep sub-micrometer MOSFETs have been widely investigated and discussed[4~7]. The use of high-k gate material results in a dielectric thickness comparable to the device gate length, thus increasing fringing fields from the gate to the source/drain regions and compromising short-channel performance[8]. Indeed, the threshold voltage for high-k gate-dielectric MOSFETs is severely affected by the fringing-field effect and short-channel effect (SCE), which make the classical threshold-voltage model of MOSFETs not applicable. Therefore, an accurate threshold-voltage model for high-k gate-dielectric MOSFETs must be developed. Liu *et al*.[9] gave a quasi 2D threshold-voltage model by assuming constant boundary conditions. When the drain voltage (V_{ds}) is small, the quasi 2D model can be used to calculate the threshold voltage of a device. But a larger error occurs for larger V_{ds}. Moreover, the threshold voltage of high-k gate-dielectric MOSFETs is closely linked to V_{ds} and the fringing fields. Therefore, this work concentrates on the development of a threshold-voltage model to include the effects of fringing fields and V_{ds} by revising the boundary conditions. Surface potential distribution along the channel of the MOSFET is obtained by using the variation method, and the effects of high-k gate dielectrics on the threshold voltage are discussed in detail over a wide range of dielectric constants.

2 Model description

The structure of an nMOSFET is shown in Fig. 1. For simplicity, it is assumed that the accumulation effect in the overlay regions of the gate and source/drain is negligible for small V_g around the threshold voltage and for high doping concentration of the source/drain region (above 10^{19} cm^{-3}). Thus, the 2D Poisson equation is solved only in the channel region and gate dielectric re-

* Project supported by the National Natural Science Foundation of China (No. 60376019)
† Corresponding author. Email: jpxu@mail.hust.edu.cn
Received 10 March 2006, revised manuscript received 24 May 2006

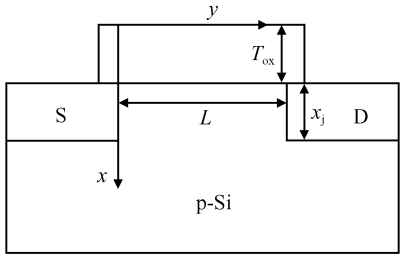

Fig. 1 Schematic diagram of nMOSFET structure

gion above the channel. By neglecting mobile-carrier charge in the channel depletion region, the 2D Poisson equation and boundary conditions can be written as

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=\begin{cases}0, & 0\leqslant x\leqslant T_{ox},0\leqslant y\leqslant L\\ \dfrac{qN_{dep}}{\varepsilon}, & T_{ox}\leqslant x\leqslant d,0\leqslant y\leqslant L\end{cases} \tag{1}$$

$$\varphi(0,y)=V_g-V_{fb} \tag{2}$$

$$\varphi_x(x,y)\mid_{x=d}=0 \tag{3}$$

$$\varphi(x,0)=g_s(x) \tag{4}$$

$$\varphi(x,L)=g_d(x) \tag{5}$$

$$\kappa\frac{\partial\varphi(x,y)}{\partial x}\bigg|_{x=T_{ox}}=\varepsilon\frac{\partial\varphi(x,y)}{\partial x}\bigg|_{x=T_{ox}} \tag{6}$$

$$d=T_{ox}+x_d \tag{7}$$

where N_{dep} is the doping concentration of the substrate, ε and k are the dielectric constants of Si and the gate dielectric, respectively, V_g is the gate voltage, V_{fb} is the flat-band voltage, $g_s(x)$ and $g_d(x)$ are the boundary potentials at the source and drain, respectively, x_d is the width of the depletion region in the substrate, and T_{ox} and L are the thicknesses of the gate dielectric and channel length, respectively. To consider the effects of fringing fields on the threshold voltage, $\varphi(x,y)$ can be considered as a sum of three potentials by setting different boundary conditions as

$$\varphi(x,y)=V(x,y)+U_1(x,y)+U_2(x,y) \tag{8}$$

where $V(x,y)$ is the potential distribution without considering the fringing fields from the source/drain ends, and $U_1(x,y)$ and $U_2(x,y)$ are the potential distributions caused by the fringing fields of the source and drain, respectively. The boundary conditions for $V(x,y)$, $U_1(x,y)$, and $U_2(x,y)$ can be respectively written as

$$\begin{cases}\dfrac{\partial^2V(x,y)}{\partial x^2}+\dfrac{\partial^2V(x,y)}{\partial y^2}=\begin{cases}0, & 0\leqslant x\leqslant T_{ox},0\leqslant y\leqslant L\\ qN_{dep}/\varepsilon, & T_{ox}\leqslant x\leqslant d,0\leqslant y\leqslant L\end{cases}\\ V(0,y)=V_g-V_{fb}\\ V_x(x,y)\mid_{x=d}=0\\ V(x,0)=0\\ V(x,L)=0\\ \kappa\dfrac{\partial V(x,y)}{\partial x}\bigg|_{x=T_{ox}}=\varepsilon\dfrac{\partial V(x,y)}{\partial x}\bigg|_{x=T_{ox}}\end{cases} \tag{9}$$

$$\begin{cases}\dfrac{\partial^2U_1(x,y)}{\partial x^2}+\dfrac{\partial^2U_1(x,y)}{\partial y^2}=0\\ U_1(x,0)=g_s(x)\\ U_1(x,L)=0\end{cases} \tag{10}$$

and

$$\begin{cases}\dfrac{\partial^2U_2(x,y)}{\partial x^2}+\dfrac{\partial^2U_2(x,y)}{\partial y^2}=0\\ U_2(x,0)=0\\ U_2(x,L)=g_d(x)\end{cases} \tag{11}$$

Thus, the effects of the fringing fields from the source/drain ends on the potential distribution are considered in Eqs. (10) and (11), respectively. By using the variation method[9~11] to solve the Poisson equation (9), the solution has the form

$$V(x,y)=V_0(x)-V_0(x)\frac{\sinh[(L-y)/l]}{\sinh(L/l)}-V_0(x)\frac{\sinh(y/l)}{\sinh(L/l)} \tag{12}$$

where $V_0(x)$ is the 1D solution for long-channel MOSFETs, and l is a characteristic length ($l=[(5\kappa T_{ox}/6+A+\varepsilon x_d)/(C_{ox}+5C_d/6)]^{1/2}$, $C_d=\varepsilon/x_d$, $A=2(T_{ox}/x_d)+(4/3)(T_{ox}/x_d)^2$).

The solution to Eq. (10) can be found using the same variation method.

$$U_1(x,y)=g_s(x)\frac{\sinh(\dfrac{L-y}{l_1})}{\sinh(\dfrac{L}{l_1})} \tag{13}$$

Here l_1 is the characteristic length for $U_1(x,y)$, and it is defined as

$$l_1=\left[\frac{\displaystyle\int_0^{T_{ox}}kg_s^2(x)\mathrm{d}x+\int_{T_{ox}}^{T_{ox}+x_j}\varepsilon g_s^2(x)\mathrm{d}x+\int_{T_{ox}+x_j}^{T_{ox}+x_j+x_{ds}}\varepsilon g_s^2(x)\mathrm{d}x}{\displaystyle\int_0^{T_{ox}}k\left(\frac{\partial g_s(x)}{\partial x}\right)^2\mathrm{d}x+\int_{T_{ox}}^{T_{ox}+x_j}\varepsilon\left(\frac{\partial g_s(x)}{\partial x}\right)^2\mathrm{d}x+\int_{T_{ox}+x_j}^{T_{ox}+x_j+x_{ds}}\varepsilon\left(\frac{\partial g_s(x)}{\partial x}\right)^2\mathrm{d}x}\right]^{\frac{1}{2}} \tag{14}$$

where $g_s(x)$ is the boundary condition of the source end. Figure 2 shows the different components of capacitance. Here C_{ox} is the oxide capacitance, C_{si} is the silicon body capacitance, C_{ov} is the gate to S/D overlap capacitance, and C_{of} and C_{if} are the outer and inner fringe capacitances respectively. The distribution of $g_s(x)(0<x<T_{ox})$ in the gate dielectric is mainly determined by C_{ov}. C_{ov} decreases linearly with scaling[12], resulting in the linear distribution of $g_s(x)(0<x<T_{ox})$. The layer between the source and the substrate is the depletion region. Thus, $g_s(x)$ can be written as

$$g_s(x)=\begin{cases}(V_g-V_{fb})-\dfrac{(V_g-V_{fb})-V_{bi}}{T_{ox}}x, \\ \qquad 0\leqslant x\leqslant T_{ox}\\ V_{bi}, \quad T_{ox}<x<T_{ox}+x_j\\ V_{bi}\left[1-\dfrac{x-(T_{ox}+x_j)}{x_{ds}}\right]^2, \\ \qquad T_{ox}+x_j\leqslant x\leqslant T_{ox}+x_{ds}+x_j\end{cases} \tag{15}$$

where x_{ds} is the depletion width of the source/substrate junction, x_j is the junction depth of the source/drain region, and V_{bi} is the built-in potential of the source/substrate and drain/substrate junctions. It can be seen from Eqs. (14) and (15) that l_1 is a function of the potential at the source end, gate voltage, thickness and dielectric constant of the gate dielectric, reflecting the effects of fringing fields from the source on the threshold voltage.

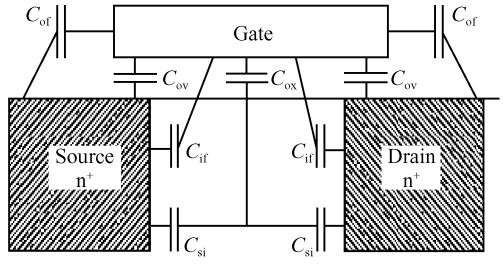

Fig. 2　Schematic of the different capacitance components

Equation (11) for $U_2(x,y)$ can be solved similarly, and a corresponding characteristic length l_2 can be defined as

$$l_2=\left[\frac{\int_0^{T_{ox}}kg_d^2(x)\mathrm{d}x+\int_{T_{ox}}^{T_{ox}+x_j}\varepsilon g_d^2(x)\mathrm{d}x+\int_{T_{ox}+x_j}^{T_{ox}+x_j+x_{dd}}\varepsilon g_d^2(x)\mathrm{d}x}{\int_0^{T_{ox}}k\left(\frac{\partial g_d(x)}{\partial x}\right)^2\mathrm{d}x+\int_{T_{ox}}^{T_{ox}+x_j}\varepsilon\left(\frac{\partial g_d(x)}{\partial x}\right)^2\mathrm{d}x+\int_{T_{ox}+x_j}^{T_{ox}+x_j+x_{dd}}\varepsilon\left(\frac{\partial g_d(x)}{\partial x}\right)^2\mathrm{d}x}\right]^{\frac{1}{2}} \tag{16}$$

$$g_d(x)=\begin{cases}(V_g-V_{fb})-\dfrac{(V_g-V_{fb})-(V_{bi}+V_{ds})}{T_{ox}}x, & 0\leqslant x\leqslant T_{ox}\\ V_{bi}+V_{ds}, & T_{ox}<x<T_{ox}+x_j\\ (V_{bi}+V_{ds})\left[1-\dfrac{x-(T_{ox}+x_j)}{x_{dd}}\right]^2, & T_{ox}+x_j\leqslant x\leqslant T_{ox}+x_{dd}+x_j\end{cases} \tag{17}$$

where x_{dd} is the depletion width of the drain/substrate junction. Finally, the solution to Eq. (1) can be found by Eq. (8)

$$\varphi(x,y)=V_0(x)-V_0(x)\frac{\sinh[(L-y)/l]}{\sinh(L/l)}-V_0(x)\frac{\sinh(y/l)}{\sinh(L/l)}+g_s(x)\frac{\sinh[(L-y)/l_1]}{\sinh(L/l_1)}+g_d(x)\frac{\sinh(y/l_2)}{\sinh(L/l_2)} \tag{18}$$

Equation (18) is the 2D potential distribution from source to drain, including the gate dielectric region after considering the effects of fringing fields from the source/drain ends. Based on Eq. (18), the location y_0 of the minimum surface potential ($\varphi_{sf\,min}$) in the channel can be determined by $\left.\dfrac{\mathrm{d}\varphi(x,y)}{\mathrm{d}y}\right|_{x=T_{ox}}=0$, and is found to be

$$y_0=\frac{L}{2}-\frac{l}{2}\ln\frac{g_d(T_{ox})/l_2-V_0(T_{ox})/l}{g_s(T_{ox})/l_1-V_0(T_{ox})/l} \tag{19}$$

Substituting Eq. (19) into Eq. (18) to get $\varphi_{sf\,min}$ and setting $\varphi_{sf\,min}=2\phi_f$ ($\phi_f=\dfrac{k_0T}{q}\ln\dfrac{N_{dep}}{n_i}$ is the Fermi potential of the substrate), the corresponding V_g is defined as the threshold voltage V_{th}:

$$V_{th}=\frac{C_{ox}+2C_d}{C_{ox}}\times\frac{2\phi_f-g_s(T_{ox})\dfrac{\sinh[(L-y_0)/l_1]}{\sinh(L/l_1)}-g_d(T_{ox})\dfrac{\sinh(y_0/l_2)}{\sinh(L/l_2)}}{1-\dfrac{\sinh[(L-y_0)/l]}{\sinh(L/l)}-\dfrac{\sinh(y_0/l)}{\sinh(L/l)}} \tag{20}$$

The threshold-voltage roll-off can be presented as

$$\Delta V_{th} = V_{th} - V_{tho} \quad (21)$$

where V_{tho} is the classical threshold voltage of a long-channel MOSFET, and $C_{ox} = \kappa / T_{ox}$ is the gate-oxide capacitance per unit area.

3 Results and discussion

From Eq. (20), it can be seen that the threshold voltage is related to l_1 and l_2, which depend on the values of $g_s(x)$, $g_d(x)$, V_{ds}, V_g, and k, i.e. the effects of the fringing fields and SCE are included in the proposed threshold-voltage model. As a result, the simulated threshold voltages agree well with the experimental V_{th} extracted with different methods for a MOSFET with SiO_2 as the gate dielectric[13], as shown in Fig. 3, confirming the validity of the model.

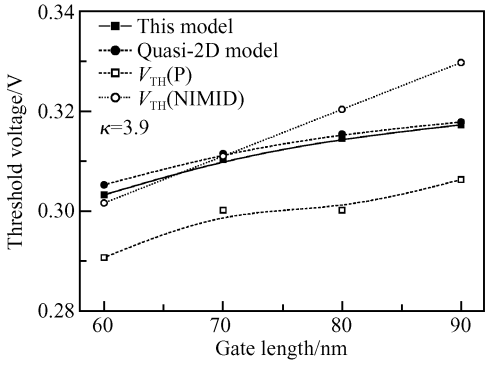

Fig. 3 Comparison between the simulated and experimental threshold voltages

For small channel lengths (e. g. 60nm), the simulated result is closer to the experimental data than that of the quasi-2D model. In Fig. 3, V_{TH}(P) and V_{TH}(NIMID) represent the threshold voltages extracted by Tikhonov's regularization theory[13], which can suppress the instability of the transconductance change method, and the normalized mutual integral difference method[14], which is sensitive to channel length variation. Furthermore, a comparison between the model and the quasi 2D model[9] is made for high-k gate dielectric MOSFETs, as shown in Fig. 4.

For small V_{ds}, good agreement between the two models can be obtained. However, for larger V_{ds}, e.g. $V_{ds} = 1$V, a larger difference between the two models occurs for larger k values, e.g. $k > 40$, which is caused by the different boundary conditions of the two models. The boundary conditions

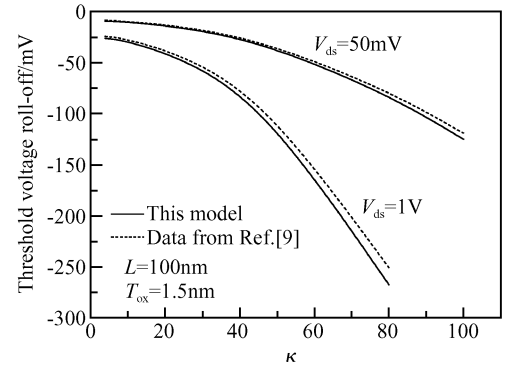

Fig. 4 Threshold voltage roll-off versus gate dielectric constant

in Ref. [9] are constant values from the classical theory: $\varphi(x, 0) = V_s$ and $\varphi(x, L) = V_d$ (V_s and V_d are the potentials of the source and drain, respectively). On the other hand, the boundary conditions in Eqs. (15) and (17) are functions of V_d, V_g, and k, with corresponding $\varphi(x, y)$ composed of three potentials as shown in Eq. (8). As a result, larger k results in a higher fringing field, giving rise to a reduction of V_{th}. Therefore, the threshold-voltage model presented by Eq. (20) is more accurate than that in Ref. [9] over a wide range of k and V_{ds}.

Figure 5 depicts the surface-potential distribution along the channel calculated by Eq. (18) at different V_{ds} and k for a given gate-dielectric thickness and V_g. Obviously, the larger k value,

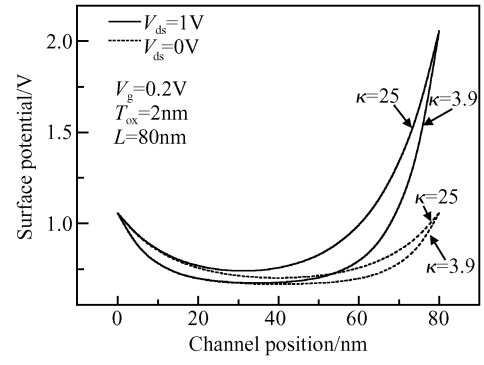

Fig. 5 Surface-potential distribution for different κ and V_{ds} $x = 0$nm and 80nm are the source and drain ends of the channel, respectively.

the higher potential in the channel, which is mainly due to influences of $U_1(x, y)$ and $U_2(x, y)$, shown in Fig. 6, indicating the enhanced fringing-field effects for increased k values. When V_{ds} increases, the surface potential is almost constant near the source but is greatly increased near the

drain, indicating a combined effect of the fringing fields and SCE (the larger V_{ds}, the more serious SCE and the higher fringing field), which gives a lower threshold voltage. Therefore, the influence of the fringing fields associated with the V_{ds} and k values on the threshold voltage must be considered for high-k gate-dielectric MOSFETs.

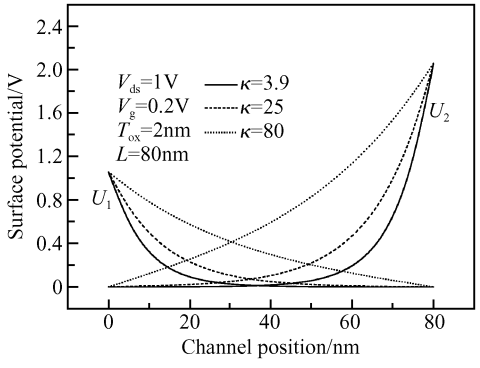

Fig. 6　Distribution of surface potential $U_1(x, y)$ and $U_2(x, y)$ for different k values

Figure 7 shows the effects of the gate dielectric constant k and channel length L on the threshold-voltage roll-off. As k increases, the threshold voltage begins to decrease at larger channel lengths, due to the enhanced fringing-field effects. In other words, the smaller the channel length, the larger is the influence of the fringing fields on the threshold voltage, and thus the weaker is the control of the gate voltage over the channel potential, especially for larger k values. As shown in Fig. 7, when the channel is long enough, e. g. $L > 200$nm, and the effect of the fringing fields on the threshold voltage can be ignored even for $\kappa=30$. Therefore, the fringing-field

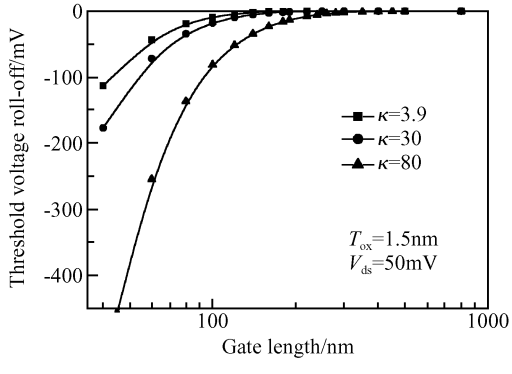

Fig. 7　Dependence of the threshold voltage roll-off on channel length with different gate dielectric constants

effects are important for accurately calculating the threshold voltage of a small MOSFET with high-k material as the gate dielectric.

Figure 8 shows the variation of the threshold-voltage roll-off with V_{ds}. For a given k value of the gate dielectric, the threshold voltage decreases as V_{ds} increases because the drain voltage can lower the surface potential barrier near the source. The higher the dielectric constant, the larger is

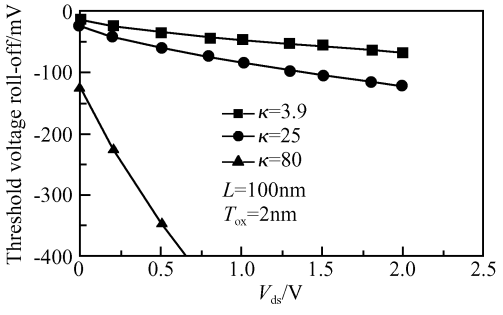

Fig. 8　Dependence of the threshold voltage roll-off on V_{ds}

the effect of V_{ds} on the threshold voltage, meaning that even a small V_{ds} (e. g. $V_{ds} = 0.5$V) can lead to a large threshold-voltage reduction ($|\Delta V_{th}| > 300$mV for $k = 80$), due to greatly enhanced fringing-field effects at the drain end as mentioned above. In fact, the threshold voltage is strongly affected by the characteristic lengths (l_1 and l_2), which are closely related to the k value, as shown in Eqs. (20), (14), and (16). The changes of the characteristic lengths with the k value are shown in Fig. 9. When $\kappa > 25$, influence of k on the characteristic lengths becomes stronger, resulting in higher surface potential through the fringing-field effects. Therefore, the gate dielectric material for future-generation MOSFETs

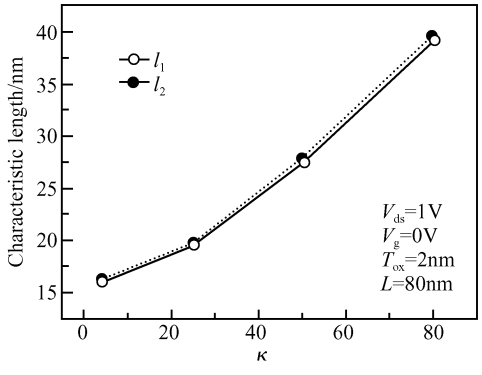

Fig. 9　Changes of the characteristic lengths as a function of k

needs to be carefully selected according to the requirements of gate leakage current and V_{th} roll-off (using the high-k gate dielectric material with a suitable k value so that not only the gate leakage current can effectively be suppressed, but the V_{th} roll-off can also be minimized), in order to suppress the fringing-field effects, especially when the effective oxide thickness is only a few nanometers.

In summary, when a high-k material replaces SiO_2 as gate dielectric, the fringing-field effect and SCE are severely enhanced. Consequently, these effects are the dominant factors in causing the threshold-voltage roll-off of deep sub-micrometer MOSFETs.

4 Summary

The 2D Poisson equation describing both the gate-dielectric region and the depletion region is solved by expressing the surface potential as a sum of three potentials to include the influences of the fringing-field effect and SCE on the threshold voltage. As a result, an accurate threshold-voltage model for high-k gate-dielectric MOSFETs is developed. To get the threshold voltage of a high k MOSFET, new boundary conditions from the depletion region to the gate dielectric material are proposed. Accordingly, the three potentials are solved in both regions. By means of this model, the effects of the fringing field and SCE on the threshold voltage are discussed in detail over a wide range of dielectric constants and V_{ds}. As compared with MOSFETs with SiO_2 as the gate dielectric, the fringing-field effect and SCE in the high-k gate-dielectric counterpart are greatly enhanced. The simulated threshold voltage roll-off using the model exhibits good agreement with experimental data and other models, with even better accuracy than the quasi 2D model[9] for higher drain voltages, indicating that the model can be used to accurately describe the threshold behavior of deep sub-micrometer MOSFETs with high-k material as gate dielectric. This analytical model is suitable for device design and circuit simulation.

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高 *k* 栅介质 MOSFETs 的二维阈值电压模型*

季　峰[1]　徐静平[1,†]　Lai P T[2]　陈卫兵[1]　李艳萍[1]

（1 华中科技大学电子科学与技术系，武汉　430074）
（2 香港大学电机与电子工程系，香港）

摘要：给出包括栅电介质与耗尽层区域的边界条件和二维沟道电势分布.根据这个电势分布,得出高 *k* 栅介质 MOSFET 的阈值电压模型,模型中考虑短沟道效应和高 *k* 栅介质的边缘场效应.模型模拟结果和实验结果能够很好地符合.通过和一个准二维模型的结果相比较,表明该模型更准确.另外,还详细讨论了影响高 *k* 栅电介质 MOSFET 阈值电压的一些因素.

关键词：高 *k* 栅介质；MOSFET；阈值电压；边缘场；短沟效应
PACC：7340Q；1240Q
中图分类号：TN386　　**文献标识码**：A　　**文章编号**：0253-4177(2006)10-1725-07

* 国家自然科学基金资助项目(批准号:60376019)
† 通信作者.Email:jpxu@mail.hust.edu.cn
2006-03-10 收到,2006-05-24 定稿