A General Method in the Synthesis of Ternary Double Pass-Transistor Circuits *

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Abstract: A general method for designing ternary circuits using double pass-transistor logic is investigated. The logical relation of each MOS transistor is formulated by using the transmission operation in order to make effective and practical use of the circuits. A way to generate ternary complementary and dual circuits by applying the complementarity and duality principles is presented. This new static ternary double pass-transistor logic scheme has some favorable properties: the use of standard CMOS process without any modification of the thresholds, a perfectly symmetrical structure, a full logic swing, the maximum possible noise margins, a less complex structure, and no static power consumption. HSPICE simulations using TSMC 0.25μm CMOS technology and a 3V power supply demonstrate the effectiveness of the proposed design.

Key words: switching circuit theory; multiple-valued logic; logic synthesis; double pass-transistor logic
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1 Introduction

The need for multiple-valued logic (MVL) has been pointed out by researchers. Implementation of MVL using CMOS technology follows two major lines: current-mode and voltage-mode circuits. Although the current-mode approach has some benefits, it also has the obvious disadvantage of high power consumption due to the constant current flow. Voltage-mode MVL circuits have the advantage of low power consumption, but at the expense of complex fabrication and high cost[1~5]. Ternary logic has received more attention than the other types of MVL because of its low interconnection cost estimation and simple electronic circuit implementation method[6]. Several static[1,3,4] and dynamic[7~9] voltage-mode CMOS circuits for ternary logic have been proposed in recent years, but possible circuit realizations are still under investigation because the many schemes proposed are, for various reasons, far from optimum[9]. Static MVL circuit schemes require a complex process to obtain both depletion and enhancement devices[1~3] or multi-threshold voltages[4,5]. The dynamic MVL circuit proposed by Wu *et al*.[7] has a simple structure. However, it has a low noise margin, uses four power supplies, and also requires a complex process technology to obtain threshold-adjusted devices. The dynamic approach proposed by Herrfeld *et al*.[8] uses standard CMOS technology and has a high noise margin. However, the circuits are quite complex and must be buffered between two successive stages to avoid incorrect discharging in the evaluation phase. The last reported dynamic ternary circuit was developed by Toto *et al*.[9], which allows the realization of ternary circuits with a standard CMOS process, three supply voltages, and high noise margins. However, the floating output affects the circuit performance when the input is at logic '1'. While the dynamic approaches have some benefits, they also have known problems such as clock race and charge redistribution.

Double pass-transistor logic (DPL)[10] has a balanced input capacitance. This reduces the dependence of the delay on the input data. The symmetrical circuit configuration results in high logic functionality. The DPL is used to attain a full rail-to-rail swing, and is very attractive for high speed and low power applications[11]. In Ref. [12], a Karnaugh map-based method for synthesizing binary DPL circuits is developed. The DPL is first intro-

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duced to design MVL circuits by Hang[13] and Park *et al*.[14]. In Ref. [14], a neuron-MOS transistor is used to design literal functions.

In this paper, a new static voltage-mode CMOS circuit scheme using DPL to realize ternary logic and a general method for synthesizing ternary logic gates are proposed. Guided by the theory of transmission switches, the logical relation of each MOS transistor is formulated by using the transmission operation. A way to generate ternary complementary and dual circuits by applying the complementarity and duality principles is presented. It is simple and intuitive and can be extended to generate larger logic functions. The circuit scheme consists of complementary inputs/outputs and is thus a dual rail ternary logic. The most significant features are the use of standard CMOS processes without any modification of the thresholds, and a less complex structure. The ease of fabrication also makes MVL circuits more practical.

2 Theory of transmission switches for a double pass-transistor

Based on the theory of transmission switches[4], the following two kinds of variables are introduced in multiple-valued circuits using a double pass-transistor.

(1) Assume that $\alpha, \beta, \cdots$ are switching variables. Their values are taken to be T or F, only representing two states of MOS transistors, ON and OFF. The basic operations related to switching variables are AND ($\cdot$), OR ($+$), and NOT($\sim$), which are expressed as $\alpha \cdot \beta, \alpha + \beta$, and α, respectively, and are used to describe three physical situations: connections of element in serial, parallel, and switching state inverse.

(2) Assume that $x, y, \cdots$ are signal variables. Taking a ternary signal as an example, its logic value is taken as 0, 1, and 2, which correspond to three different voltage signals, such as 0, 1.5, and 3V. They have a clear meaning of magnitude and can be identified by comparing their magnitude with a detection threshold $t, t \in \{0.5, 1.5\}$. For example, the two corresponding detection threshold voltages may be 0.75 and 2.25V, respectively. The basic operations related to signal variables are minimum ($\cap$), maximum ($\cup$), complement ($-$), literal ($^i x^i$) operations, etc.

In order to describe the interaction between the on-off states of switching elements and signals, the following four basic operations can be introduced.

Low-threshold comparison operation:

$$x^t \triangleq \begin{cases} T, & x < t \\ F, & x > t \end{cases} \tag{1}$$

High-threshold comparison operation:

$${}^t x \triangleq \begin{cases} T, & x > t \\ F, & x < t \end{cases} \tag{2}$$

These two equations represent the low-acting switching characteristic of a pMOS transistor and the high-acting switching characteristic of an nMOS transistor, respectively.

Transmission operation:

$$s \triangleright \alpha \triangleq \begin{cases} s, & \alpha = T \\ \phi, & \alpha = F \end{cases} \tag{3}$$

Here s is the transmitted source signal, and α represents the switching state of a transmission switch network. If $\alpha = T$, the signal s is transmitted to the output. If $\alpha = F$, the switch network is off and its output is in the high-impedance state, which is denoted by the symbol ϕ. To express the joining of the outputs of two (or more) transmission branches, the following operation can be further defined:

Union operation:

$$s_1 \triangleright \alpha \# s_2 \triangleright \beta \triangleq \begin{cases} s_1 \triangleright \alpha, & \beta = F \\ s_2 \triangleright \beta, & \alpha = F \end{cases} \tag{4}$$

In Eq. (4), the transmission operation $\triangleright$ takes priority over the union operation $\#$. Also, if $s_1 \neq s_2$ and $\alpha = \beta = T$, a voltage conflict arises between sources s_1 and s_2. This condition is not allowed.

Based on Eqs. (1) and (2), the following properties can be easily derived:

$$\begin{cases} x^t = \overline{{}^t x} \\ {}^t x = \overline{x^t} \end{cases} \tag{5}$$

Equation (5) indicates that the two threshold comparison operations can be transformed by complementing the signal variable.

The above theory of transmission switches lays a foundation for realizing the design technique of multiple-valued circuits using a double pass-transistor at the switch level.

3 Circuit design of ternary unary functions

A literal circuit is the fundamental element in

MVL circuits. Taking ternary logic as an example, the truth table of ternary literals is shown in Table 1, and the following transmission operations can be obtained.

$$ {}^{0}x^{0} = \bar{x} \rhd x^{0.5} \# 0 \rhd^{0.5} x \quad (6) $$

$$ {}^{2}x^{2} = 0 \rhd x^{1.5} \# x \rhd^{1.5} x = 0 \rhd^{0.5} x \# x \rhd x^{0.5} \quad (7) $$

Table 1 Truth table of the ternary literal functions

x	${}^{0}x^{0}$	$\overline{{}^{0}x^{0}}$	${}^{2}x^{2}$	$\overline{{}^{2}x^{2}}$
0	2	0	0	2
1	0	2	0	2
2	0	2	2	0

To attain a full logic swing, a source voltage of 0 and a high level must be transmitted by nMOS and pMOS transistors, respectively. By using Eq. (5), the last item of ${}^{2}x^{2}$ can be easily derived. In the above two equations, low-threshold operation is realized by pMOS, while the high-threshold operation is realized by nMOS. Using the complementarity principle, the complementary logic function in ternary double-pass logic can be generated after the following modifications are made to the true function:

(1) Swap pMOS and nMOS transistors;

(2) Invert all pass and gate signals.

According to the above transmission operations and following the complementarity principle, the ternary literal gates can be designed as shown in Fig. 1. Their behavior is straightforward. The circuit realization of ${}^{0}x^{0}$ is also called a negative ternary inverter (NTI), and the circuit realization of $\overline{{}^{2}x^{2}}$ is also called a positive ternary inverter (PTI)[1,7].

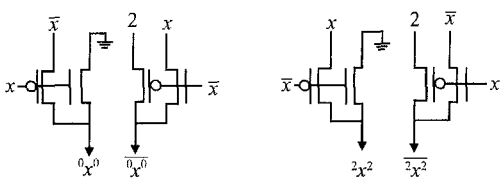

Fig. 1 Circuit realizations of ternary literal functions

Table 2 gives some ternary unary functions, where $x \oplus 1$ and $x \oplus 2$ are called the ternary cycling function and the inverse cycling function respectively, and $x\langle + \rangle 1$ and $x\langle - \rangle 1$ are called the operations of ternary truncated sum 1 and truncated difference 1, respectively. Their transmission functions are expressed as:

$$ x \oplus 1 = 1 \rhd x^{0.5} \# 2 \rhd^{0.5} x \cdot x^{1.5} \# \bar{x} \rhd^{1.5} x = \underline{1} \rhd^{1.5} x \# 2 \rhd x^{1.5} \cdot x^{1.5} \# x \rhd^{1.5} x \quad (8) $$

$$ x \oplus 2 = \underline{x} \rhd x^{0.5} \# 0 \rhd^{0.5} x \cdot x^{1.5} \# 1 \rhd^{1.5} x = x \rhd x^{0.5} \# 0 \rhd^{0.5} x \cdot^{0.5} \underline{x} \# 1 \rhd x^{0.5} \quad (9) $$

$$ x\langle + \rangle 1 = 1 \rhd x^{0.5} \# 2 \rhd^{0.5} x = 1 \rhd^{1.5} x \# 2 \rhd x^{1.5} \quad (10) $$

$$ x\langle - \rangle 1 = 0 \rhd x^{1.5} \# 1 \rhd^{1.5} x = 0 \rhd^{0.5} \bar{x} \# 1 \rhd x^{0.5} \quad (11) $$

Table 2 Truth table of the ternary unary functions

x	$x \oplus 1$	$x \oplus 2$	$x\langle + \rangle 1$	$x\langle - \rangle 1$
0	1	2	1	0
1	2	0	2	0
2	0	1	2	1

The last item in every expression is derived by using Eq. (5) to meet the demand that the low level 0 and the high level 2 must be transmitted by nMOS and pMOS transistors, respectively. Notice that the mediate source 1 may be transmitted by nMOS or pMOS transistors; thus the conflict between two sources 0 and 1 or 1 and 2 should be avoided. From Eqs. (8) and (9), it can be seen that the connections of two pMOS in serial and two nMOS in serial are used to transmit 2 and 0, respectively. Their complementary logic functions can be realized by the complementarity principle. The circuit realizations corresponding to the above equations and their complementary functions are shown in Fig. 2.

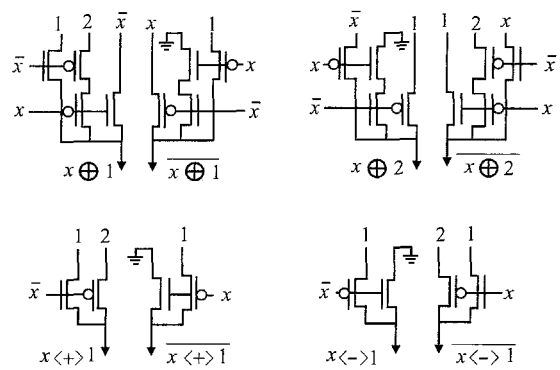

Fig. 2 Circuit realizations of ternary unary functions

4 Circuit design of ternary two-variable functions

The above proposed ternary unary gates can be used to construct complex gates. For example, Figures 3(a) and (b) show the Karnaugh map for a

2-variable ternary AND function and OR function, respectively. According to the coverage shown in Figs. 3(a) and (b), the following transmission operations can be obtained:

$$x \cap y = 0 \rhd \underline{x}^{0.5} \# x|_{x=1,2} \rhd^{1.5} y \# y|_{y=0,1} \rhd (\underline{y}^{1.5} \cdot^{0.5} x) = 0 \rhd^{1.5} \underline{x} \# x|_{x=1,2} \rhd \underline{y}^{0.5} \# y|_{y=0,1} \rhd ({}^{0.5}\underline{y} \cdot^{0.5} x) \quad (12)$$

$$x \cup y = 2 \rhd^{1.5} x \# x|_{x=0,1} \rhd \underline{y}^{0.5} \# y|_{y=1,2} \rhd (x^{1.5} \cdot^{0.5} \underline{y}) = 2 \rhd \underline{x}^{0.5} \# x|_{x=0,1} \rhd^{1.5} \underline{y} \# y|_{y=1,2} \rhd (x^{1.5} \cdot \underline{y}^{1.5}) \quad (13)$$

In Eq. (12), $0 \rhd^{1.5} \underline{x}$ means that the nMOS turns on and the source signal $\underline{0}$ is transmitted to the output only when $\underline{x} = 0$ (i.e. $x = 2$). Thus, it can be rewritten as $0 \rhd^{1.5} \underline{x} = 0 \rhd^{1.5} ({}^0x^0) = 0 \rhd^{0.5} ({}^0x^0)$. Similarly, $x|_{x=1,2} \rhd \underline{y}^{0.5}$ means that the pMOS is on and $x = 1$ or 2 is transmitted to the output only when $y = \underline{2}$ (i.e. $y = 0$). Thus, $x|_{x=1,2} \rhd \underline{y}^{0.5} = x|_{x=1,2} \rhd (\overline{{}^2y^2})^{0.5}$. The last item in Eq. (12), $y|_{y=0,1} \rhd ({}^{0.5}\underline{y} \cdot^{0.5} x)$ stands for the connection of two nMOS transistors in serial to transmit signal $y = 0$ or 1 only when $y = 0$ or $\underline{1}$ and $x = 1$ or 2. Thus, $y|_{y=0,1} \rhd (\underline{}^{0.5}\underline{y} \cdot^{0.5} x) = y|_{y=0,1} \rhd [{}^{0.5}(\overline{{}^2y^2}) \cdot^{0.5} (\overline{{}^0x^0})]$. Then Equation (12) can be rewritten as follows:

$$x \cap y = 0 \rhd^{0.5} ({}^0x^0) \# x|_{x=1,2} \rhd (\overline{{}^2y^2})^{0.5} \# y|_{y=0,1} \rhd [{}^{0.5}({}^2y^2) \cdot^{0.5} (\overline{{}^0x^0})] \quad (14)$$

In the same way, Equation (13) can be rewritten as follows:

$$x \cup y = 2 \rhd (\overline{{}^2x^2})^{0.5} \# x|_{x=0,1} \rhd^{0.5} ({}^0y^0) \# y|_{y=1,2} \rhd [({}^2x^2)^{0.5} \cdot ({}^0y^0)^{0.5}] \quad (15)$$

The circuit realizations corresponding to the above two equations are shown in Figs. 3(c) and (d) respectively, where some input literal signals are produced from the circuits shown in Fig. 1, and the ternary NAND and NOR gates are generated from their true functions by the complementarity principle. As can be seen from Fig. 3, it is perfectly symmetrical. This results in a balanced input capacitance and reduces the dependence of the delay time on data. It is also worth noting that only two external supply voltages (V_{DD} and GND) are needed, while the proposed circuit only acts as a middle block in the ternary system. The symmetrical structure makes it easy to realize other ternary complex functions.

In fact, because AND-OR is the dual logic function, ternary OR circuits can be formed from

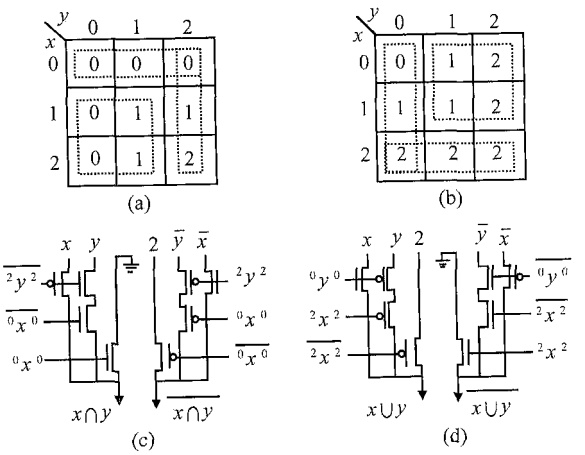

Fig. 3 (a) K-map for ternary AND operation; (b) K-map for ternary OR operation; (c) Ternary AND/NAND gate; (d) Ternary OR/NOR gate

ternary AND circuits by using the duality principle. The dual logic function in ternary double-pass logic can be generated after the following modifications:

(1) Swap pMOS and nMOS transistors;

(2) Swap logic 2 and logic 0, while logic 1 remains unchanged;

(3) Swap ${}^ix^i$ and $\overline{{}^i\underline{x}^i}$ $(\overline{{}^i\underline{x}^i})$, ${}^iy^i$ and $\overline{{}^i\underline{y}^i}$ $(\overline{{}^i\underline{y}^i})$, …;

The above duality principle can also be used to verify the circuit realizations of ternary unary functions shown in Fig. 2. For example, $x \oplus 1$ and $x \oplus 2$, $x\langle + \rangle 1$ and $x\langle - \rangle 1$ are dual logic functions.

From the above discussion, it can be seen that the synthesis efficiency is enhanced by the complementarity and duality principles. Using these principles, for example starting from the realization of a ternary AND circuit with simple transformations, one can obtain complementary and dual functions (ternary NAND, OR/NOR) using the same circuit structure, improving the library versatility. As another example, Figure 4(a) gives the Karnaugh map for ternary mod-3 multiplication. According to the coverage shown in Fig. 4(a), the following transmission operations can be obtained:

$$x \otimes y = 0 \rhd [{}^{0.5}({}^0y^0) + {}^{0.5}({}^0x^0)] \# x|_{x=1,2} \rhd [({}^0y^0)^{0.5} \cdot ({}^2y^2)^{0.5}] \# y|_{y=2} \rhd [({}^0x^0)^{0.5} \cdot x^{1.5}] \# 1 \rhd (x^{1.5} \cdot^{1.5} y) \quad (16)$$

Based on Eq. (16), the logic function $x \otimes y$ is first mapped into circuit realization. Then, using the

same circuit structure, swapping pMOS and nMOS transistors, and inverting all pass and gate signals, its complementary function $x \otimes y$ can be easily obtained as shown in Fig. 4(b).

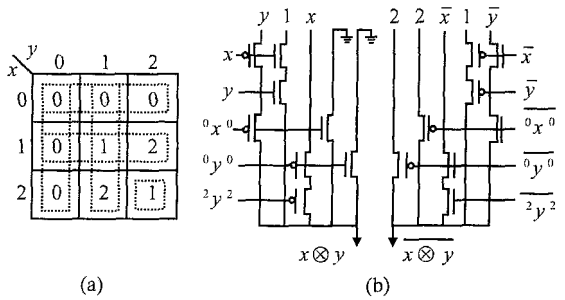

Fig. 4 (a) K-map for ternary mod-3 multiplication; (b) Circuit realization of ternary mod-3 multiplication

The proposed circuits have been simulated using HSPICE and the model parameters of a TSMC 0.25μm CMOS process. Taking the ternary AND/NAND gate shown in Fig. 3(c) as an example, the transient simulation results with a 0.1pF load at each output node, are given in Fig. 5(a). In the simulation, the voltages [0, 1.5V, 3V] are taken to represent the logic values [0, 1, 2]. The simulation results demonstrate that the full logic swing and the maximum possible noise margins are attained due to the usage of both pMOS and nMOS pass transistors. The energy dissipation curve is given in Fig. 5(b). For contrast, the energy dissipation curve of the ternary NAND gate reported in Ref. [4] is also given in Fig. 5(b) under the same simulation conditions except for modified thresholds. A detailed comparison between the proposed ternary AND/NAND gate here and the ternary NAND gate reported by Wu *et al*.[4] is summarized in Table 3. It can be concluded that the proposed circuits dissipate less power and they are improved, when both the transistor counts and the operation rates are considered. Moreover, a significant feature of the proposed circuits is the use of a standard CMOS process without any modification of the thresholds, while in the circuits proposed in Ref. [4] two pairs of transistors with modified thresholds are needed.

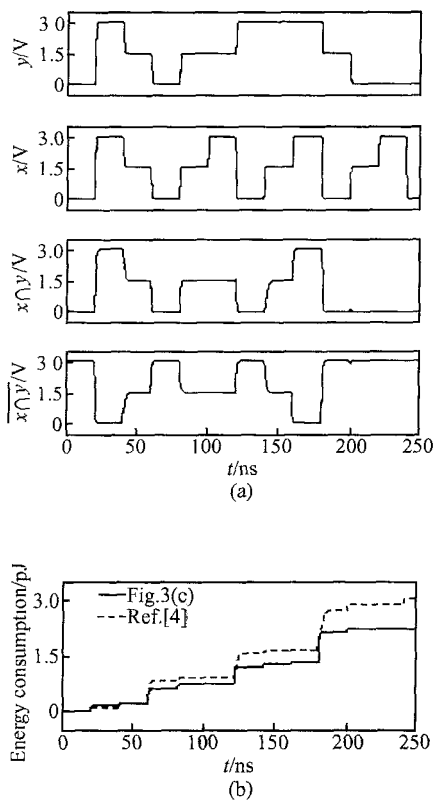

Fig. 5 (a) Simulated transient characteristics of ternary AND/NAND gate; (b) Energy consumption curve

Table 3 Comparisons between Fig. 3(c) and ternary NAND gate[4]

Subject for comparison	Proposed AND/NAND	NAND[4]
Transistor count	16 (includes AND and NAND)	16
Number of V_{th}	1	2
Propagation delay/ns (worst case)	1.91/1.45 0.1pF load	2.36 0.1pF load
Power consumption/μW	8.9	12.1

5 Conclusion

Based on the theory of transmission switches, a new kind of static circuit scheme for ternary logic and a general method for synthesizing ternary logic gates have been developed. A way to generate complementary and dual circuits was presented. By using the complementarity and duality principles, the versatility of circuits is enhanced. In the proposed circuit scheme, literal functions are also realized by using traditional MOS transistors, while in Ref. [14], they are designed using neuron-MOS transistors. As compared to some reported static ternary circuits, this new scheme uses a standard CMOS process. Furthermore, it has a perfectly symmetrical structure and attains the full logic swing and the maximum possible noise margins. As compared to some dynamic ternary circuits, it does not suffer from known problems such as clock race

and charge redistribution. In binary DPL, for any input combination, there are always two current paths driving the output, while in TDPL, this characteristic does not always exist. The circuit verification of these proposed ternary logic circuits are verified by HSPICE simulation with a TSMC 0.25μm CMOS device parameter. Furthermore, the proposed method can be extended to generate larger ternary logic functions and to synthesize quaternary logic circuits.

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三值双传输管电路的通用综合方法*

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摘要: 提出采用双传管逻辑设计三值电路的方法,对每个 MOS 管的逻辑功能均采用传输运算予以表示以实现有效综合. 建立了三值双传输管电路的反演法则和对偶法则. 新提出的三值双传输管逻辑电路具有完全基于标准 CMOS 工艺,无需对 MOS 管作任何阈值调整,结构简单、规则,输入信号负载对称性好,逻辑摆幅完整以及无直流功耗等特点. 采用 TSMC 0.25μm 工艺参数和最高电压为 3V 的 HSPICE 模拟结果验证了所提出综合方法的正确性.

关键词: 开关电路理论; 多值逻辑; 逻辑综合; 双传输管逻辑

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