A High-Performance Silicon Electro-Optic Phase Modulator with a Triple MOS Capacitor*

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Abstract: We propose and analyze a novel Si-based electro-optic modulator with an improved metal-oxide-semiconductor (MOS) capacitor configuration integrated into silicon-on-insulator (SOI). Three gate-oxide layers embedded in the silicon waveguide constitute a triple MOS capacitor structure, which boosts the modulation efficiency compared with a single MOS capacitor. The simulation results demonstrate that the $V_\pi L_\pi$ product is 2.4V · cm. The rise time and fall time of the proposed device are calculated to be 80 and 40ps from the transient response curve, respectively, indicating a bandwidth of 8GHz. The phase shift efficiency and bandwidth can be enhanced by rib width scaling.

Key words: carrier accumulation; plasma dispersion effect; electro-optic phase modulator; metal-oxide-semiconductor; optoelectronic integrated circuit

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1 Introduction

With the dramatic down-scaling in the feature size of integrated circuits (IC), more and more transistors can be integrated into one silicon wafer. This also improves the performance of the transistors, but it has a negative impact on the resistance of metal interconnects, whose delay increases with the scaling[1]. Metal interconnects seem to be the bottleneck for the system performance of the next generation of Si integrated circuits. Fortunately, optical interconnects can overcome the limitations of conventional interconnection technology with their high speed and low power consumption[2]. Optoelectronic integrated circuits (OEIC), which integrate optical elements and advanced electronics together on a single silicon substrate, have received much attention because of their potential advantages.

Several OEIC components, such as Si passive and active elements, including waveguides[3], couplers[4], AWGs[5], light emitters[6], modulators[7~14], and photodetectors[15], have been extensively studied. Optical modulators are used to encode signal data into light waves to realize optical communication links in OEIC. For their significant role in silicon photonics, many Si-based thermo-optic[7] and electro-optic[8~14] modulators have been theoretically and experimentally demonstrated. The refractive index of a thermo-optic modulator changes with the variation of temperature via the thermo-optic effect. Although the thermo-optic effect is remarkable in Si, it is rather slow and can provide modulation frequencies of only 700kHz[7]. The plasma dispersion effect is exploited to realize higher modulation frequencies to meet the requirement of fast optical communication systems.

Different configurations of modulators based on the plasma dispersion effect have been proposed, including pin diodes[8,9], three terminal bipolar-mode field-effect transistors (BMFET)[10], metal-oxide-semiconductor (MOS) capacitors[11~13], and four terminal p^+pnn^+ structures[14]. For pin and BMFET structures, both the refractive index and absorption change through carrier injection with a positive bias or positive

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current. These devices exhibit a lower frequency (several MHz) and a higher DC power compared with MOS and four-terminal p^+pnn^+ structures, whose refractive indexes vary with carrier accumulation or depletion. MOS capacitor modulators have demonstrated experimentally a modulation frequency of 1GHz[11]. Even higher bandwidth performance (10GHz) has been achieved through improvements in material quality, device design, and driver circuitry[12]. The main drawback of the MOS capacitor structure is the weak dependence of silicon's refractive index on electron-hole pair concentration because of the small interaction region between the carrier accumulation and optical waveguide mode[8], with the result that the $V_\pi L_\pi$ is 8V·cm. A shunt-capacitor configuration has been proposed to enhance the light confinement effect in the waveguide and enlarge the area of index-change region, resulting in a V_π of 4V and an active region length of 8mm[13].

In this paper, we present and simulate a silicon modulator based on a triple MOS capacitor to further improve the overlap between the carrier accumulation region and optical mode. Through careful analysis and software simulation, the device shows a higher modulation efficiency and a shorter active region.

2 Device structure

Figure 1 shows a schematic cross-section view of the proposed configuration. First, a trench with width $w_t = 2.0\mu m$ and depth $h_t = 3.5\mu m$ is etched by RIE on the SOI wafer. Second, a horizontal thin oxide layer and two vertical thin oxide layers are grown in the trench. Both the horizontal and vertical oxide layers have the same thickness of $\tau = 10nm$. Then, a polysilicon layer is deposited by low pressure chemical vapour deposition (LPCVD)[16] in the trench to form the inner rib of the waveguide. The polysilicon layer can be replaced with a single-crystal silicon layer deposited by epitaxial lateral overgrowth (ELO) for lower transmission loss. In order to guarantee single-mode operation conduction, the lateral silicon of the SOI wafer is etched by $h_r = 2.0\mu m$, leaving an outer rib with width $w_o = 2.0\mu m$ and height $h_o = 3.0\mu m$. The total width of the rib waveguide is $w = w_t + 2w_i = 4.0\mu m$. The single-crystal silicon layer of SOI has an n-type doping concentration of $10^{17} cm^{-3}$, and the deposited silicon layer has the same doping concentration but is p-type. Heavily doped p^+ and n^+ regions with doping concentration of $10^{19} cm^{-3}$ are formed in the surface to make ohmic contacts to metal. Finally, a top SiO_2 cladding layer covers the whole structure.

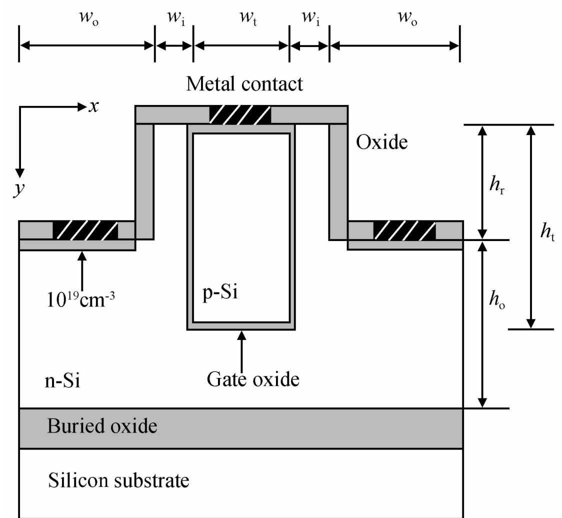

Fig. 1 Schematic cross-section of the novel modulator with three capacitors

Thus, a horizontal and two vertical gate oxide layers form the configuration of the triple MOS capacitor structure. The optical confinement in this device is the same as a conventional SOI rib waveguide because the gate oxide layer is very thin. When a forward bias voltage is applied to the metal contact, electrons and holes are accumulated on two sides of the gate oxide layer.

3 Device model

Unstrained pure crystalline Si does not exhibit a linear electro-optic (Pockels) effect, and the Kerr effect and the Franz-Keldysh effects are very weak. Therefore, the most effective mechanism for varying the refractive index in pure silicon at a fast response is the free carrier plasma dispersion effect. Soref and Bennet[17] empirically determined the refractive index and the absorption coefficient as functions of free carriers in silicon by Kramers-Kronig transformation of experimental data. At the wavelength of 1.55μm, the relations are given by

$$\Delta\alpha = \Delta\alpha_e + \Delta\alpha_h = 8.5\times10^{-18}\times\Delta N + 6.0\times10^{-18}\times\Delta P \quad (1)$$

$$\Delta n = \Delta n_e + \Delta n_h = -8.8\times10^{-22}\times\Delta N - 8.5\times10^{-18}\times(\Delta P)^{0.8} \quad (2)$$

where $\Delta\alpha_e$ and $\Delta\alpha_h$ are the variations of the absorption coefficient due to the changes of the electron and hole concentration, Δn_e and Δn_h are the changes of the refractive index due to the changes of the electron and hole concentration, and ΔN and ΔP are the changes of the electron and hole concentrations, respectively. In our device, accumulated charges near the gate oxide alter the waveguide refractive index due to the free carrier dispersion effect, resulting in a phase shift of the optical mode. The phase shift $\Delta\phi$ can be described as

$$\Delta\phi = \frac{2\pi\Delta n_{\mathrm{eff}}}{\lambda}L \quad (3)$$

where L is the length of the phase shifter and Δn_{eff} is the effective change. To realize intensity modulation, one can employ a dual-arm Mach-Zehnder interferometer, a micro-ring resonator, a Fabry-Perot cavity, or a Brag reflector structure.

4 Results and discussion

4.1 Optical simulation

The optical characteristics of the proposed device are simulated with the beam propagation method (BPM) simulator BeamPROP. Figure 2 shows the optical mode profile of the device. The simulation results show that the optical field is mostly confined in the center of the three gate oxide layers. Thus the high optical field region of the guided mode overlaps more strongly with the

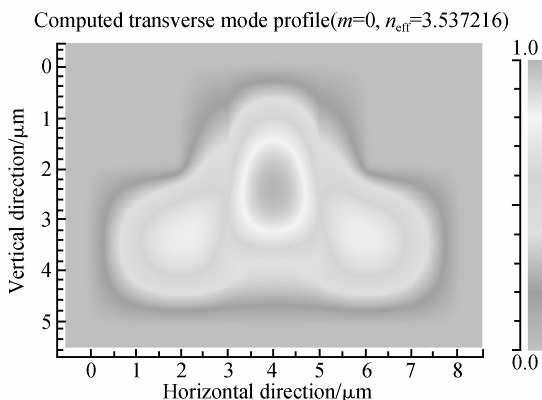

Fig. 2 Fundamental mode profile of the proposed device

regions of high charge density in the waveguide. Since the modal-field profile overlapping with the carriers determines the modulation efficiency, a higher modulation efficiency is achieved in our device compared with a single MOS capacitor[11] and dual MOS capacitor[13].

4.2 Electrical simulation

4.2.1 Static characteristics

In order to define the phase shift efficiency, the profile of the accumulated carrier in the waveguide must be investigated first. A commercially available simulation package, ATLAS from SILVACO, is employed here to model the carrier distribution in the waveguide. The device is modeled assuming that there are only ohmic contacts without any additional contact resistance or capacitance, and the Shockley-Reed-Hall recombination carrier lifetimes are set to be $t_n = 50$ns and $t_p = 50$ns.

As shown in Figs. 3 (a) and (b), the carriers near the region of the gate oxide are depleted at the voltage of 0 because of the flat band voltage of the MOS capacitor. When a positive voltage is applied to the device, a thin accumulated carrier layer about several tens of nanometers is formed in the vicinity of two sides of the gate oxide, as shown in Figs. 3 (c) and (d). Both the larger area of the accumulated carrier layer and the higher density of the accumulated carriers can enhance the phase efficiency. A higher doping concentration of the device results in a higher phase modulation efficiency due to the higher density of the accumulated carrier layer, and it also induces higher absorption index changes, which will cause larger transmission loss. Therefore there is a compromise between phase efficiency and transmission, resulting in a doping level of $10^{17}\mathrm{cm}^{-3}$.

Figure 4 shows phase shift as a function of the applied voltage for different phase shifter lengths. A $V_\pi L_\pi$ of 2.4V · cm is achieved from the simulation results, where V_π and L_π are the voltage and the active length required for a phase shift of π radians, respectively. When the size of the modulator decreases, the phase modulation efficiency is enhanced because the optical mode is more tightly confined in the region of the gate oxide and interacts more strongly with the accumulated charge layers.

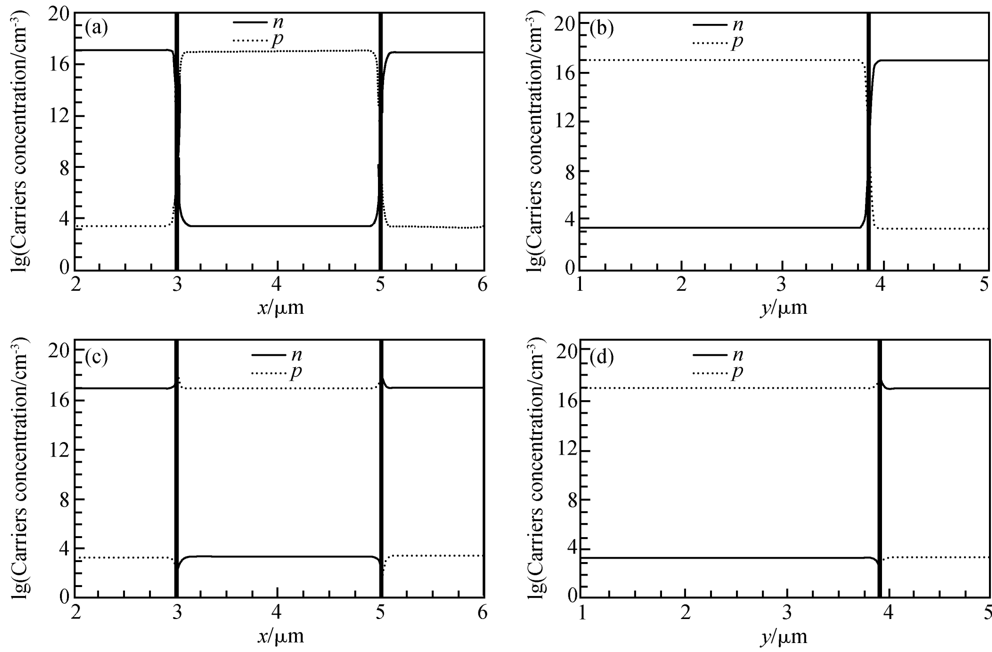

Fig. 3 Carrier concentration distributions (a) Cutline at $y = 3\mu m$, 0V applied voltage; (b) Cutline at $x = 4\mu m$, 0V applied voltage; (c) Cutline at $y = 3\mu m$, 5V positive applied voltage; (d) Cutline at $x = 4\mu m$, 5V positive applied voltage

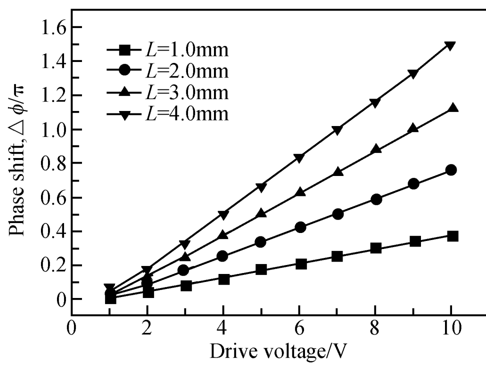

Fig. 4 Phase shift as a function of the applied voltage for different phase shifter lengths

4.2.2 Transient characteristics

The switching characteristics of the device are modeled using a transient solution. The transient time is characterized with ATLAS in terms of carrier concentration against time. A 3ns long square wave voltage with a value of 3V and a rise/fall time of 1ps is chosen to simulate the transient response of the carrier concentration near the gate oxide region. From the switching characteristics as shown in Fig. 5, the rise and fall time are 80 and 40ps, respectively. The total switching time is 0.12ns, indicating that the modulator can operate at high frequencies. It should be noted that the doping levels and modulator dimension here are not optimized for the transient response; the switching time will be reduced by higher doping and smaller waveguide width.

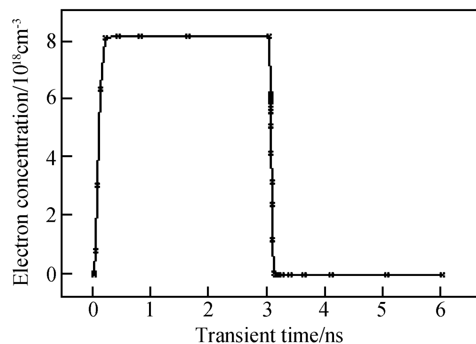

Fig. 5 Switching characteristics of the modulator at 3V forward voltage

5 Conclusion

We have proposed and analyzed a novel Si-based triple MOS capacitor modulator, which has one horizontal gate oxide layer and two vertical gate oxide layers. A 2D semiconductor simulation

package, ATLAS from SILVACO, is employed to investigate the dc and transient behaviors of the modulator by solving the Poisson and continuity equations. The beam propagation method (BPM) is also used to calculate the modal-field profile and the optical field amplitude distribution in the waveguide. Simulation results show that an active length of the modulator of $L_{\pi} = 4800\mu m$ is sufficient to yield a phase shift of π radians at a forward bias of 5V. The rise time and fall time are 80 and 40ps, respectively.

The phase modulation efficiency and transient response will be enhanced when the rib width decreases. The simulated characteristics make the proposed configuration very promising for high-frequency applications in OEIC.

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高性能硅基 MOS 电光相位调制器*

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摘要：提出了一种 SOI 新型 MOS 电容型电光调制器. 与普通单一电容型 MOS 调制器相比，由三层栅氧化层形成的新型 MOS 电容型调制器提高了调制效率. 模拟显示，调制电压和调制长度乘积为 $V_{\pi} L_{\pi} = 2.4V \cdot cm$，上升和下降时间分别为 80 和 40ps，带宽达到了 8GHz. 通过减小器件尺寸能进一步提高调制效率和调制速度.

关键词：载流子积累；等离子色散效应；电光相位调制器；金属-氧化物-半导体；光电子集成回路

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