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Analysis of Si/GaAs Bonding Stresses with the Finite Element Method*

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Abstract: In conjunction with ANSYS, we use the finite element method to analyze the bonding stresses of Si/GaAs. We also apply a numerical model to investigate a contour map and the distribution of normal stress, shearing stress, and peeling stress, taking into full consideration the thermal expansion coefficient as a function of temperature. Novel bonding structures are proposed for reducing the effect of thermal stress as compared with conventional structures. Calculations show the validity of this new structure.

Key words: bonding; thermal stress; finite element analysis
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1 Introduction

The bonding technique has been widely applied in opto-electronic devices because of its immunity to crystal lattice and directional mismatch. When two homogeneous or heterogeneous wafers that are clean and smooth on the atomic level are pressed together face to face at a certain temperature, the atoms on the two surfaces connect with a valence bond. When this binding energy reaches the level of the bulk material, the bonding process is completed. A bonded interface is achieved regardless of the lattice mismatches and the orientation mismatch, thus allowing great freedom of material choice and device fabrication. The investigation of wafer bonding, especially for materials with a large lattice mismatch, is important for overcoming epitaxy difficulties and optimizing device structures. For this bonding technique, the study of Si and Ⅲ-Ⅴ group materials bonding is essential for the realization of Si-based opto-electronic integration.

However, when bonding heterogeneous wafers, thermal stress is introduced during annealing due to the mismatch of thermal expansion coefficients (TEC). Thermal stress may cause many problems, such as a change of energy band structure and the formation of the carrier recombination centers, which affect the optical and electrical performances of devices. If the thermal stress is very large, it may lead to the bending and debonding, or even cracking of the wafer. Thus, the physical properties of the bonding materials and interface are degraded, and the bond may fail or the device itself may be crippled. Therefore it is important to investigate the causes, distribution, and influence of the thermal stress for the application of the bonding technique.

A thermal stress distribution theory of bimetals for uniform temperature change has been reported[1]. Elastic and viscoelastic theories are also used for the analysis of film[2,3]. In this paper, we use the finite element method (FEM) to investigate thermal stress distribution and its influence on Si/GaAs bonding.

2 Physical and numerical model

We consider the bonding of Si/GaAs in the case of cylindrical samples with a thickness of 300μm and a radius of 5mm. General calculations treat the TEC as a constant, ignoring its change with the temperature. Actually, the choice of the co-

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efficient greatly influences the calculation results.

Here, in order to make the simulation more like the real process, the relation of the TEC to temperature is set as shown in Fig. 1 (cited from Ref. [4]). Our calculations show that when the TECs of Si and GaAs are set at 2.6×10^{-6} and $6.8\times10^{-6}\,K^{-1}$, respectively, the calculated stress is twice as large as the experimental values.

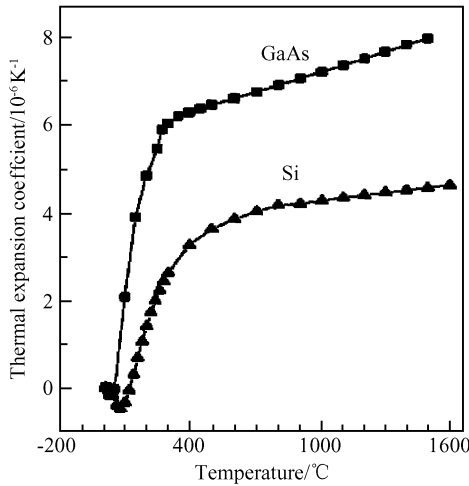

Fig. 1　Thermal expansion coefficients of Si and GaAs as functions of temperature

The following bonding process is proposed at room temperature (25℃). The Si and GaAs samples are separated and heated to 500℃. At this time, both wafers are free of stress. Then, the wafers are placed in contact and bonded. After that, the bonded wafers are cooled to room temperature, and they are subjected to thermal stress because of their different TECs. Here, no external pressure is applied.

We use finite element analysis (FEA) to analyze the above physical process. For the axisymmetric property of a cylindrical sample, a 2D simplified plane model is applied for numerical analysis. The material parameters used for Si and GaAs are shown in Table 1. Here, isotropy and linear elasticity are assumed for both materials to simplify the calculation.

Table 1　Material parameters of Si and GaAs

Material	Young's modulus /10^{11} Pa	Poisson's ratio	Thermal conductivity /(W/(cm·K))
Si	1.66	0.29	1.5
GaAs	1.19	0.32	0.455

In an ideal bonding interface, there are no bubbles, cavities or defects. During the cooling process for such ideal bonding, the displacement of the corresponding nodes on the interface stays the same in the x[1] and y directions. This can be expressed by the equation

$$x_{\mathrm{GaAs}_i} = x_{\mathrm{Si}_j},\quad y_{\mathrm{GaAs}_i} = y_{\mathrm{Si}_j} \tag{1}$$

where i and j are the numbers of nodes for GaAs and Si on the interface, respectively. The bonding structure is thoroughly meshed by quadrangles as shown in Fig. 2. The above physical and numerical model can be solved by ANSYS.

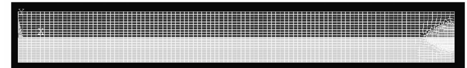

Fig. 2　Mesh for 2D Si/GaAs bonding structure

3　Results and discussion

3.1　Contour map and distribution of stress

Normal stress, axis direction stress, and shearing stress are calculated. The results are shown in Fig. 3.

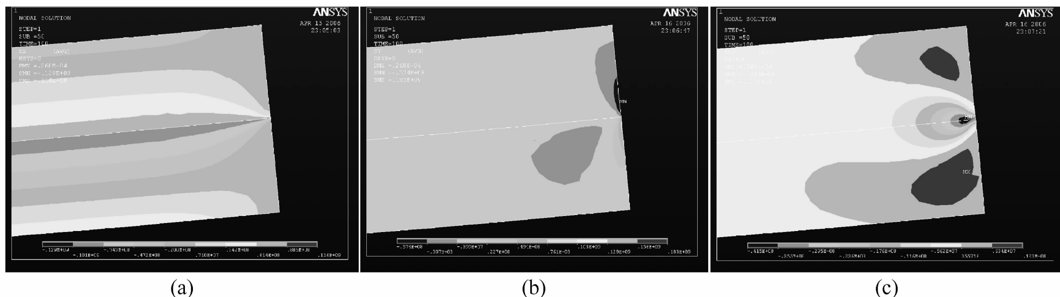

Fig. 3　(a) Contour map of normal stress; (b) Contour map of axial stress; (c) Contour map of shearing stress

Figure 3(a) is a map of the normal stress, which is parallel to the interface. It shows that along the radial direction the stress is always uniform, but it decreases dramatically near the edge. Along the axial direction, the stress distribution has a sandwich structure, which is greatest at the interface and decreases farther away from it. The normal stress shows the tensile stress in the Si region and compressive stress in the GaAs region.

Figure 3(b) is a contour of the axial stress, which is perpendicular to the interface. It shows that axial stress only exists near the edge. There are two dense regions in the picture, which are located near the interface in the material region. At the interface, the axial stress is the peeling stress, which is the most important factor that influences the bonding process.

Figure 3(c) is a contour of the shearing stress, which is also parallel to the interface. There are three dense stress distribution regions near the interface and edge.

In order to determine the influence of the stress on the bonding, the trend at the interface must be known. Figure 4 is a plot of normal, peeling, and shearing stresses (corresponding to the SX, SY, and SXY curves, respectively). From this plot, it can be seen that SX, SY, and SXY are stable until they are about 0.5mm away from the

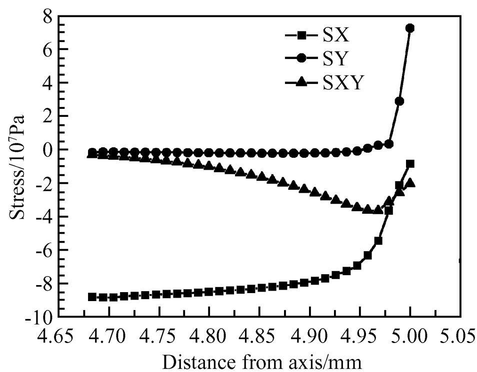

Fig. 4 Distribution of normal, shearing, and peeling stress along the interface

edge. In this region, SX (the normal stress) decreases to zero rapidly. SXY (shearing stress) and SY (peeling stress) increase dramatically from zero and reach their maxima on the edge or near the edge. The degree to which SX decreases is obviously less than the degree to which SXY and SY decrease. This indicates that near the edge, thermal stress, especially peeling stress, is very large, causing bonding difficulty on the edge. This edge effect is confirmed by our infrared transmission picture of the GaAs/Si bonding structure, as shown in Fig. 5.

From Fig. 5, the white area is the bonded region, and the dark area corresponds to the unbonded region. This indicates that in the central region, the bonding is good, while on the edge, the bonding quality is poor.

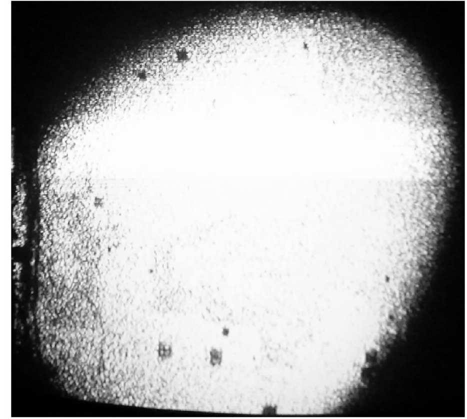

Fig. 5 Infrared transmission picture of Si/GaAs bonding structure

3.2 New structures for better bonding quality

Some methods for reducing the influence of the thermal stress on bonding have been reported[5~7]. In addition to the traditional way, which involves lowering the bonding temperature and thinning the bonding wafers, we can also change the bonding structure to reduce the thermal stress. As just mentioned, the thermal stresses are mainly focused at the edge. Thus we can make some changes around the edge to reduce the edge effect. The detailed structure is shown in Fig. 6. The thickness of the GaAs and Si samples is still 300μm, and the edges of samples are ground to a certain angle. In this way, the lengths of the bonding interfaces are 4 and 4.5mm, respectively (corresponding to Figs. 6(a) and (b)). Using the FEA method, we can also get the function of SX, SY, and SXY with the distance from the axis, which is shown in Fig. 7.

Figures 7 (a) and (b) show a change similar to that in Fig. 4 for curves SX, SY, and SXY, which correspond to normal stress, peeling stress, and shearing stress. SX decreases to zero, while SY and SXY increase from zero to their maxima at the edge. As well known, among thermal stres-

ses, peeling stress most strongly influences bonding quality. The smaller it is, the better the bonding quality is. The maximum values of peeling stress in Figs. 7(a) and (b) are 1.03×10^7 and 2.7×10^7 Pa, both of which are less than half of that in Fig. 4 (7.3×10^7 Pa). This indicates better bonding quality at the edge for the novel structures than for the conventional structure.

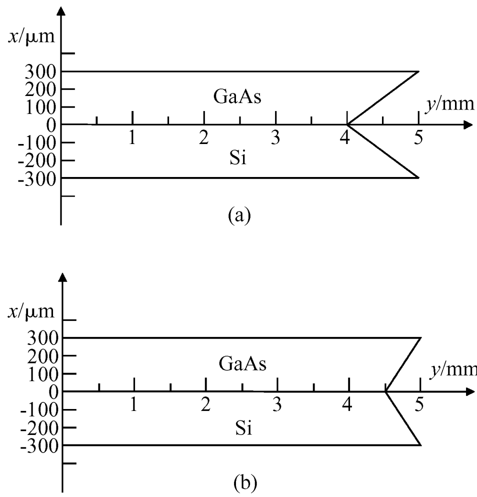

Fig. 6 Diagram of new structures

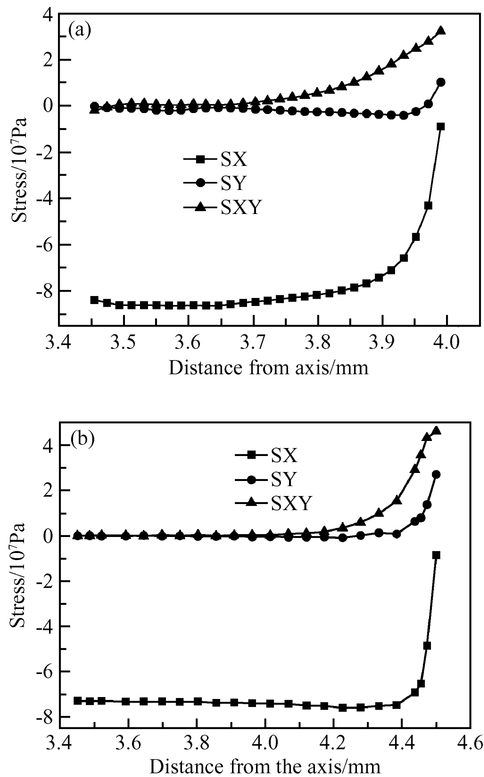

Fig. 7 Distribution of thermal stress along the interface for the structures in Fig. 6 (a) and (b)

4 Conclusion

The finite element analysis results show the distribution of the thermal stress for bonding wafers: the normal stress is stable away from the edge but decreases dramatically to zero at the edge; the shearing stress is zero until it reaches a maximum value near the edge; the peeling stress remains at zero and then increases rapidly to a maximum value at the edge. The distribution of the thermal stress suggests that there is an edge effect for bonding wafers. In order to reduce the influence of thermal stress on bonding quality, we propose novel bonding structures. Our numerical analysis shows that the structures are subjected to a much smaller peeling stress than the conventional one, which indicates better bonding quality and confirms the validity of the new structures.

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用有限元方法分析Si/GaAs的键合热应力*

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摘要： 在考虑材料热膨胀系数随温度变化后，采用有限元方法结合ANSYS软件对Si/GaAs键合热应力进行了分析，研究了普通应力、轴向应力和剪切力的分布云图和沿界面的分布.同时提出了新的键合结构以减小热应力的影响，计算结果证明了该结构的有效性.

关键词： 键合；热应力；有限元分析

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