A CMOS Low Power Fully Differential Sigma-Delta Frequency Synthesizer for 2Mb/s GMSK Modulation*

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Abstract: A CMOS fully-differential 2.4GHz Σ-Δ frequency synthesizer for Gaussian minimum shift keying (GMSK) modulation is presented. A pre-compensation fractional-N phase-locked loop (PLL) is adopted in the modulator. The transfer function of the type-Ⅱ third-order phase-locked loop is deduced, and the important parameters that affect the loop transfer function are pointed out. Methods to calibrate the important loop parameters are introduced. A differential tuned LC-VCO and a fully-differential charge pump are adopted in the PLL design. The designed circuits are simulated in a 0.18μm 1P6M CMOS process. The power consumption of the PLL is only about 11mW with the low power consideration in building blocks design, and the data rate of the modulator can reach 2Mb/s.

Key words: CMOS; fractional-N; Gaussian minimum shift keying; phase-locked loop; sigma-delta
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1 Introduction

GMSK modulation is suitable for low power, portable applications because the linearity requirement of the PA decreases[1]. In recent years, GMSK modulators have been actively studied[2~13]. There are basically three methods to realize a GMSK modulator. The first is the Cartesian architecture[2~5], which is in fact a quadrature up-conversion structure. Mismatch between the I and Q paths will distort the modulation signal. It uses two DA converters, two anti-alias filters, and two mixers to achieve the GMSK modulation. Many circuit components are used, and thus the power consumption is inevitably large. The second method is the open-loop modulation of the VCO[6~8]. The drawback of this method is that the frequency of the VCO drifts with temperature variation and the current leakage and modulation data are affected by the VCO phase noise. One DA converter and one filter are still needed, and they consume some power. The third method is the fractional-N PLL closed-loop modulation[9,10]. A digital Σ-Δ modulator is applied in this method, avoiding the use of a DA and filter. Thus the power consumption can be reduced. But the modulated data rate is limited by the loop bandwidth of the PLL. In order to resolve this problem, a pre-compensation filter is added after the Gaussian filter to compensate the loop bandwidth of the PLL[11]. The disadvantage of the Σ-Δ frequency synthesizer with pre-compensation filter is the mismatch between the transfer function of the pre-compensation filter, and the inverse of the PLL's transfer function will deteriorate the GMSK modulation.

Some works[12,13] have introduced the digital calibration method of the PLL frequency response. In this paper, the transfer function of the PLL is deduced, and the critical parameters affecting the transfer function of the PLL are pointed out. Some measures to calibrate the PLL are introduced. The fully-differential PLL is implemented to overcome the noise from the supply and the substrate. The power consumption of the PLL is about 11mW. The modulation data rate can reach 2Mb/s. The low power design consideration will

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be introduced in the building block description.

2 Transfer function of the PLL

2.1 Modulator structure

The structure of the ∑-△ PLL modulator is shown in Fig. 1. A pre-compensation ∑-△ frequency synthesizer[11] is adopted. The PLL is a type-Ⅱ third-order loop. PD/PFD is a phase detector or phase frequency detector. The charge pump (CP) and the voltage-controlled oscillator (VCO) are fully-differential in structure. The programmable divider is based on a pulse-swallow topology. These circuit structures will be discussed in detail in section 3.

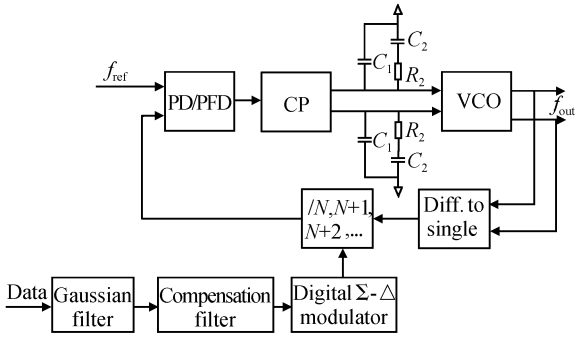

Fig. 1　Structure of the ∑-△ PLL modulator

The current of the charge pump is 25μA. The VCO gain is about 30MHz/V, and the divider number is from 116 to 124. In the second-order loop filter, the values of R_2, C_1, and C_2 are 30.9kΩ, 49.24pF, and 2.92nF, respectively. Using these circuit components, the loop bandwidth of the PLL is 80kHz and the phase margin is 51.8°.

The transfer function of the PLL is deduced below to find the critical parameters in the PLL.

2.2 Transfer function of the PLL

The open-loop transfer function $H_{op}(s)$ of the PLL in Fig. 1 is expressed as

$$H_{op}(s) = I_{cp}H(f)\frac{K_{VCO}}{s} \times \frac{1}{N_{norm}} \tag{1}$$

where I_{cp} is the current of the charge pump, $H(f)$ is the transfer function of the loop filter, K_{VCO} is the VCO gain, and N_{norm} is the average modulus of the divider.

The closed-loop transfer function $H_{close}(s)$ seen from the programmable divider is

$$H_{close}(s) = \frac{I_{cp}H(f)\dfrac{K_{VCO}}{s} \times \dfrac{1}{N_{norm}}}{1 + I_{cp}H(f)\dfrac{K_{VCO}}{s} \times \dfrac{1}{N_{norm}}} \tag{2}$$

Substituting resistor R_2, capacitor C_1 and C_2 into $H(f)$, we get

$$H_{close}(s) = \frac{1}{1 + \dfrac{N_{norm}A_0}{I_{cp}K_{VCO}} \times \dfrac{s^2(1 + sT_1)}{1 + sT_2}} \tag{3}$$

where $A_0 = C_1 + C_2$, $T_2 = R_2C_2$, and $T_1 = R_2C_2 \times C_1/A_0$.

When $sR_2C_2 \gg 1$, the following formula is obtained through simplification:

$$H_{close}(s) \approx \frac{1}{\dfrac{N_{norm}C_1s^2}{I_{cp}K_{VCO}} + \dfrac{N_{norm}(C_1 + C_2)}{I_{cp}K_{VCO}R_2C_2}s + 1} \tag{4}$$

From this formula, we can see that the closed-loop transfer function is sensitive to I_{cp}, K_{VCO}, C_1, C_2 and R_2. According to Ref. [14], the unit gain bandwidth (UGBW) of the PLL should be kept constant to minimize any mismatch with the pre-compensation filter, where the UGBW is

$$\text{UGBW} = \frac{I_{cp}R_2C_2K_{VCO}}{2\pi N_{norm}(C_1 + C_2)} \tag{5}$$

Reference [14] shows that it is enough to keep the product of I_{cp} and R_2 constant. According to the first term in the denominator of Eq. (4), the conclusion is not precise. The matching degree of the PLL and the pre-compensation filter is also dependent on the value of I_{cp}.

The magnitude and phase of the transfer function varies with ±10% change of C_1, C_2, and R_2, as shown in Fig. 2. The magnitude changes by about 1dB. When I_{cp} and K_{VCO} change by ±10%, the magnitude also changes by about 1dB. A

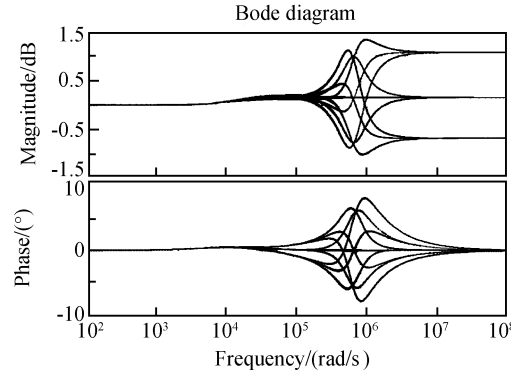

Fig. 2　Closed-loop transfer function as it varies with ±10% change of C_1, C_2, and R_2

change in the transfer function of the PLL can lead to the inter-symbol interface (ISI) and frequency deviation of the modulation signal. Thus the loop must be calibrated.

The current of the charge pump I_{cp} is provided by the bandgap current source to keep its precision. The resistor R_2 and the capacitor C_2 are relatively large. They are off-chip and can be selected relatively accurately. Capacitor C_1 is an on-chip 4-bit switchable-capacitor array. C_1 can be calibrated through the 4-bit digital control. The gain of the VCO, K_{VCO}, is not calibrated in this design. Some calibration methods in the literature can be used and will be implemented in future work.

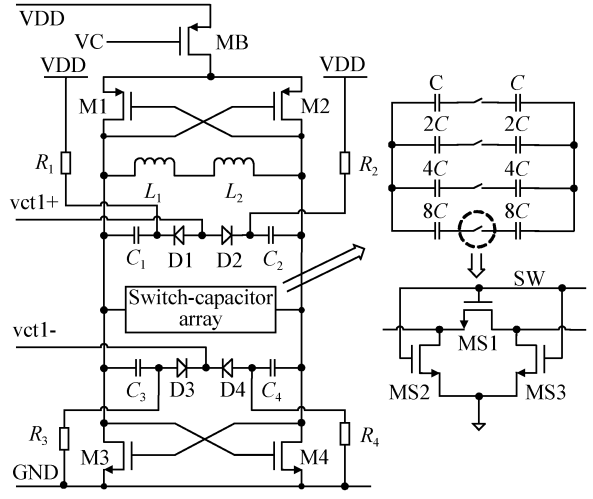

Fig. 3 Schematic of the VCO

3 Building block

In this section, the building blocks, including differentially tuned VCO, fully-differential charge pump, and programmable divider of the PLL, will be introduced.

3.1 VCO structure

The differentially tuned LC-VCO can reduce the effect of the common-noise on the control input signal[15] and extend the tuning range of the VCO. The gain of the VCO, K_{VCO}, can be reduced to improve the phase noise performance[16] with the expanded tuning range. The differentially tuned LC-VCO is adopted, and the binary switchable-capacitor array is implemented to extend the tuning range further. With the expanded tuning range, K_{VCO} is reduced to 30MHz/V.

The structure of the VCO is shown in Fig. 3. The pMOS transistors M1 and M2 and the nMOS transistors M3 and M4 constitute the cross-coupled pairs. They generate negative resistance to cancel the loss in the LC tank. The inductors L_1 and L_2 are circular inductors. Their quality factor is about 8.3 at 2.4GHz. The bias current is provided by the pMOS transistor MB. A pMOS transistor is used because the $1/f$ noise of a pMOS transistor is less than that of an nMOS transistor.

The varactors D1, D2, D3, and D4 are pn-junction varactors. The resistors R_1 and R_2, R_3 and R_4 directly bias D1 and D2, D3 and D4 to the power supply and ground GND, respectively, avoiding the need for complex bias circuits. The switchable-capacitor array is controlled by a 4-bit digital signal. The switch consists of nMOS transistors MS1, MS2, and MS3. This structure assures that the drain and source of the switch MS1 are connected to ground when the switch is on and the turn-on resistance of the switch is reduced.

The differentially-tuned VCO is designed in the current-limited regime[19] to reduce the current consumption.

3.2 Charge pump and loop filter

Here, the structure of the charge pump in Ref. [17], a fully-differential structure, is adopted. Figure 4 shows the schematic of the charge pump and the loop filter. A1 and A2 are unity-gain buffers to keep the input voltage and output voltage of the buffer equal. The amplifier A3 is part of a common-feedback circuit that keeps the common of the VCO's control voltage at the voltage REF. The loop filter is a passive second-order

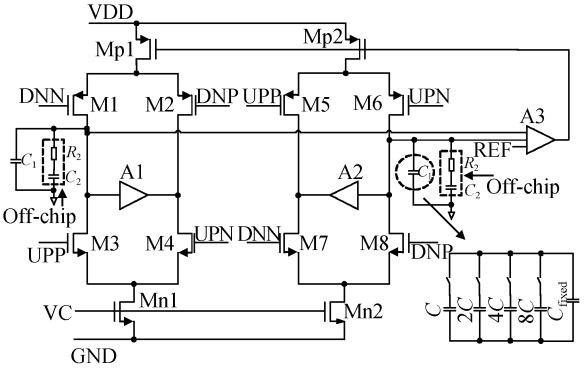

Fig. 4 Structure of the charge pump and loop filter

filter consisting of resistor R_2 and capacitors C_1, C_2. The active loop filter consumes additional power, so a passive loop filter is adopted in this design.

3.3 Frequency divider

Figure 5 shows the structure of the frequency divider, which consists of a ÷ 8/9 prescaler, a fixed-ratio counter P, and a programmable swallow counter S. The adoption of a dynamic divider reduces the power consumption of the phase-locked loop[18]. The E-TSPC ÷ 2/3 divider and ÷ 2 TSPC in Ref. [18] are adopted. The current consumption of the ÷ 8/9 divider is about 1.67mA with a 1.8V voltage supply by simulation. The divider modulus of the swallow divider is from 4 to 12, and the division ratio of the total frequency divider is from 116 to 124. The FF is a synchronizer to reduce the accumulated jitter of the divider.

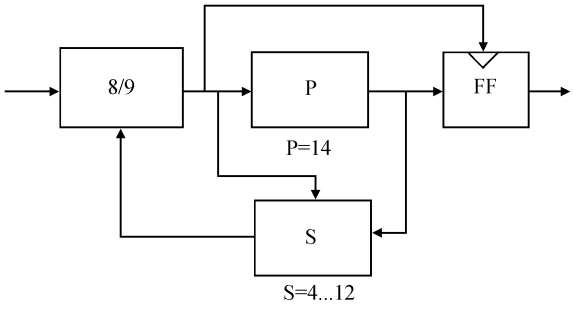

Fig. 5　Structure of the frequency divider

The diagram of the pulse-swallow divider is shown in Fig. 6. In order to reduce the power dissipation of the divider, the method in Ref. [20] is adopted to omit the swallow divider. The state of the fixed-ratio divider (P divider) is detected. When its state reaches the set value S〈1 ∶ 4〉, the 8/9 divider divide ratio changes. Thus, the swallow divider is eliminated to reduce the power consumption. The last two counters of the fixed-ratio divider are realized with a synchronous divider to improve the speed performance.

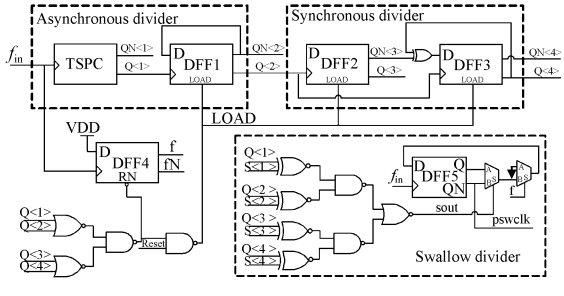

Fig. 6　Structure of the pulse-swallow divider

4 Simulation results

The phase-locked loop is simulated with a 0.18μm 1P6M CMOS process. The layout of the PLL is shown in Fig. 7. The area of the PLL is about 2.1mm × 2.4mm. As can be seen, the area of the test circuit is more than a quarter of the total area.

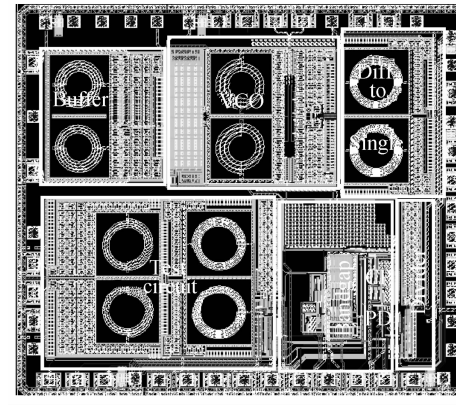

Fig. 7　Layout of the phase-locked loop

The tuning range of the VCO with 4-bit digital control is shown in Fig. 8. The tuning range is from 2.2 to 2.65GHz, covering 450MHz. K_{VCO} is about 30MHz/V. The phase noise of the VCO at 2.415GHz reaches −119dBc/Hz at 1MHz frequency offset from the carrier through simulation.

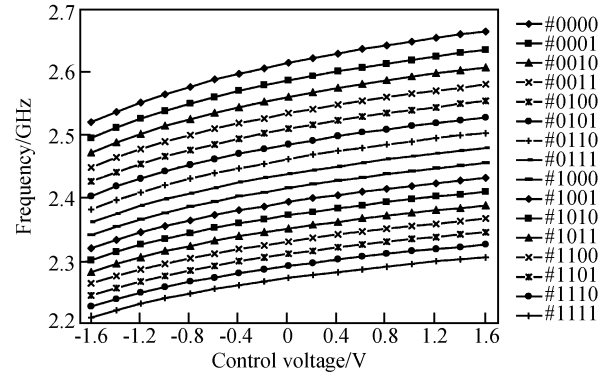

Fig. 8　Tuning range of VCO

The spectrum of the VCO output is plotted in Fig. 9 for a data rate of 1.42Mb/s. The bandwidth

of the digital Gaussian filter is 0.6MHz, and the modulation index is 0.54. The maximum data rate of the modulator is 2Mb/s.

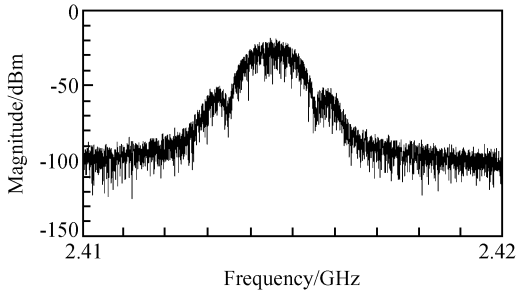

Fig. 9 Simulated RF spectrum

The current consumptions of the VCO, ÷8/9 divider, and differential-to-single converter are about 2.14, 1.67, and 1mA, respectively. The total current consumption of the PLL is about 6.2mA with a 1.8V power supply. The total power consumption is about 11mW. The output buffer's current consumption is about 4mA.

A performance comparison of the PLL designed here to those reported in the literature is listed in Table 1. As can be seen, the phase noise performance is comparable to other designs, and the power consumption is very low. A fully differential structure is adopted in the design to improve immunity to the substrate and power noise and to decrease the power consumption compared to the devices described in Refs. [21] and [18]. Low power and insensitivity to noise make this PLL suitable for portable and system-on-chip (SOC) applications.

Table 1 Performance comparison of the PLL

Reference	Structure	f_0 /GHz	P_{dc} /mW	L@1MHz /(dBc/Hz)	Process
[21]	Singly tuned	2.4	17	−104	0.2μm CMOS/SOI
[18]	Singly tuned	5.035	13.5	−116	0.25μm CMOS
[5]	Fully diff.	1.4	84.05	−120	0.35μm CMOS
[22]	Fully diff.	1.278	16.32	−119	0.5μm CMOS
This work	Fully diff.	2.415	11	−119	0.18μm CMOS

5 Conclusion

A GMSK modulator consisting of a fully-differential low power Σ-Δ frequency synthesizer with a pre-compensation filter is presented in this paper. The transfer function of the type-Ⅱ third-order phase-locked loop is deduced. The fact that the closed-loop transfer function is sensitive to the loop parameters I_{cp}, C_1, C_2, R_2 and K_{VCO} is pointed out. Methods to calibrate I_{cp}, C_1, C_2 and R_2 are introduced to improve the data rate of the modulator. A differential tuned LC-VCO and a fully-differential charge pump are adopted in the PLL design. The circuits are simulated in a 0.18μm 1P6M CMOS process. The tuning range of the VCO is from 2.2 to 2.65GHz, about 18.6%. With the designed PLL, the data rate of the modulator can reach 2Mb/s. The power consumption of the total PLL is only about 11mW. The modulator is suitable for portable and SOC applications with low power and fully differential design.

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应用于 2Mb/s GMSK 调制的 CMOS 低功耗全差分 Sigma-Delta 频率综合器*

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摘要：设计了应用于 GMSK 调制，工作在 2.4GHz，CMOS 全差分的∑-△频率综合器. 调制器中采用预补偿的分数 N 锁相环. 推导了Ⅱ型三阶锁相环的传输函数，并指出影响环路传输函数的重要参数. 介绍了校准重要的环路参数的方法. 锁相环设计中采用差分调节的 LC 压控振荡器和全差分的电荷泵. 设计的电路利用 0.18μm 1P6M CMOS 工艺进行仿真. 由于锁相环的组成模块中采用了低功耗设计，锁相环的功耗仅为 11mW 左右，调制器的数据率达到 2Mb/s.

关键词：互补-MOS 型集成电路；分数-N；高斯滤波最小频移键控；锁相环；∑-△
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