

A 1V, 156.7 μ W, 65.9dB Rail-to-Rail Operational Amplifier by Means of Negative Resistance Load and Replica-Amplifier Gain Enhancement*

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Abstract: A low-voltage, low-power, and high-gain rail-to-rail operational amplifier (OpAmp) is presented. The replica-amplifier gain enhancement technique is applied to improve the DC gain of the amplifier, which does not degrade the output swing and is very suitable for low-voltage applications. In a 0.18 μ m standard CMOS process, a 1V OpAmp with rail-to-rail output is designed. For a load capacitance of 5 pF, simulation by HSPICE shows that this OpAmp achieves an effective open-loop DC gain of 65.9dB, gain bandwidth of 70.28 MHz, and phase margin of 50° with a quiescent power dissipation of 156.7 μ W.

Key words: low-voltage low-power; high DC gain; replica-amplifier gain enhancement; negative resistance load
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1 Introduction

With the scaling down of CMOS technology, supply voltages are continuously decreasing to ensure the reliability of devices. At the same time, portable electronics have been developing rapidly and there is a growing need for low-voltage and low-power performance to decrease the weight and prolong the lifetime of the battery. However, the threshold voltage of devices does not scale proportionally with the supply voltage to avoid a higher off-state transistor current.

Operational amplifiers (OpAmps) are important building blocks in many systems, such as analog-to-digital converters (ADC) and filters. In such applications, high DC gain of OpAmps is necessary to ensure the performance of the whole system. However, some conventional methods, such as cascoding, are not suitable for improving the DC gain because of the output swing limitation in a low-voltage environment. Gain boosting^[1] is an effective method to obtain high speed and high DC gain, but the auxiliary amplifier limits the output swing. Using multiple stages^[2] is another method to improve the DC gain by cascading

more than two stages; however, it often requires frequency compensation, leading to considerable extra power consumption. Positive feedback^[3] and negative resistance load (NRL)^[4,5] techniques are also effective methods for improving the DC gain of low-voltage OpAmps, but the gain cannot be enhanced too much because the stability must be guaranteed. Gain enhancement by current shunt is used in Refs. [6, 7]; however, the gain enhancement factor is limited by the ratio between the parasitic capacitor and the load capacitor.

The DC gain of present OpAmps, which are applied to a sigma delta modulator with a supply voltage below 1V, is about 50dB—still much lower than those of regular voltage environments. The lower DC gain leads to a larger leakage factor of the integrator, which degrades the resolution of the sigma delta modulator. Therefore, it is very necessary to enhance the DC gain of OpAmps further. As shown in previous work, only one technique, such as the positive feedback technique^[3], NRL technique^[4,5], current shunt technique^[6,7] or replica-amplifier (RA) gain enhancement technique^[8], can be used to enhance the DC gain of an OpAmp; however, the resulting DC gain is not high enough to ensure the performance of the

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whole system as that of regular voltage environment because of the limit of mismatch or stability.

In this paper, the replica-amplifier (RA) gain enhancement technique^[8,9] is combined with the NRL technique to achieve higher DC gain of an OpAmp. A basic amplifier with NRL^[10] is used to obtain a moderate gain, with which stability is easily achieved. The RA gain enhancement technique is used to improve the effective open loop further. By using both gain enhancement techniques, the DC gain of the OpAmps is much higher than that obtained with conventional methods.

2 Principle of replica amplifier gain enhancement

Figure 1 shows an RA gain enhancement scheme, which consists of a main amplifier, a coupling amplifier, and a replica amplifier. The theory of this technique was described in Ref. [9]. The feedback network ($\beta_r = \frac{Z_{fr}}{Z_{ir}}$) of the replica amplifier is the same as that of the main amplifier ($\beta_m = \frac{Z_{fm}}{Z_{im}}$). The input signal V_{in} is applied to both the

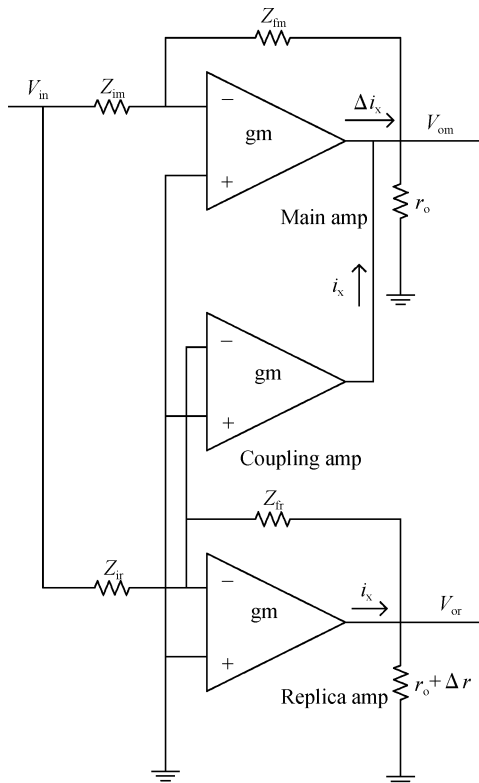


Fig. 1 RA gain enhancement technique

main amplifier and the replica amplifier, and the coupling amplifier is connected between the inverting input of the replica amplifier and the output of the main amplifier. First assume that $\Delta r = 0$. The output of the replica amplifier is derived as

$$V_{or} = -\beta_r \left(\frac{1}{1 + \frac{1 + \beta_r}{A_r}} \right) V_{in} \cong -\beta_r (1 - \epsilon) V_{in} \quad (1)$$

$$\epsilon \cong \frac{1 + \beta_r}{A_r} \quad (2)$$

From Eqs. (1) and (2), it can be seen that V_{or} is very close to the ideal output voltage ($-\beta V_{in}$) with a finite error ϵ , where β is equal to β_m and β_r . The error ϵ is caused by the finite gain of the amplifier, which becomes very low as the supply voltage decreases.

The coupling transconductance amplifier has the same inverting input as that of the replica amplifier. As a result, it produces the same current i_x as that of the replica amplifier, which is injected to the output resistance r_o of the main amplifier so that the output of the main amplifier is close to the ideal output voltage ($-\beta V_{in}$). Therefore, only a small current Δi_x is produced by the main amplifier, which makes the output of the main amplifier even closer to the ideal output voltage. Consequently, the effective gain of the main amplifier is enhanced. The output of the main amplifier is shown in Eq. (3).

$$V_{om} = -\beta_m \left(\frac{1}{1 + \left(\frac{1 + \beta_m}{A_m} \right) \left(\frac{1 + \beta_r}{A_r} \right)} \right) V_{in} \cong -\beta_m (1 - \epsilon) V_{in} \quad (3)$$

$$\epsilon \cong \left(\frac{1 + \beta_m}{A_m} \right) \left(\frac{1 + \beta_r}{A_r} \right) \quad (4)$$

From Eqs. (1) to (4), it is clear that the error is reduced by a factor of $A_r / (1 + \beta_r)$, and the effective gain of the main amplifier is improved by the same factor. However, in practice the actual improvement is limited by the matching between the main amplifier and the replica amplifier. When considering the output resistance mismatch, which is the most dominant, the gain enhancement factor is $r_o / \Delta r_o$ ^[9].

3 Basic amplifier architecture

The basic amplifier architecture, the upper part in Fig. 2, is a current mirror class-AB operational transconductance amplifier (OTA) with an

NRL^[10]. The NRL is formed by $m2a, m2b, m2an,$ and $m2bn$, where $m2an$ and $m2bn$ introduce local positive feedback between the nodes $Vom1+$ and $Vom1-$ to compensate the parasitic resistance of those two nodes. Consequently, the output resistance of the nodes $Vom1+$ and $Vom1-$ becomes very large, and the DC gain of overall OTA is improved. However, in order to keep the stability, only a moderate DC gain can be obtained, which is still very low for some applications, such as ADC or filters. In addition, to obtain higher power-efficiency, higher slew rate, and rail-to-rail output swing, class-AB operation is used.

enhancement technique is introduced in this design. As shown in Fig. 2, the upper part shows the main amplifier, which is a current mirror class-AB OTA with NRL^[10] just as described. The current of the coupling amplifier is injected into the load capacitors by $mc1-mc2$, as shown in dashed line on the upper part. The lower part represents the replica amplifier with a dummy load to match the output resistance of the main amplifier. The replica amplifier is a copy of the main amplifier, and also the replica amplifier can be sized to decrease the power. Unlike other gain enhancement techniques, such as the use of a gain booster, this replica gain enhancement does not degrade the output swing, which is very important in the nanometer era because power supply voltage will be scaled down to some extremely low-voltage.

4 Complete structure of the OpAmp

To improve the DC gain further, an RA gain

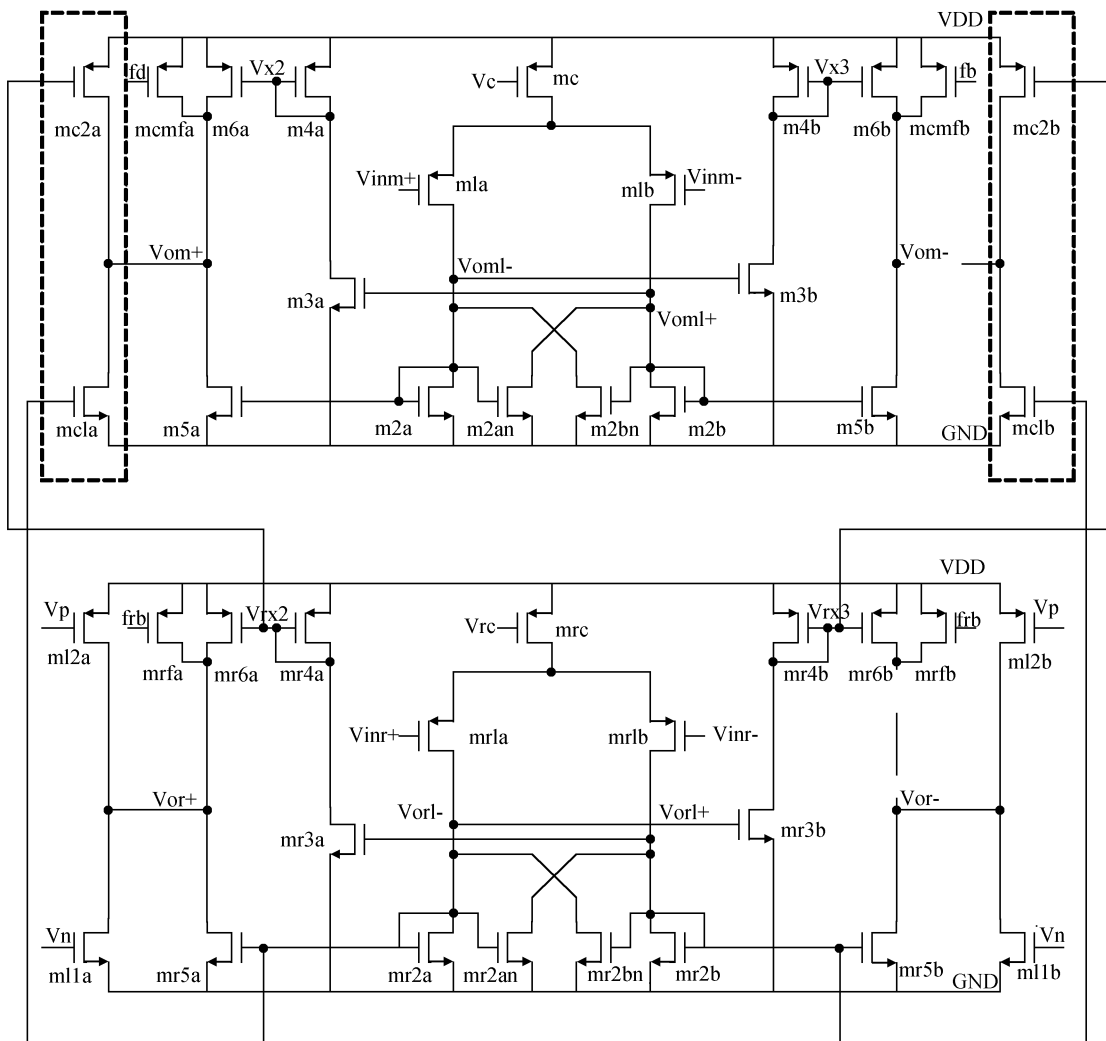


Fig. 2 Complete proposed low-voltage, low-power class-AB amplifier

5 Simulation results

The proposed amplifier is simulated in 0.18 μm standard CMOS technology with $V_{\text{thn}} = 0.421\text{V}$, $V_{\text{thp}} = 0.438\text{V}$, and a supply voltage of 1V. The test circuit is shown in Fig. 3, where the input capacitor and feedback capacitor are both 1pF, and the load capacitor is 5pF.

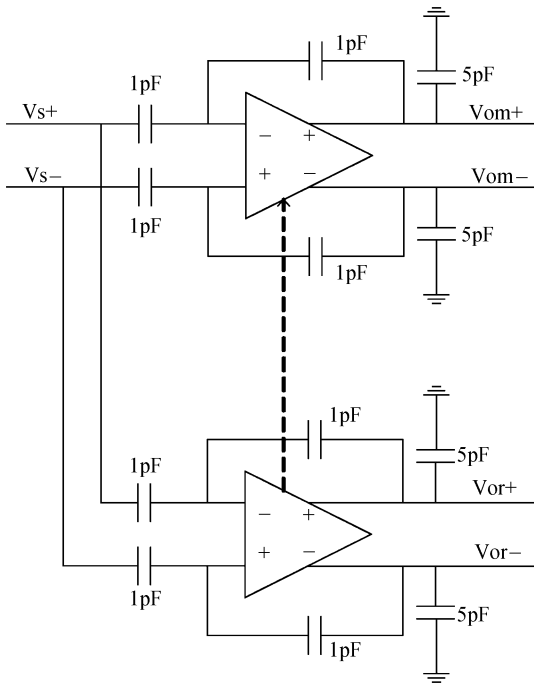


Fig. 3 Test circuit

Figure 4 shows the simulated open loop frequency response. The proposed amplifier achieves a bandwidth of 70.28MHz and consumes about 156.7mW. The DC open loop gain is 65.9dB, and the phase margin is 50 $^\circ$.

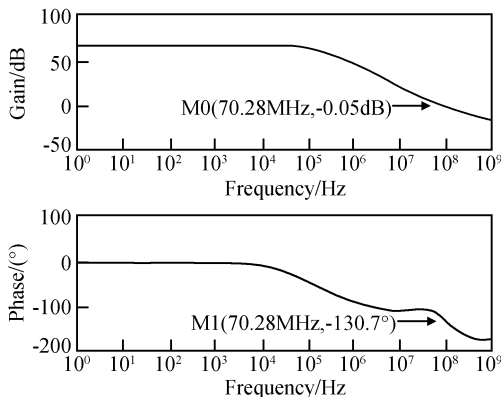


Fig. 4 Open loop frequency response

Figure 5 shows the results of a transient response with a 100mV input signal. The upper signal is the input, and the period of the pulse is 400ns. The lower one is the output signal of the main amplifier. The simulated 0.05% settling time (rising edge) of the proposed amplifier is 63.6ns. Because the phase margin is below 60 $^\circ$, there is an overshoot with a magnitude of 13.98mV. However, this will not affect much, especially in switch capacitor circuits, because the settling procedure is not important as long as the output settles to the required final value^[6].

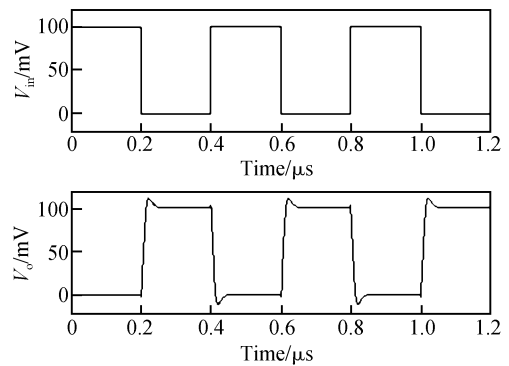


Fig. 5 Transient response

Table 1 shows the simulated performance of the proposed amplifier. The open loop gain of the proposed amplifier is 65.9dB, which is higher than that reported in other works, as shown in Table 1. Although the power of the proposed amplifier is about twice that of the basic amplifier in Ref. [10], it is still very low compared with the power of a two-stage amplifier or class A/AB amplifier, which is about in the order of mW.

Table 1 Performance of the proposed amplifier

Parameters	This work	Liu ^[10]	Gerfers ^[8]	Yao ^[7]	Martin ^[12]
Technology	0.18 μm	0.18 μm	0.18 μm	0.25 μm	0.5 μm
Supply voltage/V	1	1	1.2	0.8	± 1
Capacitor load/pF	5	5	30	18	80
Open loop DC gain/dB	65.9	58.25	52	50	43
Phase margin /($^\circ$)	50	61	92	60	89.5
Gain bandwidth /MHz	70.28	79.53	1.9	1.2	0.725
Settling time/ns	63.6@0.05%	33.6@0.05%	—	2700	29@1%
Overshoot	13.98mV@100mVpp	No overshoot	—	—	—
Power dissipation / μW	156.7	67	200	8	120

6 Conclusion

We have presented a low-voltage low-power rail-to-rail amplifier with high open-loop gain. The basic architecture is a current mirror class-AB OTA with negative resistor load to obtain a moderate DC gain. The RA gain enhancement technique is applied to improve the DC gain of the amplifier further without degrading the output voltage swing. Simulation results show that compared with the basic architecture in Refs. [8] and [12], the open loop DC gain of the proposed OpAmp is increased by over 13dB. The proposed architecture is very suitable for low-voltage switched capacitor circuits, such as ADC or filters, in which high DC gain of the amplifier is very important.

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负阻负载和复制运放增益增强技术相结合的低电压低功耗 高增益端到端输出范围运算放大器*

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摘要: 设计了一种低电压低功耗高增益端到端运算放大器. 为了提高运放的直流增益, 采用了复制运放增益增强技术, 这种技术的特点是在提高增益的同时不影响输出摆幅, 非常适合低电压场合. 该运放采用 0.18 μ m 标准 CMOS 工艺, 工作电压为 1V. 仿真结果表明, 在 5pF 负载电容下所获得运放的直流增益达到 65.9dB, 增益带宽积为 70.28MHz, 相位裕度为 50°, 静态功耗为 156.7 μ W.

关键词: 低电压低功耗; 高直流增益; 复制运放增益增强技术; 负阻负载

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