SOICMOS Integrated Circuit of Laser Range Finding Working at High Temperatures

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Abstract: Modeling analysis of thin fully depleted SOICMOS technology has been done. Using ISETCAD software, the high temperature characteristics of an SOICMOS transistor were simulated in the temperature range of from 300 to 600K, and the whole circuit of a laser range finder was simulated with Verilog software. By wafer processing, a circuit of a laser range finder with complete function and parameters working at high temperatures has been developed. The simulated results agree with the test results. The test of the circuit function and parameters at normal and high temperature shows the realization of an SOICMOS integrated circuit with low power dissipation and high speed, which can be applied in laser range finding. By manufacturing this device, further study on high temperature characteristics of shorter channel SOICMOS integrated circuits can be conducted.

Key words: silicon on insulator; high temperature characteristics; transistor; thin fully depleted
PACC: 7300; 7360J **EEACC**: 2520D; 2530F; 2570D
CLC number: TN386.1 **Document code**: A **Article ID**: 0253-4177(2007)02-0159-07

1 Introduction

Silicon on insulator (SOI) is a new material structure with a buried insulating layer. CMOS circuits made on it totally avoid the latch-up effect that is stimulated by bulk silicon at high temperatures. The devices made on it do not use a large-area insulating pn junction, and the leakage current of the devices is low and does not change too much with temperature, so the threshold voltage does not change too much with temperature[1,2]. However, as the range of uses of such devices has been extended unceasingly, the working temperature has become an important factor influencing the devices' characteristics. By experimenting on devices at high temperatures, we can improve the upper limit of the operation temperature of the circuits and meet the demand for using in high temperature environments.

Analysis and study of SOI characteristics at the circuit level at high temperatures have not been reported yet. In this paper, a 1.2μm FD SOICMOS circuit is simulated theoretically and studied experimentally. Firstly an analysis model, which meets the deep sub-micron requirements, is set up. The high temperature characteristics are simulated with the software ISETCAD[3] for a three-dimensional device to get the output characteristics of an SOI transistor at various temperatures. Then the simulation results are verified and analyzed through experiments. Finally a laser range finding circuit with full function and parameter requirement is tested at normal and high temperatures. Test results are given.

2 Setting and analysis of structure model

2.1 Structure model

The inverter structure of a laser range finding circuit is formed by FD SOI n-type and p-type transistors. Its cross section is shown in Fig.1.

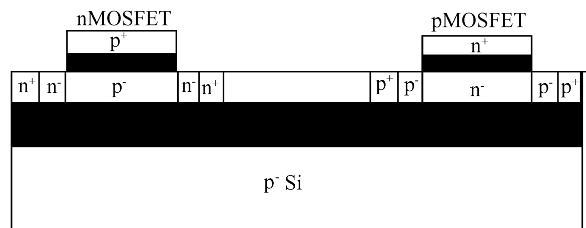

Fig.1 Cross section of a typical CMOS inverter structure in SOI technology

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Received 6 June 2006, revised manuscript received 26 September 2006
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2.2 Modeling analysis

In setting the model, ISETCAD three-dimensional device simulation software is used. Physical models such as flow liquid energy transform, thermodynamics, quantum mechanics, carrier mobility, and generation-recombination are applied, and then a coupling algorithm solves the equations.

The self-heating effect is a very important factor that affects the characteristics of a device at high working temperatures. For SOICMOS devices, the heating effect is intensified in the following way: the thermal isolation effect of buried dioxide hinders the power dissipation transforming from the active area in silicon film. Thus the temperature in the device's crystal lattice increases, the carrier mobility and saturation rate decrease, the heating resistance decreases, and the thermal capacity increases. As a result, the heating effect is intensified. Model analysis is focused on the carrier mobility of FD SOICMOS n^- and p^- areas. With the concern of high operation temperature, the correct expressions and various parameter data introduced are found according to FD SOICMOS processing requirements.

The mobility includes surface and bulk mobility. The surface mobility is influenced partly by surface phonon scattering and surface roughness, but the bulk mobility is influenced by the two cases of high electric field and low electric field. To obtain mobility data which approach real data, when setting a carrier model the combined effects are considered over the surface and bulk mobility. In the bulk mobility we pay attention to high and low electric fields. This combined effect is obtained using Mathiessen's rule. In this paper, we adopt the enhancement mode of the Lombardi model because in the channel area, n^- and p^- areas of MOSFETS influencing each other become serious between interface carrier and semiconductor/insulator for the action of a high lateral electric field, and so the mobility recession caused by surface phonon scattering and surface roughness must be written into the model. We adopt the Phumob model when calculating the bulk mobility at low electric field. This model can not only describe correctly the lattice temperature influence on carrier mobility, but also consider the influence such as electron-hole scattering, ionization and accumulation of impurities. The drift rate of carriers reaches a saturation rate that doesn't increase with electric field strength at high electric field, and thus the expression of the mobility must be corrected in high electric field conditions.

2.3 Geometric and physical parameters of device

We use ISETCAD three-dimensional device simulation software to set up the model and correct the model expression, and each geometric and physical parameter is given. An SOICMOS standard inverter structure unit with a couple of complementary MOS transistors as shown in Fig. 1 is solved using the coupled algorithm, and the geometric and physical parameters are simulated, analyzed, and designed optimally. Finally, optimal geometric and physical parameters of the SOI CMOS inverter simulation are obtained, as shown in Table 1.

Table 1 Geometric and physical parameters of SOICMOS inverter simulation

	nMOS	pMOS
Channel length/μm	1.2	1.2
Channel width/μm	5	10
Channel doping concentration/cm^{-3}	Boron, 3×10^{17}	Arsenic, 3×10^{17}
Drain (source) doping concentration/cm^{-3}	Arsenic, 5×10^{19}	Boron, 5×10^{19}
Extend area doping concentration of drain (source)/cm^{-3}	Arsenic, 5×10^{18}	Boron, 5×10^{18}
Poly-silicon gate doping concentration/cm^{-3}	Arsenic, 1×10^{19}	Boron, 1×10^{19}
Drain (source) junction depth/μm	0.12	
Gate oxidation thickness/nm	12	
Buried oxidation thickness/nm	100	
Silicon film thickness/nm	100	
Substrate film thickness/μm	300	
Sub-gate doping concentration/cm^{-3}	Boron, 1×10^{16}	

3 Simulation of transistor and laser range finding circuit

3.1 Simulation of transistor

The sub-threshold output characteristics of a 1.2μm FD SOICMOS circuit with n-type and p-type transistors at various temperatures are simulated and analyzed based on the setting model, with emphasis on the temperature influence on the leakage current. The simulated results of the n^--type transistor is shown in Fig.2.

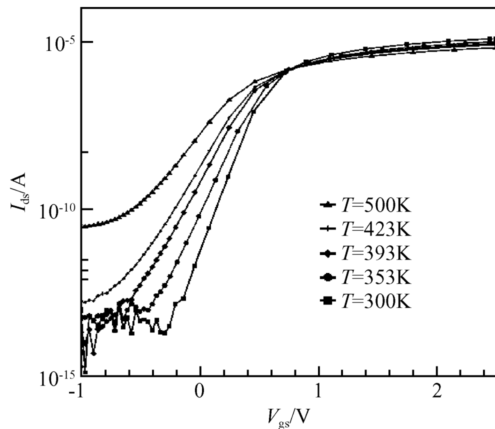

Fig. 2 Sub-threshold characteristics of an FD SOI nMOSFET as a function of temperature

From Fig.2 we conclude that as the environment temperature increases, the leakage current of the n-type transistor increases accordingly. Concurrently, the subthreshold gradient of the SOI nMOS decreases gradually, and the change is very obvious. The leakage current of the n-type transistor is 3.021×10^{-12} A/μm at 300K operation temperature ($V_{gs} = 0$). It increases to 5.281×10^{-9} A/μm when the temperature rises to 500K, but it can still be used. The leakage current will increase continually as the temperature further increases. The MOSFET cannot turn off normally when the leakage current I_{leak} approaches the turn-on current, which leads to the failure of the circuit. The leakage current of the n-type transistor increases as the temperature increases, due to the following reasons: the intrinsic carrier concentration n_i increases rapidly when the temperature increases, the mobility of the minority-carrier decreases, and the effects of short channel and DIBC (drain-induced-barrier-lowering)[4] intensify.

From Fig.2 we also conclude that there exists a point of zero temperature coefficient, which represents the gate voltage of +0.766V. The drain/source current is 1.617×10^{-6} A/μm when the SOI nMOSFET works at this gate voltage, which changes with the temperature. This is because that thermal accumulation in a bulk device results in an increase in the crystal lattice temperature, while the carrier mobility and saturation rate decrease, the thermal resistance decreases, and the thermal capacitate increases. As a result, the heating effect is intensified and the leakage current decreases. Two effects of contradiction lead to the generation of a point of zero temperature coefficient, with the benefit that the device works normally at high temperatures.

The output drain characteristics of an FD SOI nMOSFET as a function of temperature based on the model are shown in Fig.3. From Fig.3 we can draw two conclusions. The first is that the output drain characteristics buckle slightly for single output, because the device is working at saturation and the drain voltage is no more than 3V. Carrier acceleration at the drain depleted area in lateral high electric field leads to collision ionization as the drain voltage increases, but this ionization extent is very weak. As a result, the bulk electric potential approaching the source area increases slightly, the threshold voltage decreases a little, and the drain current goes slightly up, so the output drain characteristics curve buckles. The second is that the output drain current for a group of curves decreases as the environment temperature increases because thermal accumulation in the

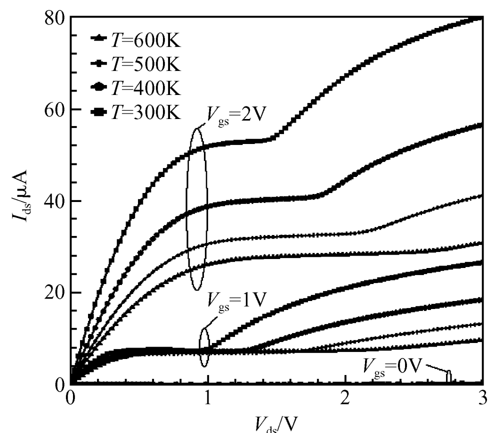

Fig.3 Drain characteristics of an FD SOI nMOSFET as a function of temperature

bulk device leads to an increase in the crystal lattice temperature, a decrease in the carrier mobility and saturation rate, a decrease in the thermal resistance, and an increase in the thermal capacitate. As a result, the heating effect is intensified, and the drain current decreases. Because of the combination of ionization of collision and thermal accumulation, the rise and fall of the drain current cancel each other out, and thus the output drain current characteristics curve is very gentle at 300 and 600K. As a result, the device can work normally at high temperatures.

We simulate the laser range finding circuit to determine whether the logical functions correspond to the design demand. The high-temperature characteristics of the transistor were analyzed using ISETCAD software, and the physical effects, which affect the sub-threshold and drain output characteristics at high working temperature, were explained. It was concluded that the comprehensive effect on the transistor enables the device to work at high temperatures. This is a basic theory for the operation of 1.2μm SOICMOS IC at high temperatures, and therefore stability and better sub-threshold and drain output characteristics at high working temperature can be obtained in actual manufacture. It was tested, as will be discussed in section 4.

3.2 Simulation of a laser range finding circuit

A schematic diagram of the fully depleted SOICMOS laser range finding circuit is shown in Fig.4. To verify the circuit design, a laser range finding circuit was simulated using Cadence and Verilog software. The optimization circuit was obtained by optimizing each parameter such as resistance and the ratio of width and length of channel. The simulated results are shown in Fig.5.

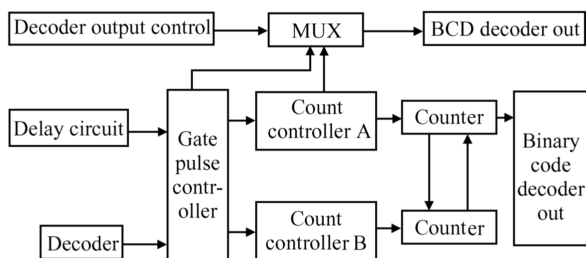

Fig.4 Schematic diagram of fully depleted SOICMOS laser range finding circuit

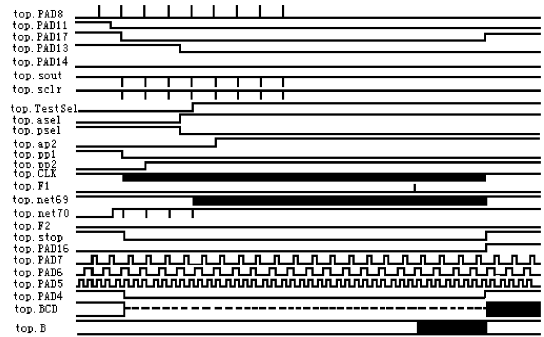

Fig.5 Simulation waveforms of fully depleted SOICMOS laser range finding device

From Fig.5, when the signal is input, the input signal is shaped by the delay circuit to become a signal of unit pulse width. Then it is decoded by the decoding circuit, and then measuring pulse counts are transferred to the multichannel demultiplexer via the gate pulse controller. Based on the requirements for the signal of the multichannel demultiplexer, a five-digit binary code is selected from an eighteen-digit binary code of the counter and is then input to the BCD-decoder-out. Then it is decoded as a four-digit BCD output code. Thus the logical function of the circuit meets the requirements of design.

4 Testing results and analysis

4.1 Technology processing

Concerning the requirements of high speed and low power, 1.2μm FD SOICMOS processing technology with single-layer poly-silicon and metal is adopted to realize this circuit. The main processes are as follows: field region oxidation, gate pre-oxidation, implanting in channel, gate oxidation, poly-silicon deposition, LDD structure, implanting in source and drain regions, and metalation, in which T_{si}: 190nm, T_{BOX}: 375nm, substrate p⟨100⟩, transistor W/L is 5/1.2, the thickness of the gate oxidation is 12nm, and the implanting in n-type is (BF_2, 70keV, 1.4×10^{14}) and p-type is (P_{31}^{+}, 70keV, 3.3×10^{15}). The "sandwich" structure of nitrogen-oxide-gate + hydroxide-gate + nitrogen-oxide-gate were made using the technique of combining the nitrogen-oxide with the hydroxide. The influence of the Si/SiO_2 interfacial state on device characteristics and threshold voltage must be considered in processing the thin gate[5]. High-

quality thin-gate oxidation was realized with a low interfacial state, high breakdown voltage, fewer defects, and uniform thickness[6,7]. By wafer processing, the integrated circuit chip is realized as shown in Fig. 6.

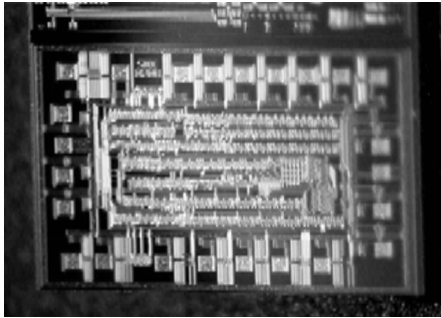

Fig. 6 Chip of laser range finding device

4.2 Test and verification

The sub-threshold and output characteristics of the 1.2μm FD SOICMOS circuit with n-type transistor were tested using semiconductor integrated circuit measuring instruments. The test results are shown in Fig. 7 and Fig. 8. The test results agree with the simulation results, demonstrating that the model is reasonable.

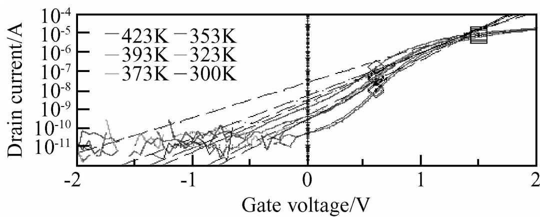

Fig. 7 Subthreshold characteristics of an FD SOI nMOSFET as a function of temperature

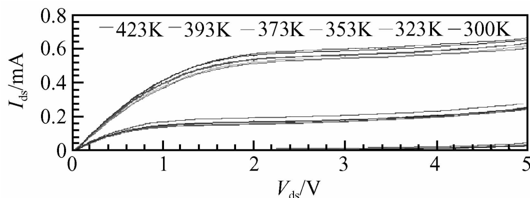

Fig. 8 Drain characteristics of an FD SOI nMOSFET as a function of temperature

The drain current, as shown in Fig. 7, goes up slowly compared with the simulated result as shown in Fig. 2. This is because the concentration in the channel is below the simulated value in actual manufacture, resulting in reduced electric-field strength, carrier deviation from the front interface, reduction in the capacity for gate control, and an increase in the sub-threshold gradient, which is above the ideal value and not cliffy as in the ideal condition. Simultaneously, when the channel carriers were not depleted thoroughly, the sub-threshold gradient also increased, further leading to a slow increase in the drain output current.

The output drain characteristics as shown in Fig. 8 don't buckle slightly as in the simulated result shown in Fig. 3. This is because the circuit was designed using the technique of bulk contact in a floating body electric potential zone. Even if a few hole carriers gather in the floating body electric potential zone, it can be led to the outside. The bulk electric potential keeps a stable value approaching the source zone of the device, so the curve doesn't buckle.

4.3 Analysis of test results

From the above characteristic curves we can draw some conclusions. The single-transistor temperature characteristics of the device remain very good even if the temperature is above 150℃, and the test curve group doesn't scatter. These cannot be realized for bulk silicon devices. The upper limit of reliable operation temperature of the similar bulk silicon circuit is 80℃ under normal conditions, but the similar SOI circuit can break down the restrictions of high operation temperature.

The delay transient characteristics of ring oscillators were measured with 3.3V supply voltage. The ring oscillators consist of a 101-stage NAND gate based on an SOICMOS standard inverter structure with a couple of n-type and p-type transistors as shown in Fig. 8. The delay transient characteristics of the ring oscillators were measured at 300, 323, 353, 373, 393, and 423K, and then the combined curve was formed. The total propagation delay is 111ns. The measured results show the realized device with small direction electric field, thick inversion layer, and low surface scattering, so the device has higher carrier mobility and bigger grid-anode transconductance. The parasitic capacitance mainly comes from the capacitance of buried oxidation layer and small wiring capacitance, so the device speed is much faster than that of the similar dimensional bulk silicon

device. Similarly, because the smaller area surrounding the drain/source of the transistor is depleted, the operation speed of the device was improved. From Fig. 9 we conclude that the delay transient characteristics curve at high temperature is not changed from the curve at normal temperature, which is as we expect for a manufactured device. We found that the voltage transient characteristics of the inverter began to degrade when the operation temperature of the inverter was above 220℃ (516K), and the low electrical level of the output didn't reach 0V. The device changed from full-depleted to partly-depleted, which has exactly the same temperature characteristics as the bulk silicon device. The delay transient characteristics of the ring oscillators we measured at 150℃ are the same as those we obtained at normal temperature. Obviously, the delay transient characteristics of ring oscillators are very steady, so there is much room yet for the device we manufactured to have improved high operation temperature.

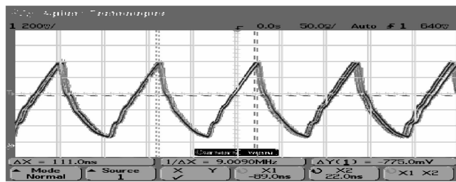

Fig. 9 Delay transient characteristics of ring oscillator circuit at various temperatures

In SOICMOS circuits, we can use a CMOS inverter to realize a circuit with complete function and parameters according to the need of function and logic. The characteristics of the laser range finding circuit we manufactured were tested at high temperatures. Test results show that the circuit has the functions of self-checking, objective-measuring, counter-overflowing, full output of BCD code, and laser range finding with a 3.3V supply voltage at 150℃. Its main electric parameters are as follows: the operation frequency is measured using an Agilent 54622A oscilloscope and HP3325B pattern generator, with a value of more than 120MHz; output cut-off current is no more than 1μA; output high-level V_{DD} is -0.001V; output low level is no more than 1mV; its static power dissipation is 0.3mW; and dynamic power dissipation is 10mW. The electric parameters are steady with little change between the parameters at high temperature and those at normal temperature. Thus the circuit we realized can be used in systems that require high precision and a wide temperature range.

5 Conclusion

In this paper, the setup of a model for analyzing SOICMOS device at high temperatures has been presented. The simulation results agree with the test results. The function and parameters of a circuit for laser range finding we manufactured were tested at 150℃. The test results show that we realized a practical circuit with low power dissipation (one-tenth that of the bulk silicon circuit) and rapid operation speed (4 times that of the bulk silicon circuit), which can be applied in laser range finding. The operation temperature has been improved 2 times compared with that of the bulk silicon circuit, which has a reliable working temperature of 80℃.

This model can guide the further study of high-temperature characteristics of shorter channel SOICMOS integrated circuits. We have studied the high-temperature characteristics of an SOI device with a 0.18μm channel. A new structure of a DSOI-AlN device, in which an AlN buried layer under the channel is used to replace the dioxide in the SOI device, is analyzed to get the high-temperature characteristics[8] and a guiding conclusion is made.

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一种高温工作的激光测距SOICMOS集成电路

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摘要: 基于薄膜全耗尽SOICMOS工艺,进行了建模分析,在300～600K温度范围内,利用ISETCAD软件对SOICMOS器件单管高温特性进行了模拟分析,同时利用Verilog软件对激光测距电路进行了整体仿真.通过工艺流片,实现了一种电路级具有完整功能和参数要求的高温工作的激光测距SOICMOS集成电路.通过实际测试表明模拟结果与之相吻合,同时通过对整体电路结果功能和参数在常温和高温下的测试,表明该电路功耗低、速度快,可满足激光测距电路的要求.该电路的研制,对进一步开展高温短沟道SOICMOS集成电路的研究具有一定的指导意义.

关键词: 绝缘体上的硅;高温特性;单管;全耗尽

PACC: 7300;7360J **EEACC:** 2520D;2530F;2570D

中图分类号: TN386.1 **文献标识码:** A **文章编号:** 0253-4177(2007)02-0159-07

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2006-06-06收到,2006-09-26定稿

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