IC Implementation of a Programmable CMOS Voltage Reference*

Zhang Ke, Guo Jianmin, Kong Ming, and Li Wenhong†

(*State Key Laboratory of ASIC & System, Fudan University, Shanghai* 201203, *China*)

Abstract: A new approach for the design and implementation of a programmable voltage reference based on an improved current mode bandgap voltage reference is presented. The circuit is simulated and fabricated with Chartered 0.35μm mixed-signal technology. Measurements demonstrate that the temperature coefficient is $\pm$36.3ppm/℃ from 0 to 100℃ when the VID inputs are 11110. As the supply voltage is varied from 2.7 to 5V, the voltage reference varies by about 5mV. The maximum glitch of the transient response is about 20mV at 125kHz. Depending on the state of the five VID inputs, an output voltage between 1.1 and 1.85V is programmed in increments of 25mV.

Key words: voltage regulation modules; current mode bandgap voltage reference; temperature coefficient; power supply rejection ratio; programmable voltage reference

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1 Introduction

Precision voltage references are critical components in many applications such as analog to digital converters (ADCs), digital to analog converters (DACs), DC-DC converters, and portable devices and instruments because they determine the accuracy of these systems.

Digital controllers used in voltage regulation modules (VRMs) have many advantages over analogue controllers due to their low quiescent power, immunity to analog component variations, ease of integration with other digital systems, ability to implement sophisticated control schemes, and potentially faster design process. A simplified block diagram of the key functions of this controller requires a programmable voltage reference and a fixed bandgap voltage reference[1]. They are used to set the output voltage(s) of the VRM, and they are also made available off chip for ancillary uses.

Previous research has focused on the development of a programmable voltage reference in a CMOS process that could be further developed to meet the requirements of an integrated digital controller[2,3]. Reference [2] presents a method based on IPTC and INTC generators and a scaling circuit. However, it is based on an operational amplifier and can only produce two or three variable voltage references. Unlike conventional bandgap circuits, Reference [3] presents MOS transistors operating in the subthreshold region instead of bipolar transistors to generate PTAT and IPTAT currents. Use of the current conveyor allows the circuit to operate at a lower supply voltage and generate variable as well as multiple voltage references. However, the PSRR is not good enough for practical implementations.

Therefore, the objective of this research is to design, develop, and test a programmable bandgap voltage reference to be implemented in a fully customizable mixed-signal ASIC in a 0.35μm CMOS process that is fully compliant with the Intel VRM9.0/9.1 VID specification shown in Table 1 and can be used in a VRM ASIC for an Intel Pentium® III processor[4,5]. It is also expected that it will find use in VRM10.0/10.1 after the improvement of the Intel Pentium® IV processor.

2 Improved current mode voltage reference

A conventional op-amp based bandgap voltage

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† Corresponding author. Email: wenhongli@fudan.edu.cn

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Table 1　VRM9.0/9.1 voltage identification(VID)table

Processor pins(0 = low,1 = high)					V_{cc}
VID4	VID3	VID2	VID1	VID0	/V
1	1	1	1	1	Off
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

reference circuit[6~9] generates a fixed output of around 1.2V, which makes the circuit unable to provide variable voltages from 1.1 to 1.85V. To overcome this limitation of the conventional architecture, the design of a current-mode (CM) architecture CMOS bandgap voltage reference with arbitrary voltage value achieved by setting the resistor value is presented[10,11].

This paper demonstrates an improved CM bandgap reference with high PSRR. The basic idea is to have a low voltage cascode current mirror biased by the output of the op-amp, as shown in Fig. 1, which decreases the current distortion compared with the basic pMOS current mirror in Refs.[10,11], makes the power dissipation lower than that of the common cascode current mirror in Ref.[12], feeds the supply noise directly into the feedback loop, and modulates the gate with respect to the source terminals of the pMOS current mirror. This would reduce the variation in drain current from the pMOS and allow the reference node to be less sensitive to the supply noise. Moreover, long-channel devices are chosen to minimize the channel-length modulation effect.

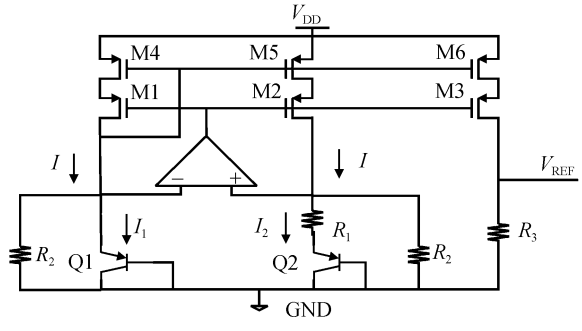

Fig.1　Improved CM bandgap reference

The complete circuit consists of a bias circuit, a start-up circuit, an operational amplifier, and the core block including two pnp bipolar junction transistors (BJTs), which are shown in Fig.2.

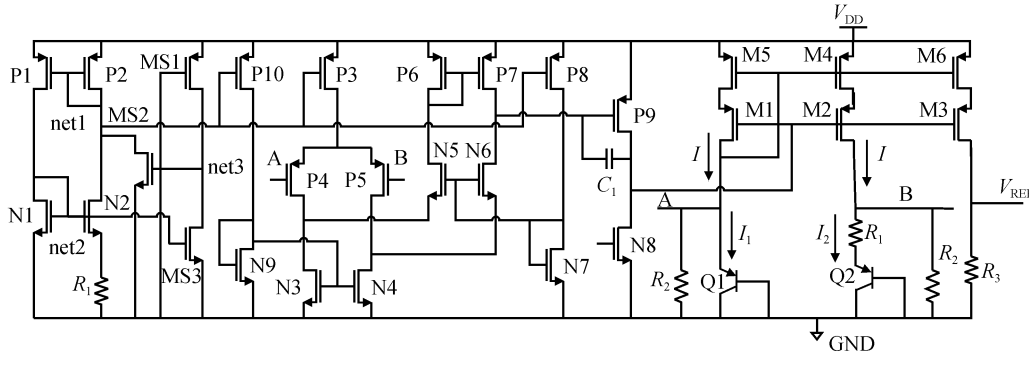

Fig.2　Complete circuit of improved CM bandgap voltage reference

2.1 Design of operational amplifier

As shown in Fig. 2, P4 and P5 consist of the differential input pair of the op-amp. Similar to conventional bandgap references, the offset voltage V_{os} of the amplifier is one of the main factors that lead to drifts and the accuracy of the reference voltage V_{REF}. According to Eq. (1), V_{os} is amplified by a ratio factor of R_3/R_1.

$$V_{REF} = IR_3 = \frac{R_3}{R_2}\left[V_{EB} + \frac{R_2}{R_1}(\Delta V_{EB} + V_{os})\right] \quad (1)$$

The offset voltage V_{os} depends mainly on the effect of the mismatches of transistor size and threshold voltage of the input differential pair of the op-amp. V_{os} is also relative to the gain of the amplifier in the open loop. To reduce V_{os} and depress the disturbance due to the fluctuation of the power supply resulting from abrupt interference from the surroundings, it is essential to improve the DC gain and PSRR of the amplifier as much as possible. In addition, sufficient consideration for symmetrical and compact layout of the circuit system is absolutely necessary.

2.2 Start-up circuit

As shown in Fig. 2, the start-up circuit is composed of MS1, MS2, and MS3. It provides start-up current for the op-amp. When the circuit operates in the zero-current state, the gate voltages of P1, P2, are pulled high and close to the supply V_{DD}. The gate voltage of N1, with N2 the same as MS3, is pulled low, so that MS3 is cut off, and the gate voltage of N2 is pulled high. This turns on N2 to inject current to the bias circuit. With the increase of the gate voltage of N2, the drain voltage of MS3 pulls low and cuts off MS2.

The W/L ratio of MS1 is critical since the loop of the reference core is destroyed if MS2 cannot be completely cut off after start-up. To ensure a complete cut-off of MS2, the W/L ratio of MS1 is chosen to be much less than one.

3 Programmable voltage reference

The bandgap output voltage is programmable by scaling up or down the output current I. This can be done easily by changing the W/L of M3 and M6 in Fig. 1, or it can be programmed digitally by adding the binary weighted currents using a current DAC as shown in Figs. 3 and 4.

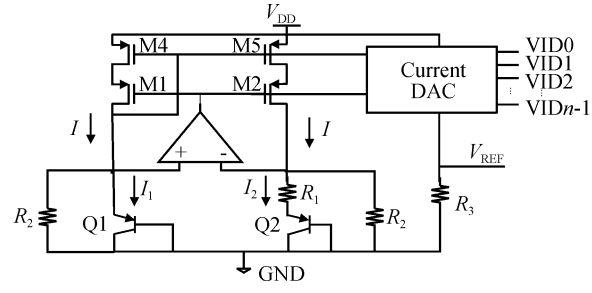

Fig. 3 Schematic for programmable CM bandgap reference

However, Reference [3] used a 2-to-1 MUX to scale up or down the current I. This has a drawback that it has a large glitch of about 100mV due to the different state "0" or "1" of the VID input, especially if the input states change from 10000 to 01111. Figure 4 shows a proposed deglitching circuit with an efficient pMOS glitch protection transistor. The digital glitch noise occurs at the gate voltage of P3, and P4 is protected at the pMOS transistors P5 and P6 that work in the saturation state. With the proposed circuit,

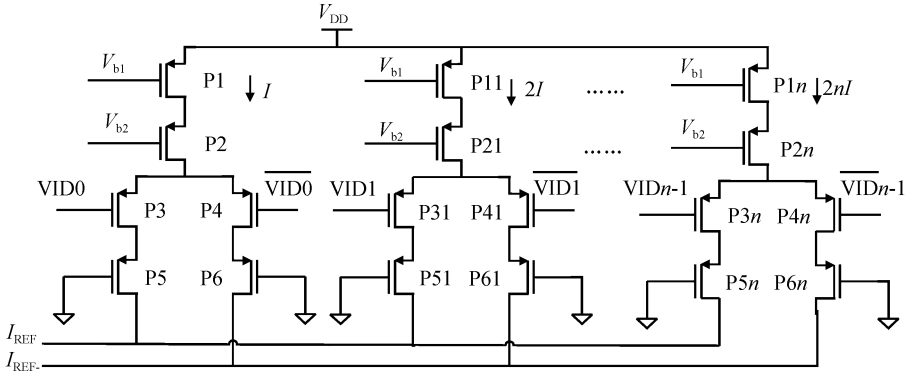

Fig. 4 A 5-bit current DAC for the PVR

the digital glitch noise can be reduced to the order of 10 or 20μV. Compared to the current DAC in Ref.[3], the desired match and deglitching performance is much better.

The mismatch of the current I is a critical problem. The MOSFETs controlled by the bias voltages V_{b1} and V_{b2} work in saturation while a leg of current is turned on. When the channel-length modulation effect is ignored, the square equation for MOSFETs in the saturation region is

$$I = \frac{\mu C_{ox}}{2} \times \frac{W}{L}(V_{gs} - V_{th})^2 \qquad (2)$$

Thus the variable current ΔI can be given by

$$\frac{\Delta I}{I} = \frac{\Delta(\mu C_{ox})}{\mu C_{ox}} + \frac{\Delta W}{W} - \frac{\Delta L}{L} - \frac{2\Delta V_{th}}{V_{gs} - V_{th}} \qquad (3)$$

where μ, C_{ox}, and V_{th} are technology-dependent constants. From Eq. (3), large W and L mean good match performance. However, a large parasitic capacitor will inevitably influence the speed of the current DAC. In practical implementation, a trade off should be taken into account. Reasonable W, L, and V_{gs} will decrease the current distortion.

4 Results

Figure 5 shows the layout drawing and photograph of the programmable CMOS voltage reference. The chip is fabricated with Chartered 0.35μm CMOS technology. The chip area of the core cell is about 357μm×300μm. In Fig. 5, the area of the thermometer decoder current DAC block occupies about 50% of the total area. The power consumption of the reference is only about 2.5mW with a 3.3V power supply.

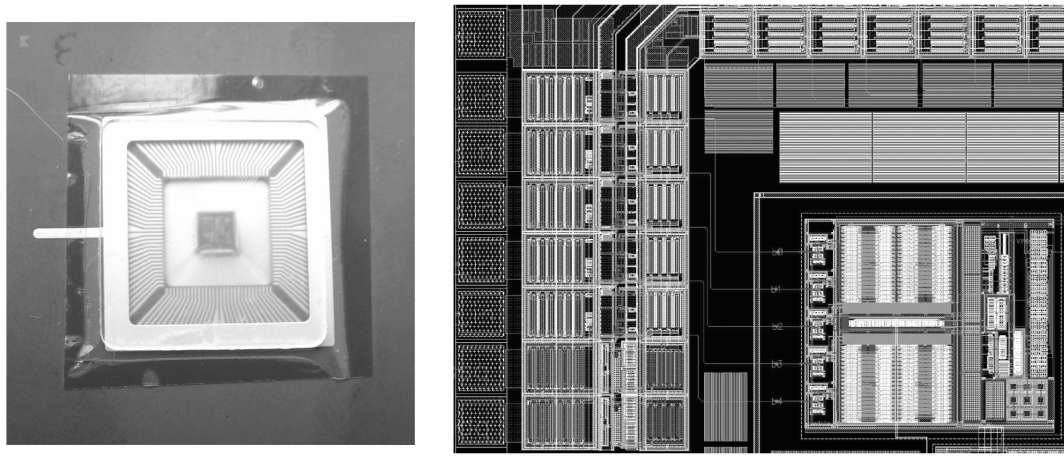

Fig. 5　Chip layout drawing and photograph for the PVR

It was tested at temperatures from 0 to 100℃ and supply voltages from 2.7 to 5.5V. Figure 6 shows a plot of the simulated and the actual measured output voltage over temperature with a 3.3V power supply. The simulation results from the HSPICE demonstrate that the TC is about 16.2ppm/℃ from 0 to 100℃ and the PSRR is −83.2dB at 1kHz.

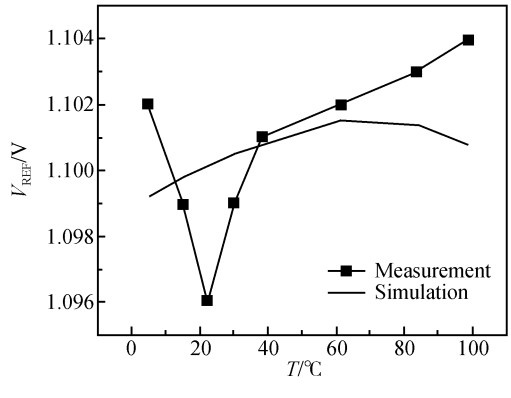

Fig. 6　TC of the voltage reference when VID = 11110

With no trimming scheme, the temperature performance of the measured results is still reasonably good. At V_{DD} = 3.3V, VID = 11110, the output varies by ±4mV (±36.3ppm/℃) from 0 to 100℃. As shown in Fig. 8, the maximum measured error of the reference is less than 0.6% at different states of the VID inputs.

The PSRR was measured by noting how the output voltage changed as the supply voltage var-

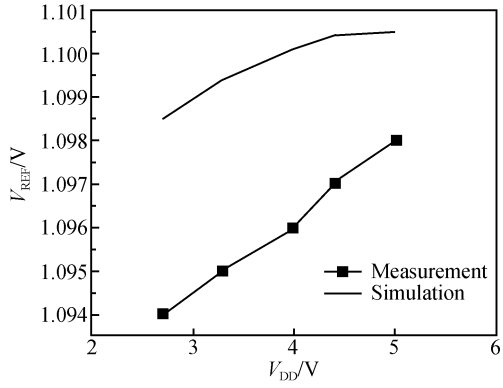

Fig. 7 PSRR of the voltage reference when VID = 11110

ied from 2.7 to 5V. In this supply range, the output voltage varied by 5mV at VID = 11110. Figure 7 shows the measurement results. Each voltage reference relative to the VID has the same voltage variance of about 5mV. As shown in Fig. 9, the maximum measured error of the reference is less than 0.8% at different states of the VID inputs.

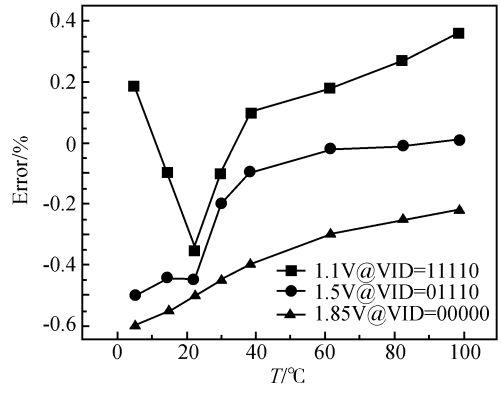

Fig. 8 Typical error versus temperature

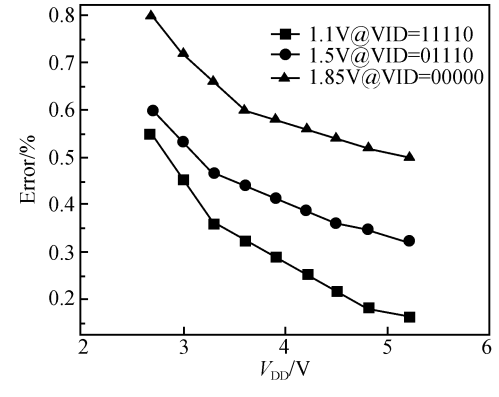

Fig. 9 Typical error versus supply voltage when T = 27℃

The transient response of the programmable bandgap reference is shown in Fig. 10. An FPGA board (Xilinx virtex-II pro) was used to generate the VID[4 : 0], and the frequency of VID0 was 125kHz. The result obtained with a Tektronix TDS5032 Digital Phosphor Oscilloscope is shown in Fig. 10. The maximum glitch of the PVR is about 20mV, and the steps are 25mV.

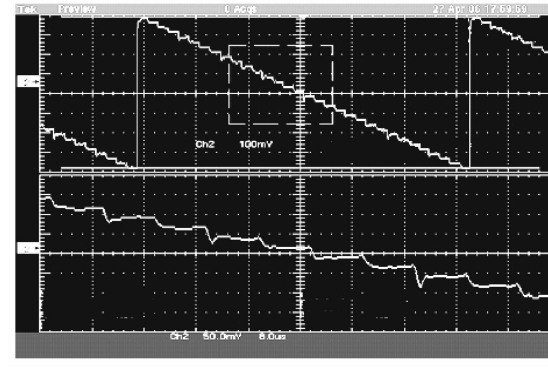

Fig. 10 Transient response of the programmable bandgap reference (VID0 at 125kHz)

5 Conclusion

Previous references do not provide the measurements of the programmable voltage references. A new approach for the implementation of a programmable voltage reference based on a CM bandgap voltage reference has been used in a DC-DC digital controller successfully. The TC of the reference is ±36.3ppm/℃ from 0 to 100℃ when the VID inputs are 11110. As the supply voltage varies from 2.7 to 5V, the voltage reference varies by about 5mV. The maximum glitch of the transient response is about 20mV at 125kHz. Depending on the state of the five VID inputs, an output voltage between 1.1 and 1.85V can be programmed in 25mV increments.

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一种可编程电压基准源设计与实现*

张　科　郭健民　孔　明　李文宏†

（复旦大学专用集成电路与系统国家重点实验室，上海　201203）

摘要：提出了一种新的基于改进的电流模式带隙基准源的可编程基准源的设计与实现方法.电路采用 Chartered 0.35μm 工艺仿真并流片.测试结果表明,温度变化范围为 0～100℃,温度系数为 ±36.3ppm/℃(VID=11110).电源电压变化范围为 2.7～5V,其相对变化值为 5mV.当 VID0 频率为 125kHz 时,瞬态响应最大毛刺幅度约为 20mV.5 位 VID 码不同的输入状态,输出基准电压从 1.1 变到 1.85V,变化步长为 25mV.

关键词：电压调整器；电流模式的带隙基准源；温度系数；电源抑制比；可编程电压基准源
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† 通信作者.Email:wenhongli@fudan.edu.cn
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