A Super-Low-Noise, High-Gain MMIC LNA*

Huang Hua†, Zhang Haiying, Yang Hao, Yin Junjian, Zhu Min, and Ye Tianchun

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: A two-stage monolithic low noise amplifier is developed for satellite communication applications, using a 0.5μm enhancement PHEMT technology. The on-chip matched amplifier employs lumped elements to reduce the circuit size, and shows a 50Ω noise figure less than 0.9dB, gain greater than 26dB, and return loss less than −10dB in the S-C band range of 3.5 to 4.3GHz. The noise figure obtained here is the best result ever reported to date of an MMIC LNA with a gain of more than 20dB for the S-C band frequency range. It is attributed to the low noise performance of the enhancement PHEMT transistor and minimized parasitic resistance of the input match network by a common series source inductor and a unique divided resistance at the drain.

Key words: low noise amplifier; enhancement PHEMT; MMIC
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1 Introduction

Nowadays, the higher data rate requirement of the wireless communication systems, such as satellite communication systems, wireless LANs, and smart antennas, is pushing communication carrier frequencies from L to C band. These systems require low noise performance to deliver high speed data between RF ends and base band computing systems. The bit error rate is mainly limited by the noise performance of the RF receiver. At the same time, because the received carrier is very weak for a satellite communication system, the signal must be magnified enough to decrease the following IF amplifier's pressure. Therefore, an extremely low noise figure less than 1.0dB and a high gain of more than 25dB are required for an outstanding satellite receiver system. The first stage of a receiver is a low noise amplifier, whose main function is to provide enough gain to overcome the noise of subsequent stages while adding as little noise as possible to the received signals.

Several monolithic low noise amplifiers have been reported for S to C band applications using GaAs PHEMT, MESFET, and HBT technologies[1~4]. The noise figure of an LNA is determined by the input matching network's parasitic resistance, the noise characteristics of the transistor, and the first stage's gain. For its excellent noise and gain properties, a PHEMT is the ideal candidate for fabricating a low noise amplifier. Enhancement PHEMTs have been greatly researched in wireless communication system applications because they have the trait of single power supply operation while keeping the features of the low noise performance and high power gain[5]. The LNA reported in this paper was designed for the application of an S-C band high speed satellite communication system. The principal design objective was a gain of over 25dB, a noise figure less than 1.0dB, and an input/output return loss less than −10dB at 3.5～4.3GHz. The power supply was 3V, and DC power dissipation was limited to 150mW. The fully monolithic LNA presented in this paper achieved a noise figure below 0.9dB between 3.5 and 4.3GHz with a high associated gain of more than 26dB using enhancement PHEMT technology with a gate-length of 0.5μm. We believed that our noise figure is the best result ever reported of an MMIC LNA with a gain of more than 20dB for the S-C band frequency range. The circuit used a two-stage common source topology. A single spiral inductor as small as 1.55nH in the in-

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† Corresponding author. Email: hua0021@sina.com
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put matching element contributed the main parasitic resistance to keep the noise down.

2 Device selection

In order to achieve a super-low noise figure, the amplifier used an enhancement PHEMT as the active element, which employed the divided voltage scheme for single supply operation.

To determine the width of the transistor, several transistors with different gate widths were chosen. Figure 1 shows the relationship between minimum noise and frequency for different gate widths (The 0425 means that the gate width is $4 \times 25\mu$m). Each transistor was biased at $V_{GS} = 0.45$V and $V_{DS} = 2.0$V. From the figure, 0225, 0250, and 0425 have lower minimum noise figures than 0825 and 0450. But the gain of 0225, 0250, and 0425 is less than 8dB at 4GHz, while the 0825 and 0450 transistors have a maximum gain of more than 13dB at 4GHz. To achieve high gain while maintaining low noise, transistor 0825(200μm gate width) was chosen for the active element in the circuit.

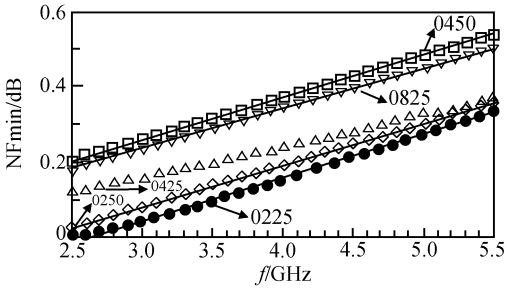

Fig. 1　Relationship of NFmin and frequency

3 Circuit design

The two-stage common source amplifier's operation with a 3V power supply was designed with on-chip input and output matching networks. One of the most important amplifier design criteria is unconditional stability at any frequency and at any source and load conditions. Because the scattering parameters of the selected enhancement PHEMT transistor revealed instability below 10GHz, a series feedback inductor at the source lead was introduced to improve the amplifier's stability. The feedback inductor provides several advantages for the low noise amplifier design. Inductive reactance at the source lead increases the real part of the transistor's gate input impedance. Thus a source inductor with a larger value can improve the circuit stability quickly. At the same time, the inductor affects the input impedance, optimum noise match impedance, and gain greatly. Lehmann has reported that S_{11}^* is altered by both the source feedback inductor and the output load impedance, whereas S_{opt} is unaffected by the output load impedance and only varies with the feedback inductor[6]. Because the noise figure of the amplifier is mainly determined by the input matching network's parasitic resistance, the noise characteristics of the transistor, and the first stage's gain, the input matching network, which contains only one small series inductor to minimize the parasitic resistance, is severely needed. Regulating the values of the series feedback inductor and load impedance, the input impedance and the optimum noise match impedance can be situated on a 50Ω resistance circle on a Smith Chart. But the result is depressed because a large series source inductor is needed to stabilize the circuit. This larger inductor reduces the first stage gain under 7dB, which will affect the whole gain and noise performance badly. Choi reported a gate width optimization technology, using a wider gate to reduce the input impedance[7]. But the DC power consumption would be unacceptable with this approach. To overcome this inconsistency, a small divided resistance at the drain lead after a medium inductance was introduced to increase the stability of the circuit while maintaining the low noise performance. After carefully regulating the series inductor and load impedance, both the input impedance and the optimum noise match impedance were situated on a 50Ω resistance circle in the Smith Chart. Figure 2 shows that S_{opt} and S_{11} lie on a 50Ω resistance circle in Smith Chart at 4GHz when the source inductor is 0.35nH and the load impedance has suitable values. It also shows that S_{opt} and S_{11} are symmetrical about the pure resistance line of the Smith Chart. From this analysis, we find that a single 1.55nH series inductor at the gate lead can make the optimum noise and conjugated input impedance match.

The second stage also uses an $8 \times 25\mu$m PHEMT with the same bias conditions as the first stage for minimizing DC power dissipation. A short microstrip was used to replace the 0.35nH

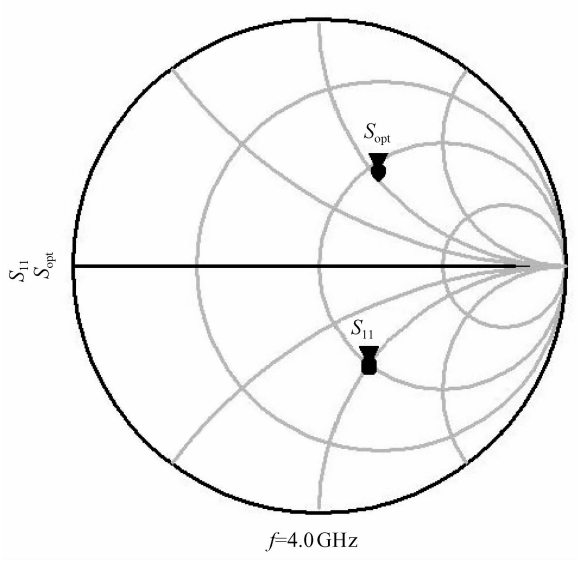

Fig. 2 S_{opt} and S_{11} values at 4GHz with 0.35nH source inductor

source inductor. A schematic diagram of the two-stage monolithic amplifier is shown in Fig. 3.

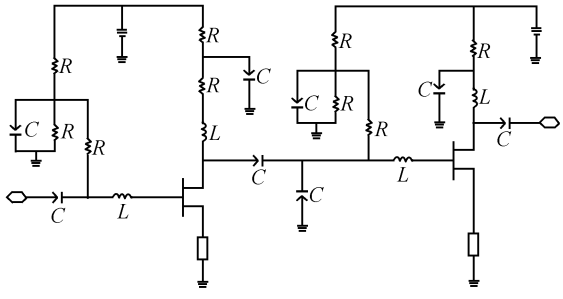

Fig. 3 Schematic circuit of the LNA

The circuit was fabricated using a 0.5μm gate length low noise enhancement PHEMT, as shown in Fig. 4. To achieve high quality factors, an inductor was implemented using two metal layers. All of the circuit elements were formed on 100μm GaAs substrate. The wafer was processed with passivation and thinned to 100μm. Then the back was etched via holes to provide low ground parasitic inductance. The chip size is 2.2mm × 1.2mm × 0.1mm.

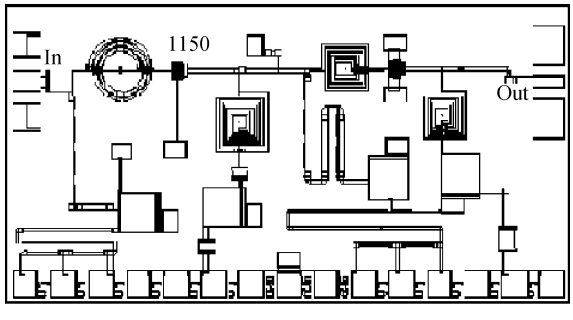

Fig. 4 Photograph of the two-stage MMIC LNA

4 Testing result

On-wafer measurements were performed using microwave and DC bias probes. A 50Ω test device for small signal parameters(HP 8510C)and noise figure(Agilent N8975A)was used. When the DC power was 3V, the total DC current of the circuit was 32mA. The amplifier had a small signal gain over 26dB, gain flatness below 0.5dB, and reverse isolation less than −40dB from 3.5 to 4.3GHz, as shown in Fig. 5. The simulated gain was plotted with the measured gain to verify the difference between design and final measurement. As expected, the gain curve shapes are similar, but the measured gain is slightly reduced, by about 2dB. It may be that the influence of passive elements on each other is not fully considered when a schematic simulation is used. The measured and simulated noise figures from 2.5 to 5.5GHz are shown in Fig. 6. It reveals a noise fig-

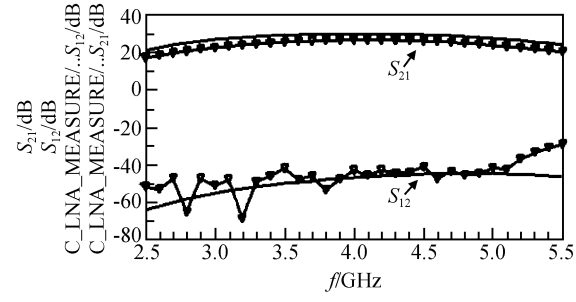

Fig. 5 Simulated and measured gain and reverse isolation versus frequency (measured data plotted with triangles)

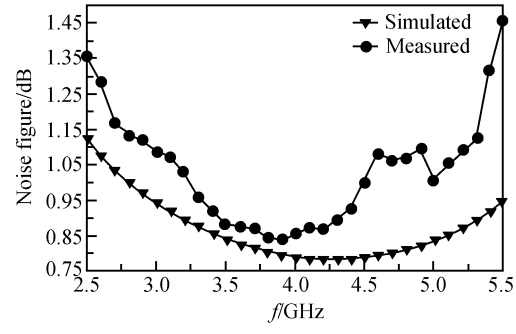

Fig. 6 Simulated and measured 50Ω noise figure versus frequency

ure less than 0.9dB between 3.5 and 4.3GHz. Choi reported a two-stage low noise amplifier with a lowest noise figure of 0.76dB at 5GHz, but the associated gain was only 16dB. We believe our noise figure is the best result ever reported of an MMIC LNA with a gain more than 20dB for the S-C band. Figures 7 and 8 show the input and output return loss versus frequency. Both input and output return losses were less than −10dB from 3.5 to 4.3GHz. The output power at 1dB gain compression was also measured at ambient temperature. The worst result was 5dBm at 3.5GHz.

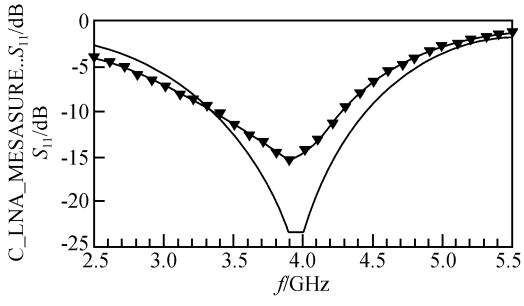

Fig. 7　Input return loss versus frequency of the LNA (measured data plotted with triangles)

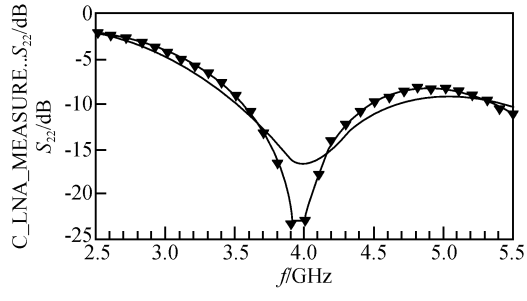

Fig. 8　Output return loss versus frequency of the LNA (measured data plotted with triangles)

5　Conclusion

A two-stage low noise amplifier using series source inductor and drain divided resistance has been fabricated. The amplifier demonstrated excellent gain, noise figure, input and output return loss performance, which have a noise figure as low as 0.9dB and gain more than 26dB from 3.5 to 4.3GHz. The amplifier can be used in high speed satellite communication directly.

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一种极低噪声高增益微波单片低噪声放大器*

黄 华† 张海英 杨 浩 尹军舰 朱 旻 叶甜春

(中国科学院微电子研究所，北京 100029)

摘要：报道了一种用于卫星通讯系统，基于 0.5μm 栅长增强型赝配高电子迁移率晶体管的两级级联微波单片低噪声放大器.采用集总参数元件来缩小电路面积进而在整个芯片内完成阻抗匹配.在 50Ω 端口测试条件下，该低噪声放大器在 3.5～4.3GHz 频率范围内，噪声系数小于 0.9dB，增益大于 26dB，回波损耗小于－10dB.这是至今为止报道的增益高于 20dB 的低噪声放大器中具有最小噪声系数的微波单片低噪声放大器，它主要归因于采用具有优异噪声性能的增强型赝配高电子迁移率晶体管以及本文提出的源极串联电感结合漏极应用一个小的稳定电阻来减小输入匹配网络寄生电阻的电路结构.

关键词：低噪声放大器；增强型赝配高电子迁移率晶体管；微波单片集成电路

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† 通信作者.Email：hua0021@sina.com

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