Low-Power CMOS IC for Function Electrical Stimulation of Nerves*

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Abstract: A low-power IC for function electrical stimulation (FES) of nerves is designed for an implantable system and fabricated in CSMC's 0.6μm CMOS technology. The IC can be used for stimulating animals' spinal nerve bundles and other nerves connected with a cuff type electrode. It consists of a pre-amplifier, a main amplifier, and an output stage. According to the neural signal spectrum, the bandwidth of the FES signal generator circuit is defined from 1Hz to 400kHz. The gain of the circuit is about 66dB with an output impedance of 90Ω. The IC can function under a single supply voltage of 3～5V. A rail-to-rail output stage helps to use the coupled power efficiently. The measured time domain performance shows that the bandwidth and the gain of the IC agree with the design. The power consumption is lower than 6mW.

Key words: neural signal; CMOS; function electrical stimulation; low power; nerve
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1 Introduction

Generally, the injury of a central neural system will result in critical effects. In the last few decades, scientists and neurologists have engaged themselves in recovering the function of injured central neural systems. Two biological methods are utilized for repairing the injury of spinal cords. One is to replant cells and organs, and the other is to lead the growth orientation of nerves by nutrition, which is essential to the growth of neurites, through the neurotrophic gene. But biological methods have been proved helpless to most central neural system injuries. Our research team has proposed an idea to recover the function of an injured central neural system, using microelectronic techniques to create an in-body embedded module that bridges the interrupted signal channels of a nerve[1～3].

The neural signal regeneration system, which can be used to recover the function of a central neural system as well as other nerves such as the sciatic nerves, includes a neural signal detecting microelectrode, a neural signal detecting amplifier, a neural signal processor, a function electrical stimulation (FES) signal generator circuit, and a stimulating microelectrode.

In the system, a microelectrode is contacted onto the upper neuron or upper neural stump near the damage point of the injured nerve to detect the bioelectrical signal on the neural stump. Because the bioelectrical signal detected by the microelectrode is weak, it is sent to the neural signal detection amplifier. There the neural signal will be amplified to suitable amplitude, for example, one hundred millivolts[1]. Then, the neural signal is further amplified and filtered by the signal processor. Then, the neural signal is sent to the FES signal generator circuit, and the desired signal is generated. Finally, the FES signal is sent to the stimulating microelectrode that is in contact with the lower neuron or lower neural stump near the damage point of the injured nerve, so that a bioelectrical signal is regenerated therein, which is similar to that from a normal neural channel[4,5].

2 Integrated circuit for function electrical stimulation of nerves

In our design, the FES signal generator circuit consists of a preamplifier, a main amplifier, and an output stage. The load of the circuit is the cuff microelectrode contacted with nerves; its imped-

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ance is about several kilo-ohms. The preamplifier is an amplifier with a constant gain, and it functions to amplify the input signal so that the neural signal can be processed more efficiently with the following stages. The main amplifier is an amplifier whose function is to provide great gain, and the output stage is a buffer between the circuit for FES of nerves and the load.

The circuit diagram of the preamplifier and the main amplifier designed in CMOS is shown in Fig. 1. The preamplifier circuit consists of a pMOS input circuit and an nMOS input circuit, which can run in a rail-to-rail input voltage, because the input signal is from the neural signal processor and thus its amplitude may be strong enough. The nMOS input circuit consists of M_{A11}, M_{A12}, M_{AB}, M_{A13}, and M_{A14}. M_{A11} and M_{A12} are input differential pair with M_{AB} as its current source. M_{A13} and M_{A14} function as the active loads of the amplifying stage. The gain of the preamplifier is determined by W/L of M_{A11} (M_{A12}) and M_{A13} (M_{A14}). The pMOS input circuit, which is similar to the nMOS input circuit, consists of M_{B11}, M_{B12}, M_{BB}, M_{B13}, and M_{B14}.

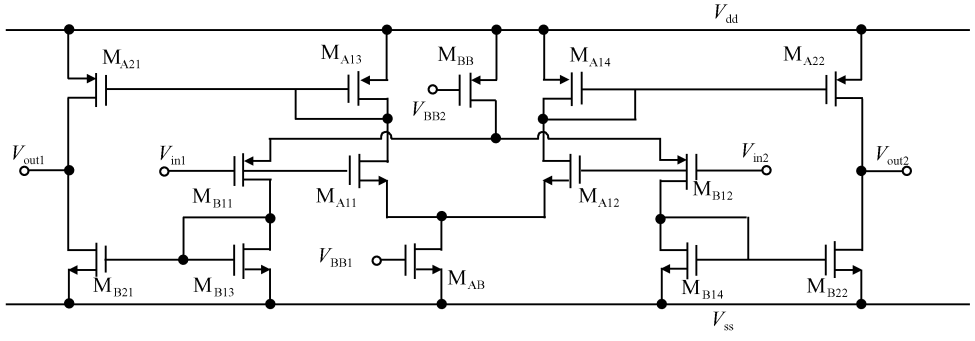

Fig. 1 Preamplifier and main amplifier of the FES signal generator circuit

For the nMOS input circuit, because the circuit is symmetric, the half-circuit method can be used to analyze the performance. Supposing the DC current of M_{AB} is I_{DD1}, according to the transconductance formula:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2K(V_{GS} - V_{TH}) = 2\sqrt{KI_D} = \frac{2I_D}{V_{GS} - V_{TH}} \quad (1)$$

the transconductance of transistors M_{A11} and M_{A13} are

$$g_{m,A11} = 2\sqrt{K_{A11} \times \frac{1}{2} \times I_{DD1}} = \sqrt{\mu_n C_{OX} \left(\frac{W}{L}\right)_{A11} I_{DD1}} \quad (2)$$

$$g_{m,A13} = 2\sqrt{K_{A13} \times \frac{1}{2} \times I_{DD1}} = \sqrt{\mu_p C_{OX} \left(\frac{W}{L}\right)_{A13} I_{DD1}} \quad (3)$$

The gain of the nMOS input circuit is

$$A_{V,NMOS-INPUT} = -\frac{g_{m,A11}}{g_{m,A13} + \dfrac{1}{r_{O,A11} \,//\, r_{O,A13}}} \quad (4)$$

This does not account for the effect of channel-length modulation, which is the effect of $r_{O,A11}$ and $r_{O,A13}$:

$$A_{V,NMOS-INPUT} = -\frac{g_{m,A11}}{g_{m,A13}} = -\sqrt{\frac{\mu_n (W/L)_{A11}}{\mu_p (W/L)_{A13}}} \quad (5)$$

According to the above discussion, the gain of the input stage is determined by the value of W/L of M_{A11} (M_{A12}) and M_{A13} (M_{A14}).

Similar to the nMOS input circuit, the gain of the pMOS input circuit is given by

$$A_{V,PMOS-INPUT} = -\frac{g_{m,B11}}{g_{m,B13}} = -\sqrt{\frac{\mu_p (W/L)_{B11}}{\mu_n (W/L)_{B13}}} \quad (6)$$

The main amplifier consists of M_{A21} (M_{B21}) and M_{A22} (M_{B22}). This is a common-source amplifier. M_{A21} and M_{B21} are the loads for each other.

Assuming the DC current of M_{A21} and M_{B21} is I_2, the values of transconductance of transistors M_{A21} and M_{B21} are:

$$g_{m,A21} = 2\sqrt{K_{A21} I_2} = \sqrt{2\mu_p C_{OX} (W/L)_{A21} I_2} \quad (7)$$

$$g_{m,B21} = 2\sqrt{K_{B21} I_2} = \sqrt{2\mu_n C_{OX} (W/L)_{B21} I_2} \quad (8)$$

When the input is from the nMOS input, M_{A21} is the amplifier transistor and M_{B21} is the load transistor, and the gain is defined by

$$A_{V,NMOS-INTER} = -g_{m,A21}(r_{O,A21} \,//\, r_{O,B21} \,//\, R_{OUTPUT}) \quad (9)$$

When the input consists of the pMOS input, M_{B21} is the amplifier transistor, M_{A21} is the load transistor, and the gain is:

$$A_{V,PMOS-INTER} = -g_{m,B21}(r_{O,A21} \,//\, r_{O,B21} \,//\, R_{OUTPUT}) \quad (10)$$

Thus the gain of the main amplifier is mainly determined by W/L of M_{A21} (M_{B21}).

According to the amplifier circuit shown in Fig. 1, the neural signals pass through the preamplifier, which includes an nMOS input circuit and a pMOS input circuit, and the main amplifier. The gains of A_N and A_P are given by

$$A_N = A_{V,NMOS-INPUT} A_{V,NMOS-INTER} = \sqrt{2\mu_n C_{OX} \frac{(W/L)_{A11}}{(W/L)_{A13}} (W/L)_{A21} I_2} \times (r_{O,A21} \,//\, r_{O,B21} \,//\, R_{OUTPUT}) \tag{11}$$

$$A_P = \sqrt{2\mu_p C_{OX} \frac{(W/L)_{B11}}{(W/L)_{B13}} (W/L)_{B21} I_2} \times (r_{O,A21} \,//\, r_{O,B21} \,//\, R_{OUTPUT}) \tag{12}$$

The total gain is:

$$A = A_N + A_P \tag{13}$$

Since the circuit is symmetric, we have:

$$A_N = A_P \tag{14}$$

This results in:

$$\sqrt{\mu_n \frac{(W/L)_{A11}}{(W/L)_{A13}} (W/L)_{A21}} = \sqrt{\mu_p \frac{(W/L)_{B11}}{(W/L)_{B13}} (W/L)_{B21}} \tag{15}$$

We assume:

$$\frac{(W/L)_{A11}}{(W/L)_{A13}} = \frac{(W/L)_{B11}}{(W/L)_{B13}} \tag{16}$$

and therefore,

$$\mu_n (W/L)_{A21} = \mu_p (W/L)_{B21} \tag{17}$$

and

$$\frac{(W/L)_{A21}}{(W/L)_{B21}} = \frac{\mu_p}{\mu_n} \tag{18}$$

The total gain of the preamplifier and the main amplifier can be expressed as

$$A = 2\sqrt{2\mu_n C_{OX} I_2} (r_{O,A21} \,//\, r_{O,B21} \,//\, R_{OUTPUT}) \times \sqrt{\frac{(W/L)_{A11}}{(W/L)_{A13}} (W/L)_{A21}} \tag{19}$$

The output stage consists of transistors M_{31}, M_{32}, and amplifiers A1 and A2. M_{31} and M_{32} with high W/L are designed to enhance the transistors' drive ability; M_{31} and M_{32} function as a common-source amplifier for a rail-to-rail output voltage, avoiding voltage loss as a source-follower. Furthermore, the circuit is in feedback through amplifiers A1 and A2 for lower output impedance.

The output stage of the FES signal generator circuit is shown in Fig. 2. Supposing transistors M_{31} and M_{32} work in the saturation region, the output voltage can be expressed as

$$V_{out} = -(g_{m,M31} V_{gs,M31} + g_{m,M32} V_{gs,M32})(r_{O,M31} /\!/ r_{O,M31}) \tag{20}$$

where

$$V_{gs,M31} = A_1 (V_{out} - V_{in})$$
$$V_{gs,M32} = A_2 (V_{out} - V_{in})$$

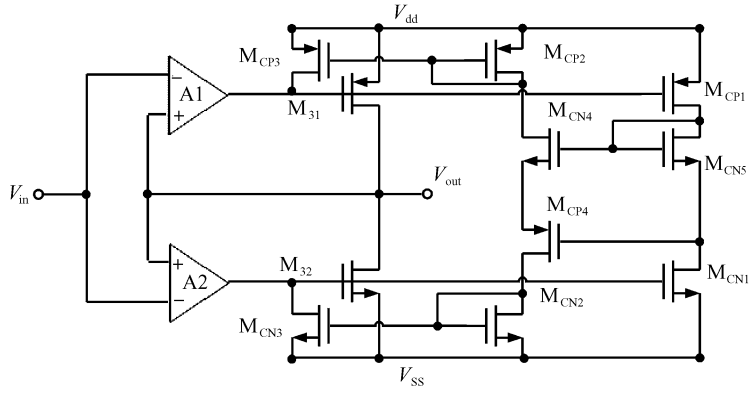

Fig. 2　Output stage of the FES signals generator circuit

By setting

$$A_1 = A_2 = A$$

we obtain

$$A_V = \frac{V_{out}}{V_{in}} = \frac{2g_{m3} A (r_{O,M31} \,//\, r_{O,M31})}{1 + 2g_{m3} A (r_{O,M31} \,//\, r_{O,M31})} \approx 1 \tag{21}$$

The structures of amplifiers A1, A2 are shown in Fig. 3.

Because the output of the FES signal generator circuit is in a rail-to-rail state, a protection circuit must be included. The protection circuit consists of M_{CP1} (M_{CN1}), M_{CP2} (M_{CN2}), M_{CP3} (M_{CN3}), M_{CP4} (M_{CN4}) and M_{CN5}, of which the W/L of transistor M_{CN5} is small. When the current of the circuit is normal, the current of M_{CN5} is weak, and thus V_{DS} of M_{CN5} is not great enough to turn the transistor M_{CP4} (M_{CN4}) "on"; otherwise, when the output current becomes too large, the current through M_{CN5}

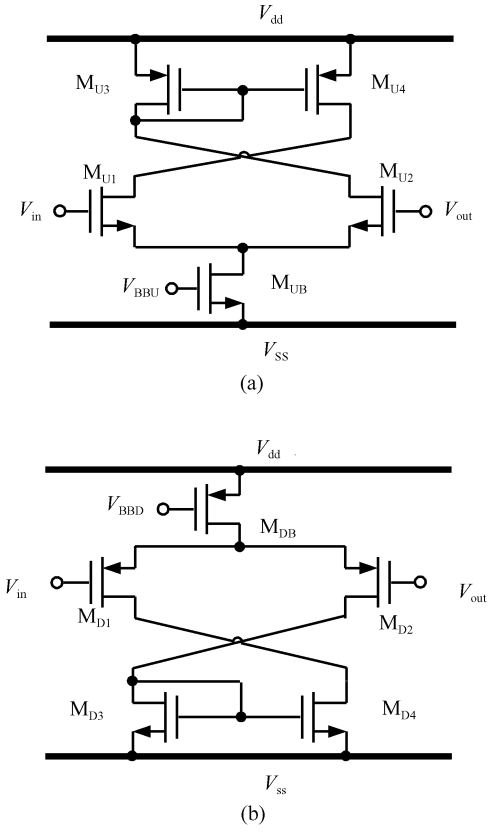

Fig. 3 Structures of amplifiers A1 (a) and A2 (b)

increases, V_{DS} of M_{CN5} becomes strong enough to open M_{CP4} and M_{CN4}, and then a feedback circuit flows to M_{31}, M_{32} though M_{CP2} (M_{CN2}), M_{CP3} (M_{CN3}) to protect the circuit.

The FES signal generator circuit was fabricated in CSMC 0.6μm CMOS technology. Its photomicrograph is shown in Fig. 4.

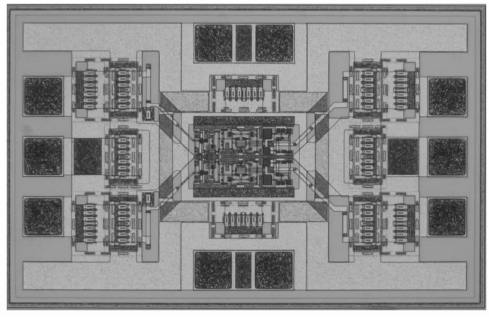

Fig. 4 Photomicrograph of the FES signal generator circuit

3 Measurement results

The chips were measured on-wafer using 50Ω coplanar test probes. The differential input signals were generated from the pulse pattern generator, an Agilent 33220. The oscilloscope was an Agilent 54624.

The DC current of the FES signal generator circuit is lower than 2mA with the power supply voltage change from 3 to 5V. Thus, the power consumption of the circuit is less than 6mW. The output impedance is about 90Ω. With a 3.3V power supply, the maximum output voltage is 3V, and with a 5V power supply, it is about 4.7V.

For the input signal amplitude of 20mV and the frequencies of 1Hz, 100kHz, and 400kHz, the waveforms of the output signal are shown in Fig. 5. For the input signal frequency of 10kHz and the amplitudes of 80, 50, and 20mV, the waveforms of the output signal are shown in Fig. 6.

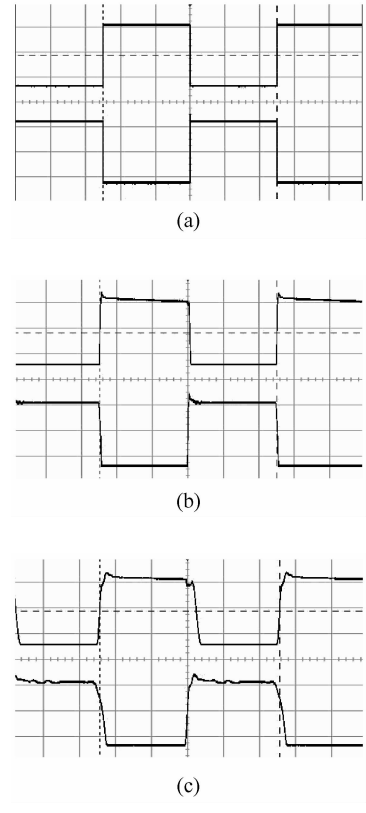

Fig. 5 Waveforms of the output signal at different frequencies of the input signal (a) f = 1Hz; (b) f = 100kHz; (c) f = 400kHz

4 Conclusions

An FES signal generator circuit has been realized in 0.6μm CMOS technology. It has a gain of about 66dB, a bandwidth of more than 400kHz, and an output impedance of 90Ω. It can

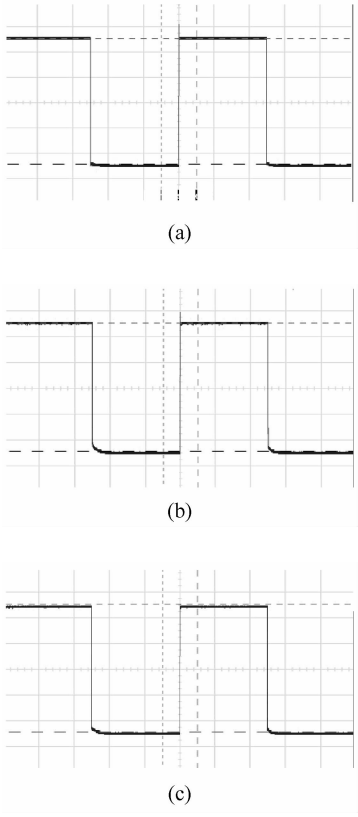

Fig. 6　Waveforms of the output signal at different amplitudes of the input signal　(a) Input $V_{p\text{-}p}$ = 80mV; (b) Input $V_{p\text{-}p}$ = 50mV; (c) Input $V_{p\text{-}p}$ = 20mV

work under a supply voltage from 3 to 5V. The power consumption is lower than 6mW. The circuit can be used in an implanted system for neural signal recovery.

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低功耗 CMOS 神经束功能电激励信号产生电路*

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摘要： 采用华润上华微电子公司 0.6μm CMOS 工艺设计了低功耗神经功能电激励集成电路. 该电路适用于以卡肤电极作为激励电极的可植入式神经信号桥接系统，可以用来激励脊椎动物的脊髓神经或其他神经束. 电路包括输入级差分预放大电路、增益级放大电路和输出电路. 为满足体内植入式神经功能电激励的要求，该集成电路避免使用任何片外元件，实现了单片集成. 根据神经信号的特点，神经功能激励电路的频率响应带宽设计为 1Hz～400kHz，输出电阻为 90Ω 时的增益为 66dB，可以在 3～5V 的工作电压下正常工作. 采用满摆幅输出级提高了有效的激励电压输出. 测试结果表明，电路的带宽和增益符合设计要求，直流功耗低于 6mW，达到了设计目标.

关键词： 神经信号；CMOS；功能激励；低功耗；神经

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