Fabrication of SiC MESFETs for Microwave Power Applications

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Abstract: 4H-SiC MESFETs are fabricated on semi-insulating SiC substrates. Key processes are optimized to obtain better device performance. A microwave power amplifier is demonstrated from a 1mm SiC MESFET for S band operation. When operated at a drain voltage of 64V, the amplifier shows an output power of 4.09W, a gain of 9.3dB, and a power added efficiency of 31.3%.

Key words: 4H-SiC; MESFET; microwave; power amplifier
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1 Introduction

SiC MESFETs are very promising for high power microwave applications due to their high operating voltage and high power density. Production-level devices with an output power of 60W and higher power MMICs are available through Cree foundry service. The operational reliability and wear-out reliability have been shown to exceed the requirements for commercial and military microwave power amplifiers[1]. In China, research on SiC MESFETs has also worked out some encouraging results[2,3]. In this paper, we report our work on SiC MESFETs and present results of a SiC power amplifier with an output power of over 4W at 2GHz.

2 Device process

A cross-section of the device design is shown in Fig.1. The MESFET structures were fabricated on high purity semi-insulating (HPSI) 4H-SiC substrates produced by Cree. A low-doped p-type buffer layer was deposited to minimize the effects of deep levels or extended defects due to the substrate. The buffer layer was 0.5μm in thickness and doped to a concentration of about 2×10^{15} cm^{-3}. Then a 0.4μm n-type channel layer was grown with a doping of $2\times10^{17}cm^{-3}$. Finally, a 0.2μm n^+ contact layer doped to a concentration of about $2\times10^{19}cm^{-3}$ was deposited.

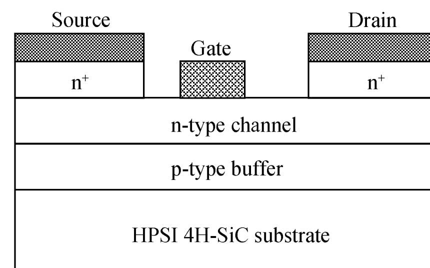

Fig. 1 Cross-sectional view of 4H-SiC MESFET

The MESFET utilized a ten-fingered design with 100μm for each finger and a total gate width of 1mm. The gate length was 0.8μm, and the gate-source and gate-drain spacings were 0.8 and 1.6μm, respectively. The fabrication process is similar to that reported previously[3]. All lithography was done using a Karl Suss MJB3 contact exposure system. The fabrication process started with the etching of mesas down to the substrate for device isolation. The contact layer etching and the channel recess were done using an inductive coupled plasma (ICP) system. The source and drain ohmic contacts were annealed, and a Ti/Pt/Au multilayer metal system was used as the gate. All deposited metal patterns were defined by the lift-off technique. The MESFET was passivated with Si_3N_4 film deposited by plasma enhanced

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chemical vapor deposition (PECVD). A 2μm-thick Au air-bridge was fabricated using the electroplating technique.

According to our previous work[3], the device performance was limited by the ohmic contact process, which produced a specific contact resistance typically in the mid range of $10^{-5}\Omega\cdot cm^2$. By optimizing the annealing time and the annealing temperature, we lowered the contact resistance by one order of magnitude. Figure 2 shows the resistance between adjacent ohmic contacts plotted as a function of contact spacing. The data exhibit an excellent linear relationship with a minimum specific contact resistance of $9\times10^{-7}\Omega\cdot cm^2$.

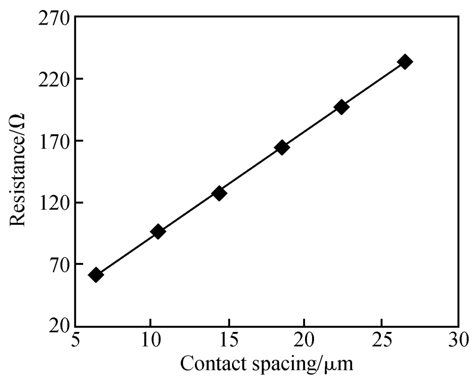

Fig. 2　Resistance between adjacent ohmic contacts as a function of contact spacing

Channel recess was another performance limiting process. For a channel recessed MESFET, the Schottky gate is formed on an etched surface. The quality of the interface is crucial to the device performance. Reactive ion etching (RIE) tends to roughen the surface and leaves a carbon-rich, contaminated surface. The surface image of the RIE etched surface, which was taken by a scanning electron microscope (SEM), is shown in Fig. 3 (a). The surface roughness is evident even after sacrificial oxidation. In this work, we have developed an ICP etching process with a NF_3 and O_2 mixture. ICP etching relies more on chemical etching, resulting in smooth surfaces with less damage. Figure 3 (b) shows a surface SEM image after ICP etching. For the same amount of channel recess, the ICP etching apparently produced a much smoother surface than RIE, leading to reduced etching damage and improved device performance.

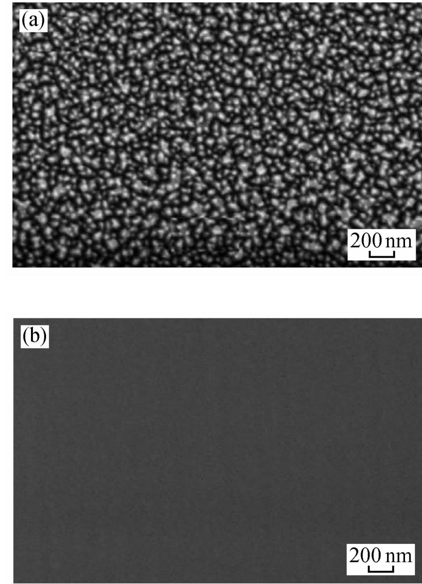

Fig. 3　SEM image of the surface after channel recess by RIE (a) and ICP (b) etching

3　DC and RF performance

The typical *I-V* and transfer characteristics of the 100mm SiC MESFET are shown in Fig. 4 and Fig. 5, respectively. When $V_{ds}=40V$, the saturation current density was about 400mA/mm and the peak transconductance was 25～30mS/mm, with a gate pinch-off voltage of −18V. The maximum output power density for a class A amplifier is given by the equation[5]

$$P_{max} = \frac{I_{dss}(V_b - V_{knee})}{8}$$

where I_{dss} is the saturation current, V_b is the breakdown voltage, and V_{knee} is the knee voltage. The gate-drain breakdown voltage and the knee voltage were about 120 and 10V, respectively. The

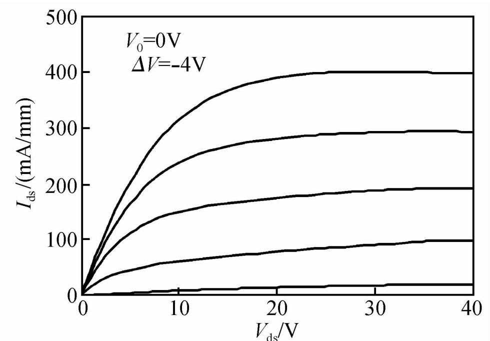

Fig. 4　*I-V* characteristics of SiC MESFET with 100mm gate width

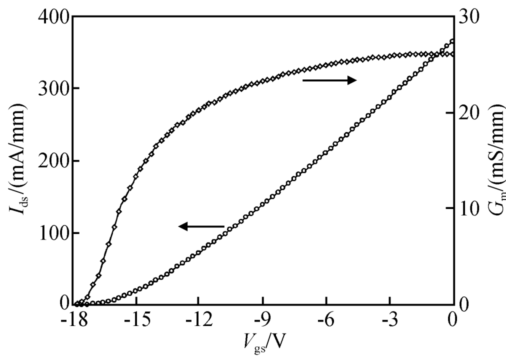

Fig. 5 Transfer characteristics of SiC MESFET with 100μm gate width

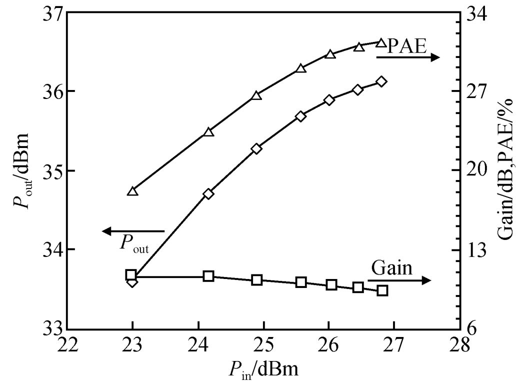

Fig. 6 RF power performances of the SiC MESFET power amplifier at 2GHz

maximum power density should be 5.5W/mm, according to the DC characteristics. The DC characteristics of the 1mm SiC MESFET were similar to that of the 100μm device when $V_{ds} < 20$V. At higher voltages, there is large power dissipation in SiC MESFETs, leading to a self-heating effect. In spite of the good thermal conductivity of the SiC material, a decrease in current is observed.

The 1mm SiC MESFETs were diced, individually packed, and mounted on hybrid amplifier circuits. Chip capacitors were used as the first matching elements at both the input and output. Mechanical slide tuners on both the input and output provided additional tuning for maximum power. When operated at 2GHz, a drain voltage of 64V, and gate bias of −10V, one power amplifier showed an output power of 4.09W with a gain of 9.30dB under continuous wave (CW) conditions. The power added efficiency (PAE) was calculated to be 31.3%. The CW power sweep for this amplifier is shown in Fig. 6. Both the output power and the power density (4.09W/mm) are the highest ever reported for a SiC MESFET in China. However, the obtained power density is much lower than the theoretical expectation of 5.5W/mm, and inferior to the best reported result[6].

The RF stability of the power amplifier was tested at room temperature with a fan cooling system. A drain bias of 56V and an input power of 0.39W were applied to reach an output power level of 3.50W, corresponding to a 3dB gain compression. The time dependence of the output power is shown in Table 1. Throughout the limited time of testing, the output power remained fairly stable. An investigation of the RF stability for a longer time period is underway.

Table 1 Time dependence of the output power

Time/min	0	5	10	15	20	25	30
Power/W	3.50	3.48	3.47	3.48	3.49	3.50	3.50

4 Conclusion

In summary, we have fabricated high performance SiC MESFETs on HPSI 4H-SiC substrates. Using a 1mm SiC MESFET, we demonstrated a power amplifier with an output power of 4.09W at 2GHz and 64V operation. Some initial results of RF power stability are also presented.

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SiC MESFET 微波功率器件的研制

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摘要： 利用本实验室生长的 4H-SiC 外延材料开展了 SiC 微波功率器件的研究.通过对欧姆接触和干法刻槽工艺的优化,研制出高性能的 SiC MESFET.利用 1mm 栅宽 SiC MESFET 制成的微波功率放大器在 2GHz 64V 工作时,连续波输出功率达 4.09W,功率增益为 9.3dB,PAE 为 31.3%.文中还给出了 SiC 功率放大器在微波大信号工作时的稳定性的初步测试结果.

关键词： 碳化硅；MESFET；微波；功率放大器

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