An Analog Equalizer and Baseline-Wander Canceller for 100/1000Base-TX Transceiver *

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Abstract: A frequency-domain equalizer with a mixed-signal adaptive control loop and a novel baseline wander (BLW) canceller are proposed. The equalizer is independent of channel-modeling accuracy, and its control loop is intrinsically stable. An AGC function is incorporated into the equalizer without an extra AGC circuit. The proposed BLW canceller uses a peak detector to monitor the BLW and full feedback method to accomplish BLW canceling. High canceling accuracy and robust performance are achieved. The circuits are tested in 0.25μm CMOS technology. Better performance and smaller silicon area are achieved compared with results in the literature.

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1 Introduction

Equalizers and baseline-wander (BLW) cancellers are two key modules of 100/1000Base-TX Ethernet transceivers. Equalizers are used to eliminate inter-symbol interference (ISI) caused by the limited bandwidth of category 5 UTP (unshielded twisted-pair) cable, and BLW cancellers are used to compensate DC component loss caused by the high pass nature of network transformers. Their performance greatly affects a chip's BER performance, and they account for most of a chip's area and power consumption[1~5]. In order to meet the demands of low cost, low power, and high performance, robust designs with tight requirements on performance, area, and power consumption are necessary.

One widely used adaptive equalization method is based on time-domain equalization, which uses an FIR filter to eliminate ISI and an LMS algorithm to update the FIR coefficients adaptively. It can be realized in either the digital or analog domain. Digital implementations usually require a low-resolution and high speed ADC to perform analog to digital conversion preceding the following DSP processing. Large silicon area and power consumption are the main shortcomings of this method[1~5]. Direct analog implementation is somewhat better in this respect, but its performance is vulnerable to technology and timing mismatch[6,7]. Frequency-domain equalization is considered to be a more efficient way to achieve small area and low power performance, which adopts a g_m-C or RC active filter to match the inverse transfer function of the channel. The key problems of such an equalizer are how to make its performance channel modeling-accuracy independent and how to construct a robust adaptive control loop. Three different kinds of adaptive control loops are presented in Refs. [7~9]. The method presented in Ref. [8] is a simple but efficient one, yet it cannot control a signal's flat loss; the other two methods presented in Refs. [7,9], respectively, incorporate the control of an AGC, a BLW canceller, and equalization together but have potential stability problems.

The implementation of a BLW canceller is dependent on the architecture of the equalizer. The same architecture as the equalizer will be adopted if a time-domain equalizer is used[1~5]; otherwise a feed-forward method, which regenerates the approximate DC value of the transmitted signal and then restores it back to the received

signal, is commonly used[10,11]. The former will consume more silicon area and power, while the canceling accuracy of the latter is highly dependent on the transformer characteristics, technology variance, signal quality, and dynamic range of the circuit.

In this paper, a compact frequency-domain adaptive equalizer that adopts a second order g_m-C filter controlled by a novel adaptive loop and a BLW canceller with a simple structure but high accuracy are proposed. The equalizer is channel-modeling accuracy independent, and the control loop is intrinsically stable. The equalizer elaborately incorporates the automatic gain control (AGC) function to compensate the flat loss without an extra AGC circuit, which helps to save chip area and power consumption further. The BLW canceller is a novel design and is very simple in structure but efficient in performance and silicon area. In addition to the advantages mentioned above, good performance, low power, and low silicon area consumption are achieved. The circuit is fabricated in 1st silicon 0.25μm CMOS technology. Measurement results and comparison to the results in the literature are also given in the following sections.

2 System architecture

A 100/1000Base-TX transceiver uses category 5 UTP cable as the signal transferring media. For this kind of cable, the maximum signal attenuation Loss (in dB) at 20℃, defined by the TIA/EIA-568-A standard[10], is

$$Loss(d,f) = \frac{d}{100}(1.967\sqrt{f} + 0.023f + 0.050/\sqrt{f}) \quad (1)$$

where d is the cable length in meters, and f is the frequency in MHz. This demonstrates nonlinear frequency dependent attenuation: small attenuation is observed at low frequencies, while large attenuation at the speed of about -20dB/dec can be observed at high frequencies. A first-order transfer function is insufficient to compensate the attenuation over the entire frequency range. Thus a 2nd-order transfer function as below is considered:

$$H_{eq}(s) = \frac{1 + \dfrac{s}{\dfrac{p_1}{1 + a_1}}}{1 + \dfrac{s}{p_1}} \times \frac{1 + \dfrac{s}{\dfrac{p_2}{1 + a_2}}}{1 + \dfrac{s}{p_2}} \quad (2)$$

Here p_1, p_2 are the poles of the transfer function, and a_1, a_2 are the coefficients to set the gain of the equalizer. For a given length channel model, a Matlab-based curve fitting routine is used to determine p_1, p_2 and a_1, a_2. The result shows that p_1, p_2 can be fixed at 2 and 50MHz, respectively, and only a_1, a_2 need to be adjusted for channel length variation. The maximum matching error between $|H_{eq}(s)|$ and the inverse response of different channel lengths in the frequency range of 0.5 to 65MHz is plotted in Fig.1. It can be seen that a good equalization result can be achieved using this transfer function as the equalizer prototype as long as proper coefficients a_1, a_2 are set.
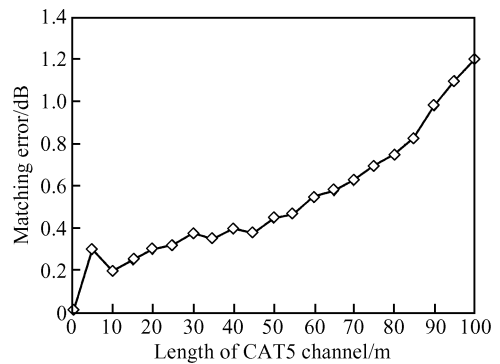

Fig. 1   Maximum matching error versus channel length

According to the curve fitting result, the peak value of the proper equalized signal passing through a band-pass filter versus channel length is plotted in Fig.2. For the purpose of comparison, the peak value of input signal without equalization is also plotted. It can be seen that when the input signal is well equalized this peak value is almost independent of the channel length and can be used as the criterion of whether proper equalization is achieved.
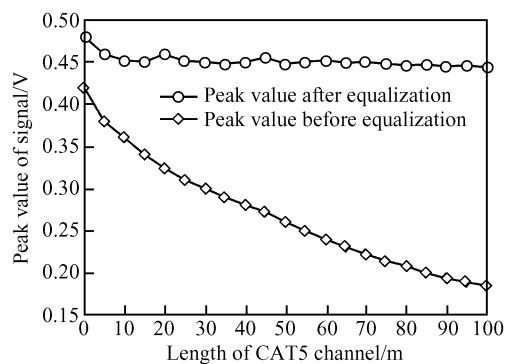

Fig. 2   Peak value of equalized signal through band-pass filter

Based on the above analysis, it is natural to get the system implementation idea that the transfer function described above can be implemented as the equalizer core. A lookup table can be constructed to store the needed coefficients, and a control loop that detects the peak value of the equalized signal passing through a band-pass filter can be used to search for the proper coefficients in the lookup table. The detailed system block diagram is shown in Fig. 3. Its operating principle can be described as follows: The received signal with ISI and BLW first arrives at the equalizer. At the reset state, the initial a_1, a_2 are given, and the equalizer works under the initial state. For every T_0 time, the peak value of the equalized signal through the band-pass filter is compared with two fixed levels, which are the expected peak value as shown in Fig. 2 plus/minus a small margin. This is for the reliable convergence of the loop. When the outputs of the comparators, D_0 and D_1, are "10", the coefficients set currently are considered to be the proper ones; otherwise the counter will increase for "00" or decrease for "11". Thus the index of the lookup table will move in the same manner and the coefficients converted by the DAC will change towards the right direction. After equalization, the signal will be sent into the BLW canceller to compensate the BLW if necessary.
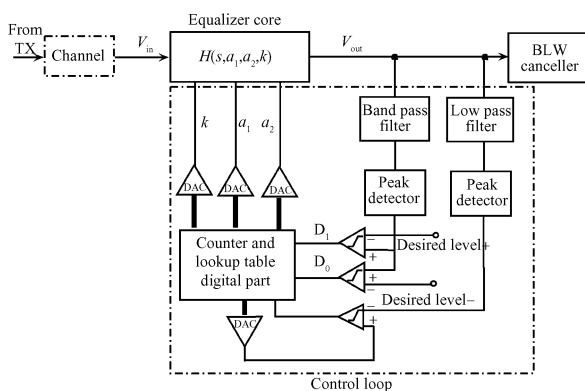
in the range of ±30% must be considered, which is commonly ignored in the literature[1～11,16,17]. Proper step size and content optimization of the table are used to diminish the inherent modeling accuracy dependence of the frequency-domain equalizer. Figure 4 shows the system level simulation result of the equalizer controlled by the proposed loop when the channel characteristics vary in the range of ±30%. The matching error is controlled within 1.3dB for all cases.
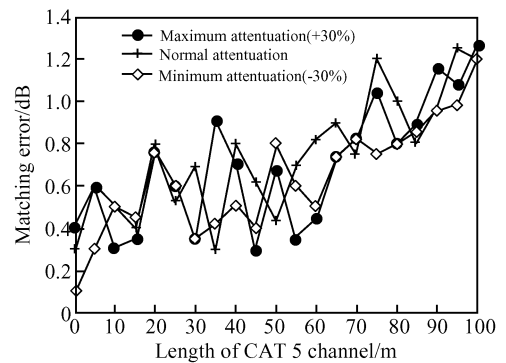

Fig. 4   Matching error for ±30% channel characteristics variation

The flat loss introduced by the network transformer and amplitude variation of transmitted signal is ignored in the above analysis. When flat loss does exist and no compensation is adopted, the signal will be over-equalized. Thus an extra flat loss compensation loop is added, the structure and the principle of which is similar with the adaptive equalization control loop, while a low-pass filter is used instead of a band-pass filter. A system level simulation result shows that this loop can compensate the flat loss in the range of 0 ～ −4.4dB with an accuracy of 50mV. The following section will show that the flat gain k as illustrated in Fig. 3 can be incorporated in the equalizer without an extra circuit.

For stability considerations, the flat loss compensation loop is active for only one time after coarse equalization is achieved. When it finishes, the flat loss is compensated and the adaptive equalization control loop is enabled again to perform fine equalization. Figure 5 shows the eye-diagram of the equalized signal at system level simulation with a 100m worst-case channel model and −3dB flat loss.
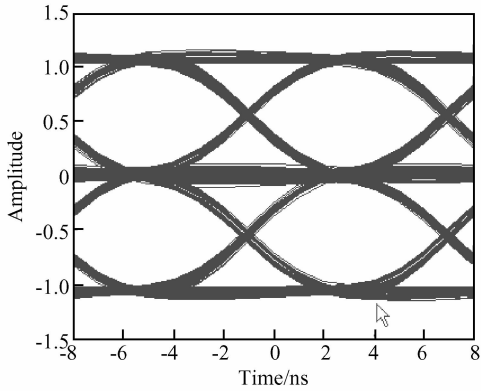
When BLW occurs, it is manifested on the

Fig. 3   System block diagram

The lookup table is constructed according to the system level simulation. Actual cable has a 0.3% temperature coefficient[12], and its performance also has some relation with different manufacturing technology. To achieve robust performance, channel model characteristics varying

Fig.5 Eye diagram of 100m channel with −3dB flat loss

peak values of the differential input signal: one peak value will increase while the other decreases. If the peak values can be forced to be equal while the useful signal remains unaffected, the BLW can be successfully compensated. The block diagram based on the above idea can be used to fulfill this task, which is illustrated in Fig. 6. The BLW is detected by the dual peak detectors and inversely amplified by the following high gain operational amplifier. The output signal of the amplifier is then added to the input signal.
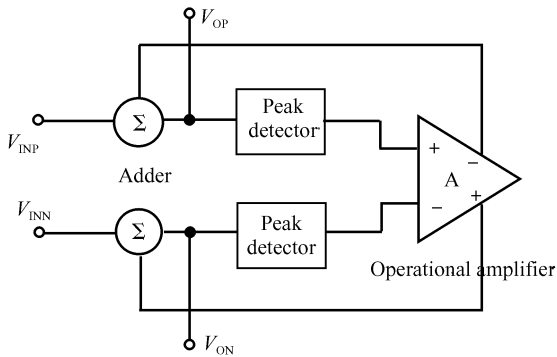

Fig.6 Block diagram of BLW canceller

When the feedback loop is settled, the BLW of the input signal is well compensated. Assuming all the modules are ideal, the remaining BLW can be described as

$$V_o = \frac{1}{1 + A}V_{in} \tag{3}$$

where V_o means the remaining BLW after compensation, V_{in} means the input BLW, and A means the DC gain of the operational amplifier. It can be seen that as long as A is high enough, BLW can be totally compensated independent of transformer characteristics, technology variance, and environment change. Circuit level implementation and non-ideal factors will be discussed in Section 3.

3 Circuit implementation

3.1 Adaptive equalizer

The equalizer core is illustrated in Fig. 7[13].

p_1, p_2 in Eq. (2) are determined by g_{m1}/C_1 and g_{m2}/C_2, respectively. The control voltage of g_m-cells, g_{m1}, g_{m2}, is provided through a switched-capacitor tuning circuit[14] so that the poles are fixed and won't change with technology variance. The schematic of g_m-cells used in the equalizer is depicted in Fig. 8. A proper control voltage V_c is chosen and an operational amplifier is used to force the input transistor operating in the triode region. Thus the transconductance of the g_m-cell is as follows:

$$g_m = k' \frac{W}{L}V_c \tag{4}$$

where k' is the transconductance parameter, W, L are the width and length of the transistor, respectively, and V_c is the control voltage. If the
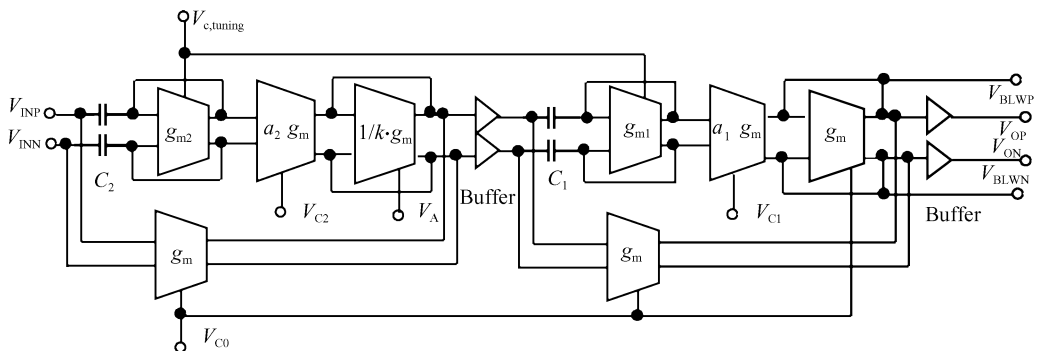

Fig.7 Schematic of the equalizer core

same W to L ratio is used for all the g_m-cells except g_{m1} and g_{m2}, then the coefficients a_1, a_2, and flat gain k are only determined by the control voltage ratio V_{c1}/V_{c0}, V_{c2}/V_{c0} and V_{c0}/V_A. Since the same reference voltage and resistor-divided DAC are used, high accuracy for these coefficients can be achieved. The effect of finite DC gain and bandwidth of the g_m-cell on the equalizer core can be compensated by the adaptive control loop.

The band-pass filter and low-pass filter in the control loop are simple g_m-C filters tuned by the same switched-capacitor circuit mentioned above. The peak-detector is an operational amplifier based structure as used in the BLW canceller illustrated below.

3.2　BLW canceller

The detailed circuit of the BLW canceller is shown in Fig. 9. It is directly connected to the equalizer through the pins named V_{BLWP} and V_{BLWN} in Figs. 8 and 9. Considering the structure of the preceding equalizer, a current mode adder is used here. The V-I converter for the input signal and I-V converter needed is already incorporated in the equalizer as demonstrated in the dotted frame. Only an extra g_m-cell is needed to convert the BLW voltage into current. The quantitative analysis of the canceling result, considering the mismatch of the transistors, is given by

$$V_{BLWO} = \frac{V_{inBLW}}{1+A_2} + \frac{V_{osin}}{1+A_2} + \frac{A_2}{1+A_2}V_{os1} + \frac{V_{os2}}{1+A_2} \approx V_{os1} \quad (5)$$

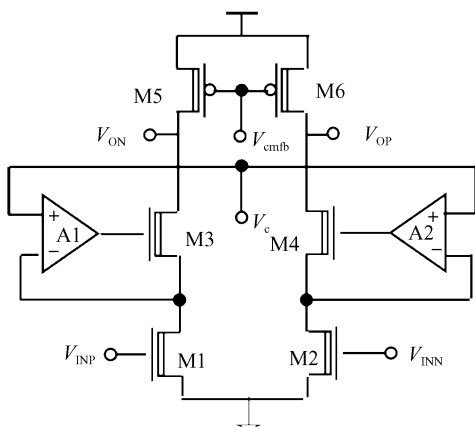Fig. 8　Schematic of g_m-cell

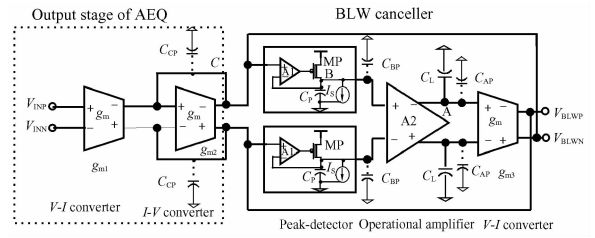Fig. 9　Schematic of BLW canceller

where V_{inBLW}, V_{osin}, V_{os1}, and V_{os2} are the input wandering value, the offset voltage of the input signal, the mismatch of the two peak detectors plus the input offset voltage of the operational amplifier A2, and the offset voltage of the g_{m3} transconductance, respectively. It can be seen that almost only V_{os1} will impact the accuracy of the BLW canceller when the DC gain of the operational amplifier is high enough. It can also be seen that this circuit can correct the offset voltage of the equalized signal at the same time.

Since negative feedback is used to achieve robust performance, stability should be considered carefully. Its open loop transfer function can be described as

$$H(s) = \frac{-A_2}{\left(1+\dfrac{s}{\omega_1}\right)\left(1+\dfrac{s}{\omega_2}\right)\left(1+\dfrac{s}{\omega_3}\right)} =$$

$$\frac{-A_2}{\left[1+\dfrac{s}{\dfrac{1}{R_{out}(C_L+C_{Ap})}}\right]\left[1+\dfrac{s}{\dfrac{A_1 g_{mM}}{(C_P+C_{Bp})}}\right]\left[1+\dfrac{s}{\dfrac{g_m}{C_{Cp}}}\right]} \quad (6)$$

where R_{out}, C_L are the output resistance and load capacitor of the operational amplifier, C_{AP}, C_{BP}, C_{CP} are the parasitic capacitors at nodes A, B, C, respectively, A_1 is the DC gain of the operational amplifier in the peak-detector, g_{mM} is the transconductance of the transistor, Mp, in the peak-detector, and g_m is the transconductance of the g_m-cell, g_{m2}. Here the minimum static transconductance value is considered for the transistor Mp since it is time-varying. To guarantee stability, ω_1 is set to be the main pole, and ω_2 is set at least two times higher than the 0dB bandwidth to guarantee 60° phase margin and ω_3 is set high enough that it can be totally neglected. The 0dB bandwidth is set about ten times higher than the corner frequency introduced by the transformer so that robust canceling and high-speed response can be achieved.

Here the g_m-cell adopts the same structure as

used in the equalizer, which has about a 1V linear input range. Thus a large compensation range, about 1V, is achieved, which is sufficient for the worst case, about 750mV, defined by Ref. [15].

4 Measurement results

The equalizer and BLW canceller are designed and fabricated in 1st silicon 0.25μm CMOS technology. A die photograph is shown in Fig. 10, and the active area is 0.5mm^2. Measurement results of 40 samples using three different bands of CAT-5 cable indicate consistency in the performance. Figure 11 shows the eye-diagram of the un-
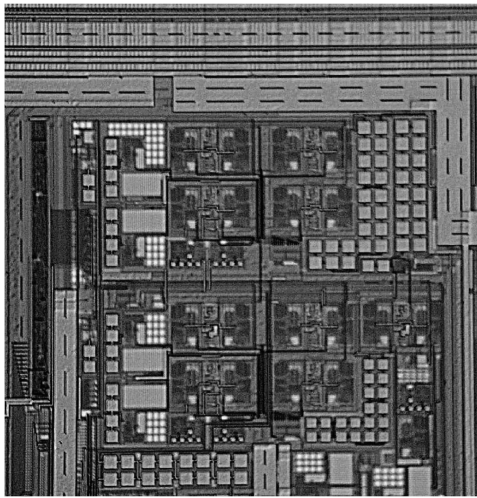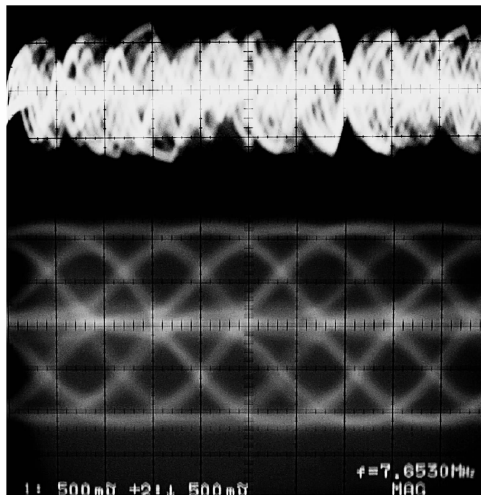
equalized/equalized signal through 100m CAT-5 cable and -3dB flat loss is added intentionally (It is somewhat distorted by the on-chip test buffer and the noise introduced by the FPGA board used for testing). Figure 12 shows the worst case BLW signal after and before the BLW canceller and the equalizer with 100m cable. The power consumption is 75mW. The circuits are incorporated in a fast Ethernet transceiver, and the measured BER is less than 10^{-12} with 100m cable. Table 1 summarizes the comparison of the results in the literature and this paper.
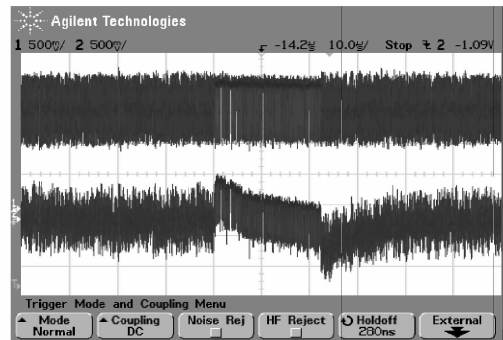

Fig. 10　Die photography

Fig. 11　100m cable worst case eye-diagram of un-equalized/equalized signal

Fig. 12　Signal after/before BLW canceller and equalizer with 100m cable

5 Conclusion

A frequency-domain equalizer with a mixed signal mode adaptive control loop and a novel BLW canceller have been proposed. Careful system level design ensures that the equalizer is channel-modeling accuracy independent. The equalizer also incorporates a flat loss compensation function without an extra AGC circuit. Mixed signal mode and time-divided control of equalization and flat loss compensation ensure the stability of the loop. The BLW canceller proposed uses a peak detector to monitor the BLW and a feedback method to achieve high canceling accuracy and robust performance. It is simple in structure but efficient in performance and silicon area. Better performance and smaller silicon area are achieved compared with other results in the literature.

Table 1   Comparison of this paper's result with the results in the literature

	Equalization method	Control method	Technology	Power consumption	Eye diagram openness	Die area
Ref.[1]	Digital implementation of time-domain equalizer	LMS algorithm	0.18μm 1P5M CMOS	350mW	About 60% open	6.6mm^2
Refs.[4,5]	Digital implementation of time-domain equalizer	LMS algorithm	0.18μm SEC CMOS	——	——	128,528 Gates （about 1.28mm^2）
Ref.[17]	Analog implementation of time-domain equalizer	LMS algorithm	——	80mW	——	1.0mm^2
Ref.[16]	1st order RC-active filter based frequency-domain equalizer	Continuous -time control loop	0.4μm 1P3M CMOS	65mW	poor	1.1mm^2
Ref.[11]	2nd order RC-active filter based frequency-domain equalizer	Programming	0.25μm CMOS	——	About 60% open	0.984mm^2
This paper	2nd order g_m-C filter based frequency-domain equalizer	Novel mixed-signal control loop	0.25μm 1P4M CMOS	75mW	About 70% open	0.5mm^2

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一种用于 100/1000 Base-TX 收发器的模拟均衡器和基线漂移消除电路 *

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摘要： 提出了一种用于 100/1000Base-TX 收发器的频域均衡器和新颖的基线漂移消除电路. 均衡器采用混和信号模式的自适应控制环路, 系统优化使其性能不依赖于信道模型的精确性, 控制环路稳定可靠, 该均衡器还同时实现自动增益控制功能；基线漂移消除电路采用峰值检测器监测基线漂移, 用负反馈思想实现漂移量的消除, 消除精度高, 性能可靠. 电路采用 $0.25\mu\mathrm{m}$ CMOS 工艺进行了硅片验证, 与文献结果相比, 本文方案在性能和芯片面积上均具有明显优势.

关键词： 均衡器；基线漂移；自适应控制环路

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