Total Ionizing Dose Radiation Effects on MOS Transistors with Different Layouts*

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Abstract: Both nMOS and pMOS transistors with two-edged and multi-finger layouts are fabricated in a standard commercial 0.6μm CMOS/bulk process to study their total ionizing dose (TID) radiation effects. The leakage current, threshold voltage shift, and transconductance of the devices are monitored before and after γ-ray irradiation. Different device bias conditions are used during irradiation. The experiment results show that TID radiation effects on nMOS devices are very sensitive to their layout structures. The impact of the layout on TID effects on pMOS devices is slight and can be neglected.

Key words: MOS transistor; layout; total ionizing dose; radiation effect
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1 Introduction

CMOS integrated circuit technology plays the most important role in electronic systems and has dominated the electronics industry for more than 30 years[1]. With increasing requirements for high performance systems in radiation environments, such as space and high-energy physics experiments[2~5], more and more integrated circuits must operate under exposure to radiation. Total ionizing dose (TID) radiation effects degrade the performance and reliability of MOS transistors and integrated circuits[1,6].

Radiation introduces both trapped oxide charges and interface traps, which cause a shift in the threshold voltage[1,6,7]. Oxide-trap charge is almost universally found to be net positive in MOS gate oxides[8], leading to a negative threshold voltage shift in both nMOS and pMOS transistors during radiation exposure. Interface trap charge is predominantly negative for nMOS transistors, leading to a positive threshold voltage shift, and positive for pMOS transistors, leading to negative threshold voltage shift[6,8]. The radiation-induced threshold voltage shift depends on oxide thickness according to a square law[9].

TID radiation also leads to leakage current for nMOS transistors. Trapped charge buildup in lateral oxide isolation regions (field oxide structures) increases transistor edge leakage current[10~12]. The leakage paths induced by the positive trapped charge in the thick field oxide occur at the transitional edges[13].

The purpose of this work is to analyze the TID radiation effects of MOS transistors in a standard commercial 0.6μm CMOS/bulk process with different layout structures by ^{60}Co γ irradiation experiments. The experimental results mainly focus on the increase of leakage current and the shift of the threshold voltage, as well as the transconductance change. The layout structures of test transistors, experiment conditions, and conclusions will be addressed.

2 Devices and experimental techniques

2.1 Test devices

The MOS transistors studied in this work were designed in a standard commercial 0.6μm CMOS/bulk process. The gate oxide thicknesses

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were in the range of 12.5～13nm. Both pMOS and nMOS transistors were designed with two different traditional layout structures without implementing any special radiation-hard techniques: a two-edged (standard single-stripe poly) transistor and a multi-finger (multi-stripe poly) transistor, as shown in Fig. 1. The channel lengths of all transistors were 0.6μm. The channel widths were 60μm for two-edged transistors, and 6×10μm for multi-finger transistors with six fingers in the layout.

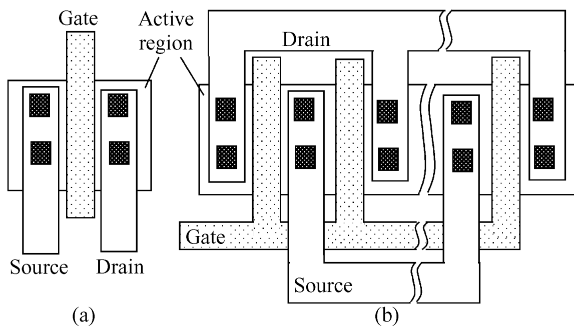

Fig.1 Layout structures of two edged transistor (a) and multi-finger transistor (b)

2.2 Experiment

Irradiation tests were carried out with γ-rays from a ^{60}Co source. Since MOS radiation damage effects have a strong bias dependence[6], both nMOS and pMOS transistors were biased under two different conditions during radiation exposure.

In the case of the nMOS transistors: (a) biased with 5V on the drain relative to gate, source and body ($V_{gs}=0$, $V_{bs}=0$, $V_{ds}=5V$); (b) biased with 5V on the gates, with all other terminals (source, drain, and body) grounded ($V_{gs}=5V$, $V_{ds}=0$, $V_{bs}=0$).

In the case of pMOS transistors: (a) biased with 5V on the drain, source, and body relative to the gate ($V_{gs}=-5V$, $V_{bs}=0$, $V_{ds}=0$); (b) biased with 5V on the gate, source, and body relative to the drain ($V_{gs}=0$, $V_{ds}=-5V$, $V_{bs}=0$).

The devices were irradiated with a total dose of about 9.5kGy(Si) at a rate of 1.58Gy(Si)/s. The edge leakage, threshold voltage shift, and transconductance were measured before and after irradiation at room temperature with $|V_{ds}|=0.8V$.

3 Results and discussion

3.1 Leakage current

Figure 2 shows the drain current versus gate voltage characteristics for nMOS transistors with two-edged and multi-finger layout structures at different gate-to-source voltage biases: $V_{gs}=0$ and $V_{gs}=5V$. After irradiation, leakage currents in the subthreshold region increase enormously. The transistors show different leakages depending on bias condition and layout structure.

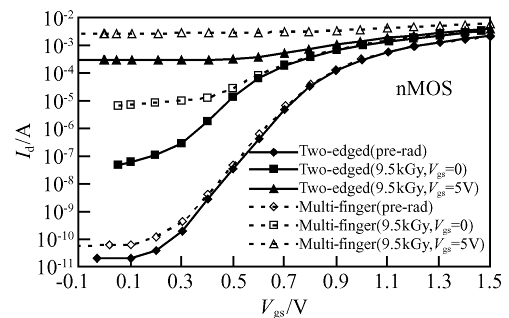

Fig.2 Drain current I_d versus gate voltage before and after irradiation for a two-edged nMOS transistor (solid lines) with $W/L=60\mu m/0.6\mu m$ and a multi-finger nMOS transistor (dashed lines) with $W/L=6\times10\mu m/0.6\mu m$ The devices were biased at $V_{gs}=0$ and 5V during irradiation. The total dose was 9.5kGy (Si) at 1.58Gy(Si)/s dose rate. The measurements were carried out with $V_{ds}=0.8V$.

Comparing results of the devices in two bias conditions, it can be noticed that for both layout structures, the leakage drain currents in the subthreshold region are unacceptable for the devices in the case of $V_{gs}=5V$, which are much larger than the leakages in the case of $V_{gs}=0$.

It is shown in Fig. 2 that the leakage drain currents of the multi-finger transistors are much larger than the leakages of the two-edged transistors under the same bias conditions during irradiation. The reason is that there are more transistor edges, which are possible leakage paths, in multi-finger transistors than in two-edged transistors, as shown in Fig. 1.

Unlike nMOS transistors, measurements of irradiated pMOS transistors show no different characteristics between the two-edged and multi-finger layout structures (Fig. 3). Although the leakage currents in pMOS transistors increase during irra-

diation, the magnitudes are very small, only a few tens of pA in the case of $V_{gs}=0$, several nA in the case of $V_{gs}=-5\text{V}$. These are much smaller than those observed in nMOS devices. Therefore the leakages of pMOS transistors can be neglected in most applications.

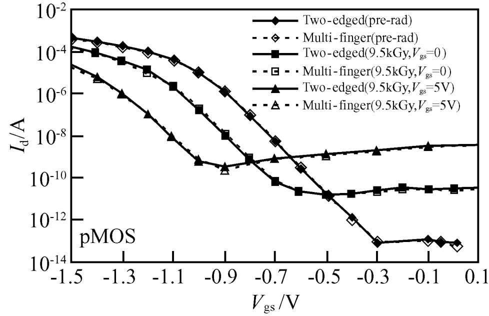

Fig.3　Drain current I_d versus gate voltage before and after irradiation for a two-edged pMOS transistor (solid lines) with $W/L=60\mu\text{m}/0.6\mu\text{m}$ and a multi-finger pMOS transistor (dashed lines) with $W/L=10\times 6\mu\text{m}/0.6\mu\text{m}$　The devices were biased at $V_{gs}=0$ and 5V during irradiation. The total dose was 9.5kGy (Si) at 1.58Gy(Si)/s dose rate. The measurements were carried out with $|V_{ds}|=0.8\text{V}$.

The results above show significant differences between nMOS and pMOS in terms of leakage characteristics. Because in the case of pMOS, the radiation-induced positive trapped charges in oxide decrease the width of the depletion region in n-substrate at the edges of the active region and field oxide beneath gate poly, which cannot lead any leakage paths. Therefore the leakage current in pMOS transistors remains low after irradiation, showing no difference between two-edged and multi-finger devices.

3.2　Threshold voltage shift

A key parameter for the evaluation of TID radiation effects on MOS transistors is the threshold voltage shift ΔV_{th}. In order to analyze the behavior of the oxide-trap and the interface-trap charges, we split the threshold voltage shift ΔV_{th} into a contribution due to interface traps ΔV_{Nit} and a contribution due to oxide-traps ΔV_{Not}, which are extracted from the curves in Fig.2 and Fig.3 using the techniques described in Ref.[7].

The post-radiation ΔV_{th}, ΔV_{Nit}, and ΔV_{Not} of both nMOS and pMOS transistors biased at $V_{gs}=0$ and $V_{gs}=5\text{V}$ (-5V for pMOS) during irradiation are shown in Table 1 and Table 2, respectively. These data confirm that ΔV_{Nit} is positive for nMOS transistors and negative for pMOS transistors, while ΔV_{Not} is negative for both nMOS and pMOS transistors, as described in Section 1. The gate bias voltage makes the radiation-induced electron-hole pairs separate quickly during irradiation, which decreases the recombination of the electrons and holes, leading to the trapping of more holes in the oxide. Therefore, the magnitude of ΔV_{Not} is larger for $V_{GS}=5\text{V}$ (or -5V) than for $V_{GS}=0$ during irradiation, especially for nMOS transistors. According to the data in Table 1 and Table 2, positive gate voltage leads to more negative interface traps in nMOS transistors, while negative gate voltage increases positive interface traps in pMOS transistors, but not so much as in nMOS transistors.

Table 1　Threshold voltage shifts for $V_{gs}=0$ during irradiation

Type	ΔV_{Nit}/V	ΔV_{Not}/V	ΔV_{th}/V
Two-edged nMOS	0.298	−0.536	−0.238
Multi-finger nMOS	1.102	−1.464	−0.362
Two-edged pMOS	−0.034	−0.133	−0.167
Multi-finger pMOS	−0.037	−0.124	−0.161

Table 2　Threshold voltage shifts for $V_{gs}=5\text{V}$ for nMOS and $V_{gs}=-5\text{V}$ for pMOS during irradiation

Type	ΔV_{Nit}/V	ΔV_{Not}/V	ΔV_{th}/V
Two-edged nMOS	3.984	−5.183	−1.199
Multi-finger nMOS	18.62	−25.62	−7.00
Two-edged pMOS	−0.092	−0.292	−0.384
Multi-finger pMOS	−0.118	−0.256	−0.374

For nMOS transistors with the multi-finger layout, the magnitude of ΔV_{Nit} and ΔV_{Not}, as well as ΔV_{th}, increases more than that of the devices with the two-edged layout. The total oxide-trapped charges in the multi-finger transistor are much more than that in the two-edged transistor because of the multiple edges. Since they have the same channel area, more trapped charges lead to a greater threshold voltage shift. Thus the threshold voltages of multi-finger transistors shift more.

As expected from the curves in Fig.3, the magnitude of the threshold voltage shift shows almost no difference between the pMOS transistors with different layout structures.

3.3 Transconductance

The transconductance is extracted from the I_d-V_{gs} curves in Fig.2 and Fig.3. The g_m behavior of nMOS devices in the drain current region up to 1mA is shown in Fig.4. The g_m in the case of $V_{gs}=0$ shows no change. The g_m of the two-edged transistor decreases from 35% (at $I_d=0.3$mA) to 8% (at $I_d=1$mA) in the case of $V_{gs}=5$V. With the large drain current after irradiation, the g_m of the multi-finger nMOS transistor is out of the plot region in Fig.4, but a large decrease can be expected from the curves in Fig.2.

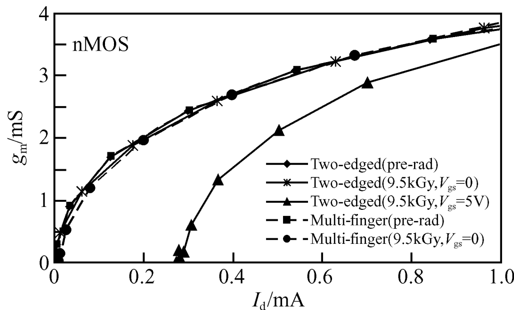

Fig.4 Transconductance g_m versus drain current I_d before and after irradiation for a two-edged nMOS transistor (solid lines) with $W/L=60\mu$m/0.6μm and a multi-finger nMOS transistor (dashed lines) with $W/L=6\times10\mu$m/0.6μm The devices were biased at $V_{gs}=0$ and 5V during irradiation. The total dose was 9.5kGy(Si) at 1.58Gy(Si)/s dose rate. The measurements were carried out with $V_{ds}=0.8$V. The line of multi-finger (9.5kGy, $V_{gs}=5$V) is out of plot region.

The transconductance of pMOS devices is shown in Fig.5 with the drain current region up to 20μA. In the operating region described by these plots, the transconductance approaches linear dependence on the drain current, because the devices are biased close to weak inversion. Since the g_m shows a small decrease (⩽3%) in Fig.5, the g_m of pMOS transistors has been affected by irradiation to a very limited extent.

The main reason for the transconductance decrease could be the reduction of carrier mobility due to the increase in interface traps after irradiation. The number of the interface traps N_{it} can be deduced from Table 1 and Table 2. The value of ΔV_{Nit} indicates the number of interface traps. The ΔV_{Nit}, and thus the N_{it}, in multi-finger nMOS is the largest, leading to the most severe degradation

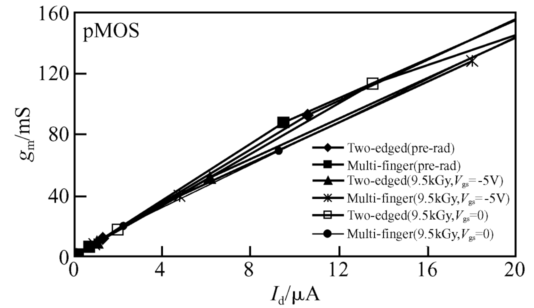

Fig.5 Transconductance g_m versus drain current I_d before and after irradiation for a two-edged pMOS transistor (solid lines) with $W/L=60\mu$m/0.6μm and a multi-finger pMOS transistor (dashed lines) with $W/L=6\times10\mu$m/0.6μm The devices were biased at $V_{gs}=0$ and 5V during irradiation. The total dose was 9.5kGy(Si) at 1.58Gy(Si)/s dose rate. The measurements were carried out with $V_{ds}=0.8$V.

of transconductance. The ΔV_{Nit}, and thus the N_{it}, in pMOS is the smallest, leading to negligible degradation of transconductance. That is in agreement with the results of transconductance decrease illustrated in Fig.4 and Fig.5.

Till now, there has been no effective design technique to eliminate the threshold voltage shift in both nMOS and pMOS transistors during irradiation. The leakage in nMOS devices could be mitigated by using the layout structure with no thick field oxide at the transistor edges, such as an enclosed-gate structure with p^+ guard rings[14].

4 Conclusion

The TID radiation effects on MOS transistors with two-edged and multi-finger layout structures have been studied by γ-ray irradiation experiments. The test devices were designed in a standard commercial 0.6μm CMOS/bulk process. The results show that the multi-finger layout increases the leakage current and the threshold voltage shift due to radiation in nMOS transistors. No significant variation in leakage current, threshold voltage, and transconductance have been observed between the pMOS transistors with different layouts. The experiment results also confirm that the TID radiation effects on MOS devices have a strong dependence on bias conditions during radiation.

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版图结构对MOS器件总剂量辐照特性的影响*

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摘要：在商用标准0.6μm体硅CMOS工艺下，设计了采用普通单栅及多栅版图结构的nMOS和pMOS晶体管作为测试样品，讨论其经过γ射线照射后的总剂量辐照特性.辐照中器件采用不同电压偏置，并在辐照前后对器件的源漏极间泄漏电流、阈值电压漂移及跨导特性进行测量.研究表明nMOS总剂量效应对器件的版图结构非常敏感，而pMOS的总剂量效应几乎不受版图结构的影响.

关键词：MOS晶体管；版图；总剂量；辐照效应

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