A Novel Low Power ASK Receiver with AGC Loop*

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Abstract: We report a low power ASK IF receiver for short-range wireless systems, which includes an AGC loop that compensates the channel attenuation and an ASK detector. A novel current-limited transconductor and feed-forward differential peak detector have been designed to maintain a high compression ratio and fast response for the AGC with lower power consumption. A storage unit with a zero and a feed-forward structure have been introduced into the peak detector to control the damping characteristic of the AGC loop. A rectifier and low-pass filter included in the ASK detector have been integrated into a more compact structure to further lower the power consumption. The simulation results show the feasibility of the proposed technique.

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1 Introduction

Nowadays, low-power low-cost short-range wireless data communication systems, such as implantable electronic devices (IEDs)[1] and wireless sensor networks[2], are becoming more and more popular, and they are likely to expand dramatically in the future. Because amplitude shift-keying (ASK) modulation enables much simpler system architecture, which means low power consumption and low cost, it is an attractive candidate modulation scheme for these systems, in which power efficiency rather than spectrum is the specification of greatest concern.

In a receiver for ASK modulation, the signal strength has to be well controlled in order for the ASK detector to compensate the attenuation induced by the unstable channel. Because the information is carried in the amplitude of the ASK signal, an automatic gain control (AGC) loop, which performs a linear controlling, must be used. Therefore, the design of an AGC loop that consumes lower power without loss path gain is an issue of interest.

This paper presents an ASK IF receiver containing an AGC loop and an ASK detector, which features low power consumption, compact size, and robust demodulation. Though the IF receiver is designed for a wireless endoscopy capsule system[3], where a 10MHz ASK IF signal with 40dB dynamic range has to be demodulated, the proposed techniques are not limited to the application.

2 Circuit descriptions

The proposed ASK IF receiver is shown in Fig. 1. A two-stage variable gain amplifier (VGA) and a constant gain amplifier (CGA) compose the forward gain path, while a differential peak detector (PeakDET) and a transconductor with limited output current (LimGm) compose the feedback path. Both forward and feedback paths form the AGC loop, by which the IF ASK signal with variable strength is amplified to a signal with well-defined amplitude whose envelope is set by a tunable reference generator (RefGen). The output of the AGC is then discriminated by an ASK detector (ASKDET). Two OTA-C integrators around VGA and CGA regulate the frequency characteristics of the forward gain path to 2nd-order band pass, which enables compact DC-coupling between the VGA and CGA and reduces the

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low frequency noise from the RF front end.

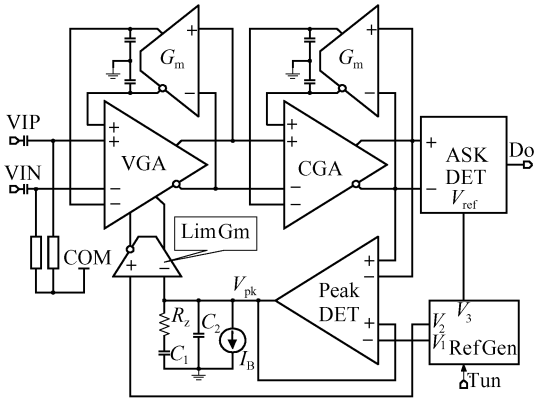
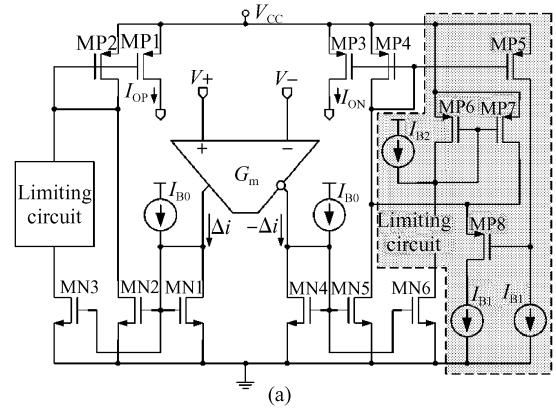


Fig. 1 Block diagram of the proposed receiver

Since the AGC is a closed loop system, the stability is a critical issue. Because the average power of the ASK signal varies with the amount of information carried, only the peak value can be used to tune the gain of the VGA. Since the peak detector is unilateral, the stability requirement is more rigorous, because any overshoot makes the loop lose track of the input signal until the peak value storage capacitor has discharged enough, which normally occurs rather slowly. Conventionally, the VGA gain is controlled by a voltage produced by an error amplifier, where the error between the detector's output and a setpoint voltage is amplified[4,5]. If the error amplifier has a low gain, the AGC output is not so well-defined, which means a higher error bit rate. If it has a high gain, the induced pole cannot be ignored. For keeping such a loop stable, either a large capacitor, which results in a lagged response, or high power consumption is necessary. The proposed AGC loop circumvents this tradeoff by using a transconductor with limited output current and a current-controlled VGA. The transconductor converts the error between V_{pk} and V_2 (Fig. 1) to a controlling current, with which the gain of the VGA is tuned to a suitable value. For having no high voltage gains, the transconductor introduces no notable poles when it is loaded by diodes. Furthermore, the error of the AGC output can be lowered enough when the transconductance is high enough.

To achieve a wider gain tuning range and keep a relatively stable loop dynamic under different input signal strengths[5], a two-stage VGA with almost exponential gain control is used, which is the cascade of the circuit proposed by Huang *et al*.[6]. Since the gain control curve of the VGA becomes steeper than an exponential curve when the differential control current is too large, which could destabilize the AGC loop, the output current of the transconductor (LimGm in Fig. 1) should be limited. Figure 2 (a) shows a schematic of LimGm. When $I_{MN4} < I_{B1}$, MP6 and MP7 are switched off and MP8 is turned on, I_{ON} cannot be less than I_{B1}. When $I_{MN4} > I_{B2}$, MP8 is switched off and $I_{MP6} = I_{MN4} - I_{B2}$, and then $I_{ON} = I_{MN4} - (I_{MN4} - I_{B2})$; therefore I_{ON} cannot be larger than I_{B2}. When $I_{B1} < I_{MN4} < I_{B2}$, both MP7 and MP8 are shut down, so $I_{ON} = I_{MN4} = I_{B0} - \Delta i$. I_{OP} is limited with the same behavior. The simulation result of the gain control curve is shown in Fig. 2 (b). It is evident that the gain has been limited within ±30dB. Palmisano's amplifier[7] is used as the CGA. When the AGC loop is closed, the differential peak value of the AGC output is set at $V_2 - V_1$ (Fig. 1).



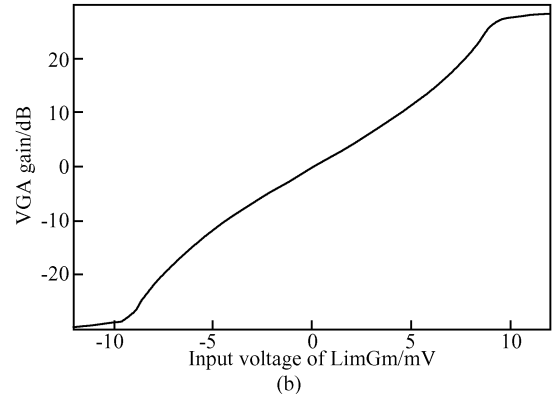


Fig. 2 (a) Schematic of the limiting transconductor; (b) VGA gain control curve

To prevent the common-mode fluctuation from debasing the accuracy of the AGC output strength, the differential peak value is used to control the VGA. For the conventional peak detector[8] detecting a single-end signal only, two of such detectors, which detect peak and valley value respectively, have to be used. The proposed detector shown in Fig. 3 detects the differential peak value directly, which means higher power efficiency. It is a feed-forward differential difference amplifier followed by a current mirror used as a rectifier. When the output current of MP8 is integrated by the storage unit and V_{pk} is fed back, $V_{pk} - V_{CM}$ will converge at the peak value of the differential signal between IP1 and IN1. Two gain stages have been cascaded to keep the error of the peak value low enough. MN5 and MP6 compose the feed forward path, which compensates the phase without a capacitor. The storage unit is composed of C_1, C_2, and R_z. R_z induces a zero which, cooperating with the feed-forward structure, helps to control the AGC loop's damping characteristic, which has been achieved conventionally by increasing loop components' bandwidth meaning higher power cost.

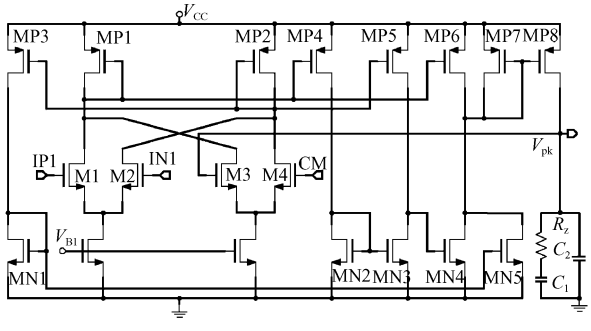


Fig. 3　Schematic of the peak detector

The proposed ASK detector, in which a rectifier and subsequent low-pass filter have been integrated into a more compact structure, resulting in lower power consumption, is shown in Fig. 4. All four transconductors, annotated as G_m, are identical. The voltage signal is converted by $G_{m1\text{-}2}$ to a current signal, which is rectified to I_{rec} by MP1～MP4. I_{rec} is then filtered and converted back to a voltage that indicates the signal strength by $G_{m3\text{-}4}$ and $C_{1\text{-}2}$. The voltage is given by

$$V_{FOUT} = V_{COM} + \frac{2}{\pi}A \approx V_{COM} + 0.64A \quad (1)$$

where A is the envelope amplitude of the differential input. V_{FOUT} is compared with V_{ref} by a hysteresis comparator to regenerate the information carried by the ASK. V_{ref} is set at V_3 (Fig. 1) by RefGen.

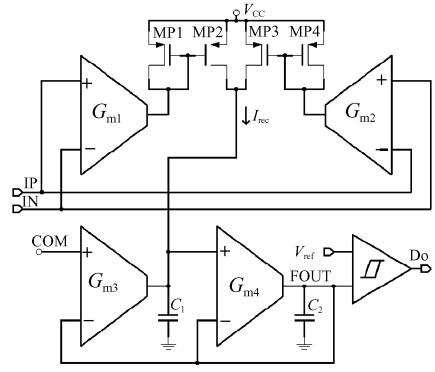


Fig. 4　Schematic of ASK detector

3　Simulation results

The scheme by which the IF receiver demodulates the ASK signal with a 10MHz carrier has been implemented in a UMC 0.18μm CMOS process. The whole chip draws about 4mA current from a 1.8V power supply. The die area, including buffers for test and PADs, is about 1.3mm × 1.5mm. The layout is shown in Fig. 5.

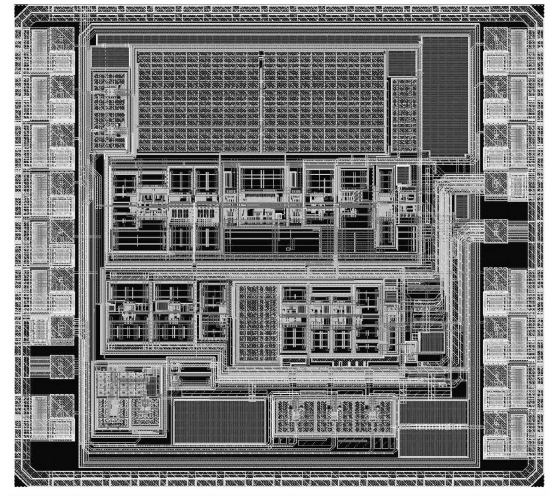


Fig. 5　Layout of the chip

The AGC compression characteristic is shown in Fig. 6. The figure indicates that the AGC stabilizes the output when input signal's amplitude is between 60μV and 50mV. Outside the range, the VGA controlling current is limited, so any change

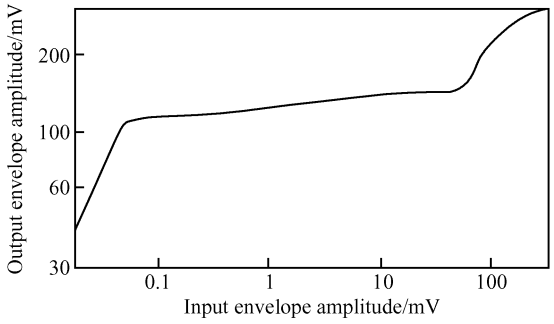


Fig. 6 Simulated AGC characteristic

in input results in an identical change in AGC output, until the forward path is saturated. Figure 7 gives the step response of the AGC loop, where Figure 7(a) is the AGC input, Figure 7(b) is the response of the proposed AGC, and Figure 7(c) is the response of the same AGC but with no feed-forward in the peak detector and no R_z. It is shown that the overshoot appearing in Fig. 7(c) has been erased in Fig. 7 (b), which means that the loop damping characteristic has been adjusted by R_z and the feed-forward structure. The simulated results of the ASK detector are given in Fig. 8, where information has been recovered correctly.

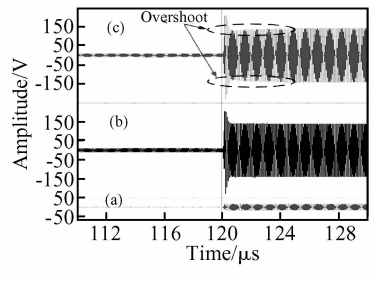


Fig. 7 Simulated loop dynamic of AGC loop

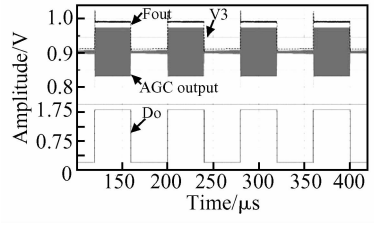


Fig. 8 Simulated results of ASK detector

4 Conclusion

An ASK IF receiver with some improved circuits has been presented. The conventional error amplifier in AGCs, which suffers the tradeoff between lagging response and high power consumption, is replaced by a current-limited transconductor, and then a fast response with lower power cost can be achieved. A novel peak detector that can detect the differential peak value directly has been presented. Compared with the conventional methods, where peak and valley values are detected respectively, the proposed detector saves power. A compact ASK detector and some techniques for damping adjustment without additional power cost have also been proposed. The feasibility of the proposed circuits has been verified by simulations.

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一个新型的带自动增益控制环路的低功耗 ASK 接收机*

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摘要：实现了一个适用于短距离无线系统的低功耗 ASK 中频接收机电路.该接收机包括一个用于补偿信道衰减的自动增益控制环和一个 ASK 检波器.自动增益控制环中采用了新型的限流跨导器和带前馈的差分峰值检测器，从而以较低的功耗实现了较高的压缩比及较快的响应速度.通过在峰值存储单元中引入零点及在峰值检测电路中引入前馈，实现了对自动增益控制环阻尼特性的调整.ASK 检波器中传统的整流器和低通滤波器被整合为更紧凑的结构，从而进一步降低了功耗.仿真结果验证了本文所提技术的有效性.

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