Realizing High Breakdown Voltage SJ-LDMOS on Bulk Silicon Using a Partial n-Buried Layer*

Chen Wanjun†, Zhang Bo, and Li Zhaoji

(*Center of IC Design, University of Electronic Science and Technology of China, Chengdu 610054, China*)

Abstract: A new design concept is proposed to eliminate the substrate-assisted depletion effect that significantly degrades the breakdown voltage (BV) of conventional super junction-LDMOS. The key feature of the new concept is that a partial buried layer is implemented which compensates for the charge interaction between the p-substrate and SJ region, realizing high breakdown voltage and low on-resistance. Numerical simulation results indicate that the proposed device features high breakdown voltage, low on-resistance, and reduced sensitivity to doping imbalance in the pillars. In addition, the proposed device is compatible with smart power technology.

Key words: super junction; LDMOS; breakdown voltage; substrate-assisted depletion effect
EEACC: 2560; 2560P **PACC**: 7340Q
CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2007)03-0355-06

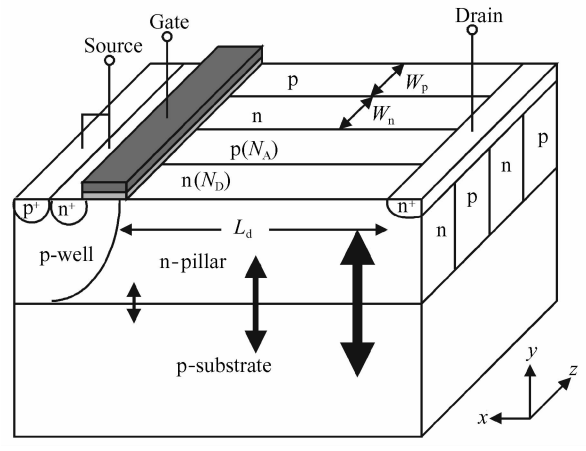
1 Introduction

The development of smart power IC (SPIC) is driven by the rapid growth in applications of motor control, electronic ballasts, switched mode power supplies, and other related technologies[1]. The key component used in SPIC that dominates these functions is the LDMOS device. One of the main issues concerning the design of LDMOS is the trade-off between breakdown voltage (BV) capability and the on-resistance (R_{on}). Recently, a new device called the super junction (SJ) device has been gaining attention because it can be used to achieve significant improvement in the tradeoff between on-resistance and breakdown voltage as compared to conventional devices. The SJ concept is based on achieving charge compensation in the off-state, in a set of alternating and heavily doped n and p pillars comprising the drift region of the device. Provided that the pillars of SJ are fairly narrow and net dopants in both pillars are approximately equal, it is possible to deplete the pillars at a relatively low voltage. Upon depletion, the pillars appear to be an "intrinsic" layer and a near uniform electric field is achieved, resulting in a high BV[2~7].

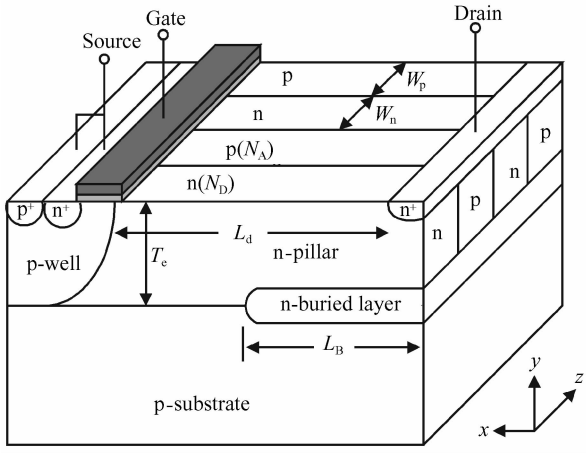
However, the SJ concept has not yet been widely applied in lateral power devices because the SJ-LDMOS implemented on a p-substrate results in a charge interaction between the p-substrate and SJ region, as shown in Fig. 1 (a), which is called the "substrate-assisted depletion effect". Then the behavior of the structure deviates from the above ideal description, which significantly degrades the BV of the SJ-LDMOS device[7~11]. In order to increase breakdown voltage capability, several solutions have been proposed to eliminate the substrate-assisted depletion effect. An SJ/R-LDMOS structure was reported in which the drift region was split into an SJ region and RESURF region with different doping concentrations[8]. However, it is difficult to form the different doping concentrations for the SJ region and RESURF region. Furthermore, a USJ-LDMOS was developed on SOI which also can be applied to bulk silicon[10]. Unfortunately, it requires both a tight layout and high process tolerances. Another possible solution to suppress the substrate-assisted depletion effect is the use of an n-buffer layer between the p-substrate and SJ region[11].

In this paper, a novel SJ-LDMOS using a partial n-buried layer is proposed. A more uniform surface electric field is obtained due to the suppression of the substrate-assisted depletion effect, which results in high BV and low on-resistance.

* Project supported by the National Natural Science Foundation of China (Nos. 60436030, 60576052)
† Corresponding author. Email: cwjzcz@yahoo.com.cn
Received 7 September 2006, revised manuscript received 23 October 2006



(a)



(b)

Fig. 1 Three-dimension view of the conventional SJ-LDMOS (a) and proposed SJ-LDMOS (b)

Furthermore, the proposed device allows the integration of lateral power devices based on the SJ concept into mainstream and low-cost CMOS/BiCMOS technology without any additional processes.

2 Device structure and operation

The basic cell of the proposed structure is shown in Fig. 1 (b). In the conventional SJ-LDMOS (called the conventional device), pn junctions are formed between the n-pillars and the p-substrate, resulting in a vertical electric field component $E_y(x)$ which is a function of lateral position in the drift region. The vertical electric field component gives rise to a surplus of p-type charge in the p-pillars and upsets the delicate charge balance between the n-and p-pillars in the off-state. Generally, the charge imbalance in the pillars leads to reduced BV[9]. In the proposed SJ-LDMOS (called the proposed device), an n-buried layer is implemented between the p-substrate and SJ pillars in order to suppress the substrate-assisted depletion effect, resulting in an improvement in BV. This is due to the fact that the depletion between the p-pillars and the n-buried layer causes the reduction of the charge density in the p-pillars, which compensates for the lack of charge in the n-pillars caused by the depletion between the n-pillars and p-substrate. However, the substrate-assisted depletion effect is most significant near the drain and less effective near the channel, as evident from the equipotential contours in Fig. 2 (a) for the conventional device. Thus, it is important that the n-buried layer is only partially under the drain contact region, which is different from the n-buffered SJ-LDMOS where the n-buffered layer is under the entire drift region.

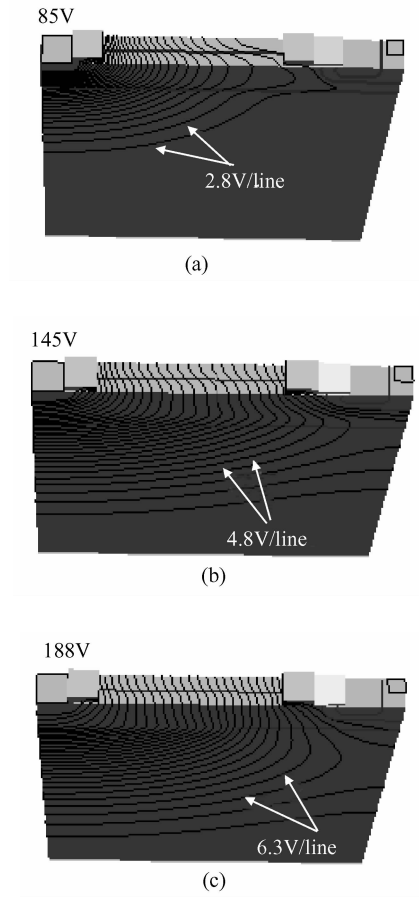


Fig. 2 Equipotential contours plotted at the breakdown voltage (a) Conventional SJ-LDMOS; (b) n-buffered SJ-LDMOS; (c) Proposed SJ-LDMOS

3　Simulation results and discussions

3D device simulation for the proposed SJ-LDMOS was performed using ISE[12]. We will compare the BV at the device parameters shown in Table 1. Figure 2 shows the equipotential contours at the BV for the different devices. It is clear that the space of the equipotential lines in the proposed device are more uniform than those of its counterparts, resulting in a breakdown voltage of 188V in the proposed device, compared to 85 and 145V in the conventional SJ-LDMOS and n-buffered SJ-LDMOS, respectively. Figure 3 (a) shows the vertical electric field near the drain terminal. It is clear that for the proposed device, a new electric field peak occurs at the pn junction between the p-substrate and n-buried layer which reduces the surface electric field, i.e., the n-buried layer suppresses the charge interaction between the p-substrate and SJ region, resulting in improvement in BV.

Table 1　Device specifications

Parameter	Conven.	n-buffered	Proposed
Drift length, $L_d/\mu m$	8.0	8.0	8.0
Gate length, $L_g/\mu m$	1	1	1
n-pillar doping, N_D/cm^{-3}	2×10^{16}	2×10^{16}	2×10^{16}
p-pillar doping, N_A/cm^{-3}	2×10^{16}	2×10^{16}	2×10^{16}
Pillar width, W_n, $W_p/\mu m$	1	1	1
Epi thickness, $T_e/\mu m$	2	2	2
Buried dose, Q_B/cm^{-3}	—	1.4×10^{12}	3×10^{12}
Buried length, $L_B/\mu m$	—	8	5
Sub doping, N_S/cm^{-3}	5×10^{14}	5×10^{14}	5×10^{14}

The BV improvement of the proposed device can also be explained by the electric field modulation effect. Since the partial n-buried layer is implemented between the SJ region and p-substrate, the electric field peak occurs near the buried layer regions at the bottom surface of the epitaxial layer in the off-state. The electric field peak near the buried layer modulates the electric field distribution at the top surface of the epitaxial layer, causing a uniform distribution of the surface electric field as shown in Fig. 3 (b). Through optimizing the dose of the n-buried layer, the optimal modulation effect can be obtained and the optimization of BV is achieved.

The dose Q_B and the length L_B of the n-buried layer are important parameters in the design

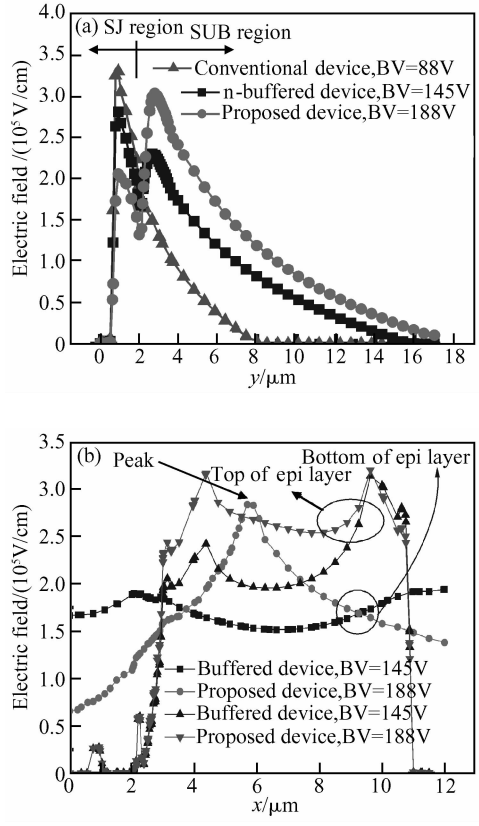


Fig. 3　Electric field distributions for different devices (a) Vertical electric field distributions near the drain terminal ($x = 10\mu m$, and the z axis located in the n-pillar center); (b) Lateral electric field distributions at the bottom ($y = 5\mu m$, and the z axis located in the p pillar center) and the top surface ($y = 0\mu m$, and the z axis located in the p-pillar center) of the epitaxial layer

of the proposed device. Figure 4 shows the dependence of the BV on the length L_B. It is clearly shown that there is an optimal value L_B for the maximum BV of the proposed device. At smaller values of the length L_B, the n-buried layer is only located under the drain region, which cannot completely compensate for the charge imbalance in the entire drift region, resulting in the low BV. However, at larger values of the length L_B, the n-buried layer is nearer the channel region, and only low dose Q_B can be depleted by the low potential of the channel region. The low dose Q_B cannot completely suppress the substrate-assisted depletion effect, especially near the drain region. Therefore, the BV of this case is low, too. In fact, the n-buffered SJ-LDMOS is like this case. The optimal length $L_{B.Opt}$ for our condition is $5\mu m$, for which BV reaches 188V. The conventional SJ-LD-

MOS and n-buffered SJ-LDMOS can be treated as the specific cases of the proposed device at $L_B = 0$ and $L_B = 8$, respectively. Obviously, the BV of the proposed device with an optimal length is larger than those of its counterparts.

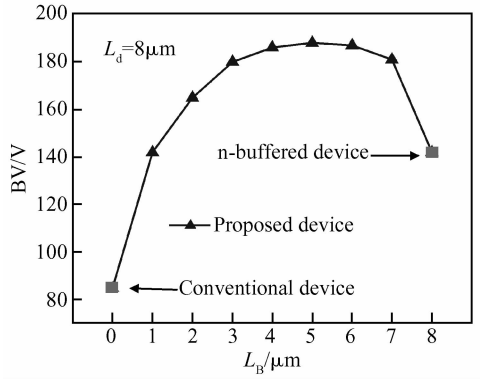


Fig. 4 BV versus the length of the n-buried layer

Figure 5 shows the BV versus the dose Q_B of the n-buried layer for three typical cases ($L_B < L_{B.Opt}$, $L_B = L_{B.Opt}$, $L_B > L_{B.Opt}$). It is shown that, firstly, there is an optimal value Q_B for a certain length of n-buried layer. Secondly, the optimal value Q_B increases as the length of n-buried layer is reduced. Moreover, to obtain the maximum BV for a certain length, the process tolerance also increases with the reduction of the length of the n-buried layer. It is advantageous to achieve a low on-resistance with a high BV.

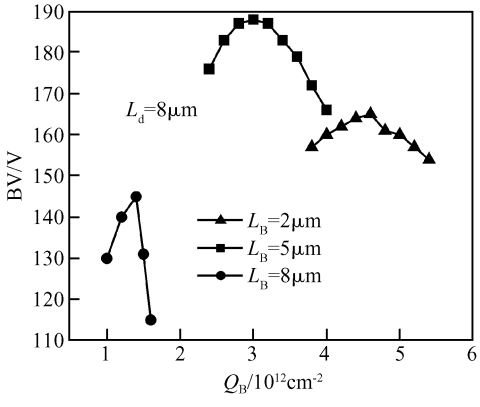


Fig. 5 BV as a function of the n-buried layer dose

The effect of the doping imbalance on the BV for the proposed device and n-buffered device are compared in Fig. 6. It can be seen from this figure that the proposed device has almost the same sensitivity to doping imbalance as the n-buffered device for the same doping concentration. This is due to the partial n-buried layer which contributes to the balance between the n-pillar and p-pillar of SJ.

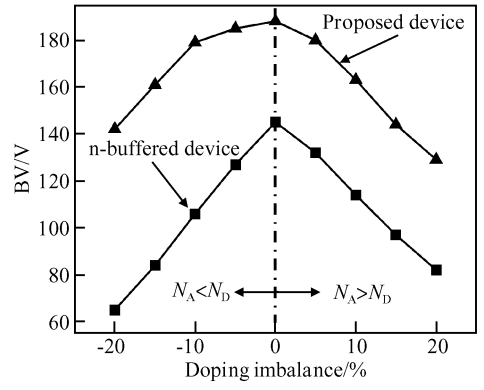


Fig. 6 Dependences of the BV on doping imbalance

The on-state characteristics have been compared. The simulation results are shown in Fig. 7 (a). It is clear that the proposed device and n-buffered device have almost similar on resist-

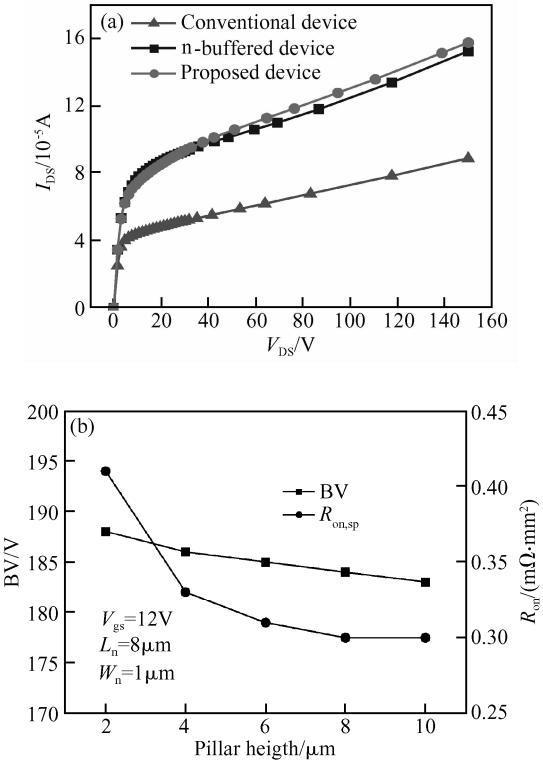


Fig. 7 (a) On-state characteristics of the conventional, n-buffered, and proposed devices when V_{gs} = 12V; (b) Dependence of the BV and specific on-resistance on pillar height of the proposed device

ances, which have a superior on-state characteristic to that of the conventional device. The improvement in the on-state characteristics must be due to the highly doped n-buried layer. In fact, the on-resistance of the SJ-LDMOS decreases with inverse proportion of aspect ratio, as expressed in Ref.[8]:

$$R_{\mathrm{on,sp}} \cong KL_{\mathrm{d}}^{2}\frac{w}{h} = KL_{\mathrm{d}}^{2}\frac{1}{\alpha} \qquad (1)$$

Here K is a constant, α is the aspect ratio, and w and h are the pillar width and height of the SJ region, respectively. Figure 7 (b) shows the dependence of the BV and specific on-resistance on the pillar height of the proposed device. In this picture, the BV of the proposed device remains almost constant while the specific on-resistance decreases with the increase in the pillar height.

The proposed SJ-LDMOS is compatible with smart power technology. Before the n epitaxial layer is grown, the n-type buried layer is implemented. Then the alternate n- and p-pillars drift region and other processes are formed like those of a conventional SJ LDMOS.

4 Conclusions

A novel SJ-LDMOS with partial n-buried layer is proposed that realizes high breakdown voltage and low on-resistance (R_{on}). The proposed structure overcomes the substrate-assisted depletion effect, thus achieving the charge compensation between the n- and p-pillars as well as a near uniform electric field distribution in the drift region in the off-state. The n-buried layer also provides a low current path in the on-state. In addition, the proposed device is compatible with smart power technology.

References

[1] Chen Wanjun, Zhang Bo, Li Zehong, et al. Design and optimization of a versatile 700V SPIC process using a fully implanted triple-well technology. Proc ISPSD, 2006: 269

[2] Chen X B, Johnny K O. Optimized of the specific on-resistance of the COOLMOSTM. IEEE Trans Electron Devices, 2001, 48: 344

[3] Chen X B, Mawby P A, Board K, et al. Theory of a novel voltage sustaining layer for power devices. Microelectronics Journal, 1998, 29: 1005

[4] Zhang Bo, Xu Zhenxue, Huang A Q. Analysis of the forward bias safe operation area of the super junction MOSFET. Proc ISPSD, 2000: 61

[5] Chen X B. Semiconductor power devices with alternating conductivity. US Patent, 5216275, 1993

[6] Strollo A G M, Napoli E. Optimized on - resistance versus breakdown voltage tradeoff in superjunction power device: a novel analytical model. IEEE Trans Electron Devices, 2001, 48: 2161

[7] Udrea F. Advanced 3D RESURF devices for power integrated circuits. Proceedings of CAS Semiconductor Conference, 2002, 2: 229

[8] Nassif-Khalil S G, Hou L Z, Salama C A T. SJ/RESURF LDMOS. IEEE Trans Electron Devices, 2004, ED-51: 1185

[9] Nassif-Khalil S G, Salama C A T. Super-junction LDMOS on a silicon-on-sapphire substrate. IEEE Trans Electron Devices, 2003, ED-50: 1385

[10] Ng R, Udrea F, Sheng K, et al. Lateral unbalanced super junction (USJ)/3D-RESURF for high breakdown voltage on SOI. Int Symp Power Semiconductor Devices and ICs, 2001: 395

[11] Park I Y, Salama C A T. CMOS compatible super junction LDMOST with n-buffer layer. Proc ISPSD, 2005

[12] ISE TCAD Manuals, Release 10.0

具有部分 n 埋层的高压 SJ-LDMOS 器件新结构*

陈万军† 张 波 李肇基

(电子科技大学 IC 设计中心，成都 610054)

摘要：针对衬底辅助耗尽效应降低常规 super junction LDMOS(SJ-LDMOS)击穿电压的不足，提出了一种新的具有部分 n 埋层的高压 SJ-LDMOS 器件结构.通过该部分 n 埋层，不仅补偿了由于衬底辅助效应所致的电荷不平衡现象，实现了高的击穿电压，而且该埋层在器件正向导通时为电流提供了辅助通道，减小了器件导通电阻.分析了器件结构参数和参杂对器件击穿电压和导通电阻的影响，结果表明文中所提出的新结构具有高的击穿电压、低的导通电阻以及较好的工艺容差等特性.此外，该结构与智能功率集成技术兼容.

关键词：超级结；击穿电压；LDMOS；衬底辅助耗尽效应

EEACC：2560；2560P **PACC**：7340Q

中图分类号：TN386 **文献标识码**：A **文章编号**：0253-4177(2007)03-0355-06

* 国家自然科学基金资助项目(批准号：60436030，60576052)

† 通信作者.Email：cwjzcz@yahoo.com.cn

2006-09-07 收到，2006-10-23 定稿