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A Monolithic Integrated Logic Circuit of Resonant Tunneling Diodes and a HEMT

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Abstract: A technology for the monolithic integration of resonant tunneling diodes (RTDs) and high electron mobility transistors (HEMTs) is developed. Molecular beam epitaxy is used to grow an RTD on a HEMT structure on GaAs substrate. The RTD has a room temperature peak-to-valley ratio of 5.2∶1 with a peak current density of 22.5kA/cm^2. The HEMT has a 1μm gate length with a −1V threshold voltage. A logic circuit called a monostable-to-bistable transition logic element (MOBILE) circuit is developed. The experimental result confirms that the fabricated logic circuit operates successfully with frequency operations of up to 2GHz.

Key words: MOBILE; RTD; HEMT; InGaAs; GaAs
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1 Introduction

A variety of ultra-dense and ultrahigh-speed integrated digital logic circuit applications for RTDs have been reported[1,2]. The RTD's feature of negative differential resistance (NDR) allows a significant reduction of circuit complexity and reduces power consumption[3], while their very fast switching capability makes them suitable devices for high-speed circuits.

RTDs have been integrated with high electron mobility transistors (HEMTs) since the fabrication is relatively simple and HEMTs exhibit high transconductance and excellent high-frequency characteristics. The HEMT gate recessing was formed by a highly selective low-Al mole fraction GaAs/AlGaAs heterojunction selective wet etching[4,5], which can achieve a uniform and reproducible threshold voltage.

In this paper, a type of logic circuit called a monostable-bistable transition logic element (MOBILE)[6] that employs resonant tunneling diodes and HEMTs is proposed. After briefly explaining MOBILEs, we present the experimental results of a logic circuit that is fabricated by integrating GaAs-based RTDs and HEMTs. These results confirm the validity of the basic idea of the logic operation.

2 Operation principle

We will explain MOBILEs, which exhibit two functions, that is, down and up literals. As shown in Fig.1, a MOBILE is composed of two series-connected RTDs, A and B, and one HEMT. RTD B is connected parallel to the HEMT, and the HEMT can modulate the RTD's peak current. A clock voltage (V_{clock}) between V_1 (low) and V_2 (high) is supplied to the circuit. When the cir-

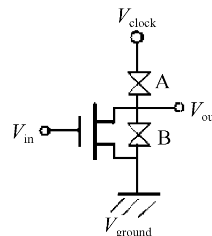

Fig.1 Circuit configuration of the MOBILE

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cuit voltage V_{clock} is V_1, the circuit is monostable. There is only one output voltage value (low) when both RTDs are in the "on" (low-resistance) state. As V_{clock} changes from V_1 to V_2, the circuit evolves from the monostable state to the bistable state, and there are then two output voltage values. V_2 is selected so that either A or B switches from the "on" state to the "off" (high resistance) state when $V_{clock} = V_2$. If B switches to the "off" state and A remains in the "on" state, the output is V^H (high), because the voltage between the terminals of B increases as B switches off. In a similar manner, if A switches off and B remains on, the output is V^L (low). The output is thus determined at the rising edge of the clock voltage.

For the modulation of the RTD peak current, which is indispensable for the logic operation proposed here, the RTDs and the HEMT are connected in parallel. NDR appears in the *I-V* characteristics of this parallel connection because the total current flowing through the parallel connection is the sum of the RTD current and the HEMT drain current. The HEMT gate voltage controls the total current and thus the effective peak current as well. The peak current of RTD A and the effective peak current of HEMT and RTD B control which RTD is in the "off" state and which RTD is in the "on" state.

3 Experiment and results

A schematic cross-section of the fabricated device is shown in Fig. 2. The RTD is grown on the HEMT on a semi-insulating GaAs substrate by molecular beam epitaxy (MBE). For the structure of the HEMT, we grew a 10 period 18.5nm/1.5nm AlGaAs/GaAs superlattice layer, an undoped (ud-) GaAs buffer layer, a 12nm ud-InGaAs channel layer, a 4nm ud-AlGaAs spacer layer, a δ-doped (3×10^{12} cm^{-2}) layer, a 30nm ud-AlGaAs barrier layer, a 100nm n^+-GaAs (5×10^{18} cm^{-3}) cap layer, and a 4nm ud-AlAs etch stop layer. For the RTD, we grew a 150nm n^+-GaAs (5×10^{18} cm^{-3}) layer, a 10nm n-GaAs (5×10^{17} cm^{-3}) cathode layer, a 10nm n^--GaAs (5×10^{16} cm^{-3}) spacer layer, a 5nm ud-GaAs spacer layer, a double barrier quantum well (DBQW) with AlAs(1.7nm)/GaAs(5nm)/AlAs(1.7nm), a 1.2nm $Al_{0.24}Ga_{0.76}As$ 'chair' barrier layer, a 5nm ud-GaAs spacer layer, a 10nm n^--GaAs (5×10^{16} cm^{-3}) spacer layer, a 10nm n-GaAs (5×10^{17} cm^{-3}) anode layer, and finally a 200nm n^+-GaAs (5×10^{18} cm^{-3}) ohmic contact layer.

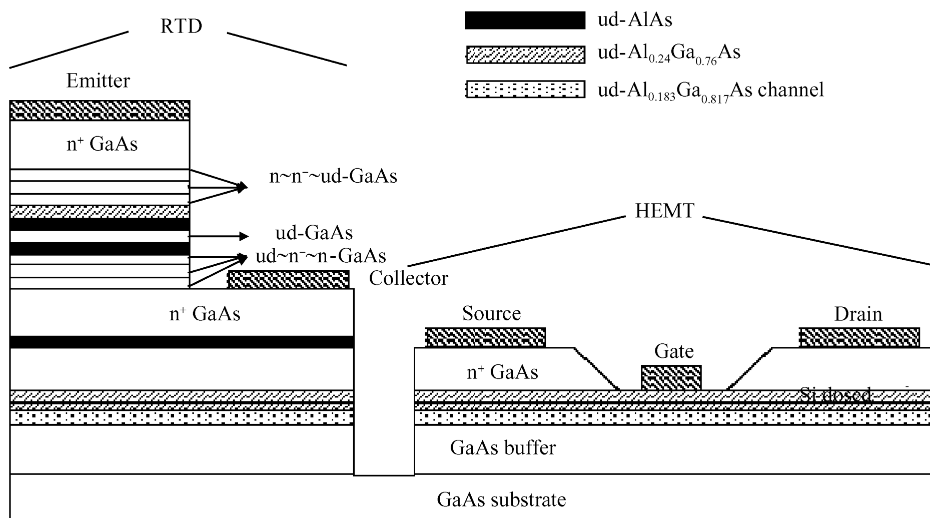

Fig. 2　Schematic cross-section of the fabricated device

The device processing employed standard optical lithography, III/V semiconductor wet etching, highly selective low-Al mole fraction GaAs/AlGaAs heterojunction selective wet etching, and evaporated metal liftoff patterning techniques.

Figure 3 shows the *I-V* characteristics of RTD A at room temperature. The RTD has a peak current density of 22.5kA/cm^2, a room tempera-

ture peak-to-valley ratio of 5.2 ∶ 1, and a peak voltage of 0.45V.

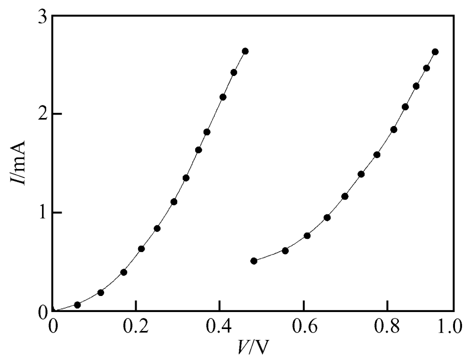

Fig.3 *I-V* characteristics of RTD A with an area of 6μm×10μm at room temperature

Figure 4 shows the *I-V* characteristics of the parallel connection of RTD B with the HEMT. A current peak due to the sequential switching of the RTDs was observed. The peak current increased as the HEMT gate voltage increased, as mentioned above. The HEMT device is in depletion-mode and therefore has a negative threshold voltage of −1V.

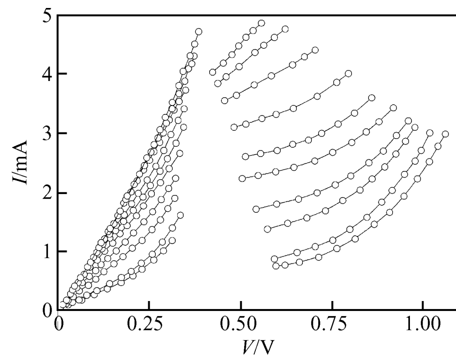

Fig.4 *I-V* characteristics of an integrated device in which RTD B is connected parallel to the HEMT

To obtain an inverter operation, the peak current of RTD B must be smaller than that of RTD A, and the maximum peak current of the parallel connection of RTD B and the HEMT must be larger than that of RTD A. To satisfy these conditions, the areas of RTDs A and B were selected to be 6μm×10μm and 6μm×6μm, respectively, while the HEMT gate width was 40μm, and the gate length was 1μm. In the fabricated circuit, the peak currents of A and B were 2.6 and 1.1mA, respectively. The maximum peak current of the parallel connection of RTD B and the HEMT was 4.8mA, as shown in Figs.3 and 4.

The operation of the proposed logic circuit was tested via on-wafer RF probing. Figure 5 shows the inverter operation of the logic circuit. The traces show V_{in}, V_{clock}, and V_{out} from top to bottom. The RTD is defined as follows: The state in which the voltage between the two terminals of the RTD is lower than the RTD's peak voltage (V_p) is called the "low resistance on" state. In the opposite case, it is called the "high resistance off" state. In the measurement, V_{clock} is from −0.53 to 0V, and V_{in} is from −1.0 to 0V. V_{clock} is chosen so that either A or B switches from the "on" state to the "off" state when V_{clock} = −0.53V. When V_{clock} = 0V, V_{out} is 0V, because the output voltage is the voltage between the terminals of B. Then the circuit is in the monostable state. When V_{clock} = −0.53V, there are two cases. In the first case, when V_{in} = −1V, there is no current between the drain and the source of the HEMT. The HEMT cannot modulate the peak current since the peak current of RTD B is lower than that of RTD A. Thus RTD B is in the "off" state, and V_{out} is in the logic low level, L. In the second case, when V_{in} = 0V, the peak current of RTD B is larger than that of RTD A because of the modulation of the HEMT. Thus RTD B is in the "on" state, and RTD A is in the "off" state, so V_{out} is in the logic high level (approach 0V), H. Then the circuit is bistable.

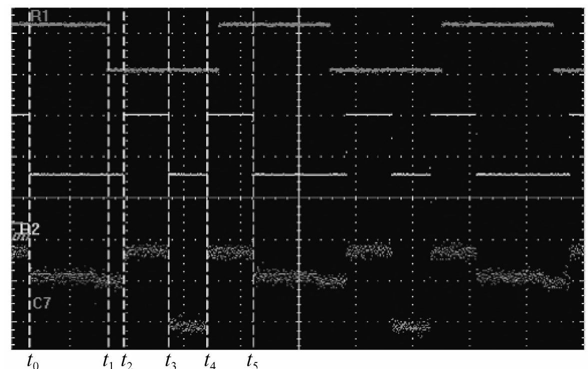

Fig.5 Inverter operation of the logic circuit

As shown in Fig.5, before t_0, V_{in} is 0V and V_{clock} is also 0V, and then V_{out} is H. At t_0, V_{clock} falls from H to L, since V_{in} is H, and thus RTD B is in the "on" state and RTD A is in the "off" state, so V_{out} remains at H. At t_1, V_{in} falls from H

to L, since RTD A is already in the "off" state, and V_{out} remains at H. At t_2, V_{clock} rises to 0V, so V_{out} is 0V (H). At t_3, V_{clock} falls from H to L, since V_{in} is L, and thus RTD B is in the "off" state and RTD A is in the "on" state, so V_{out} falls from H to L. At t_4, V_{clock} rises to 0V and V_{out} rises from L to H. Finally, t_5 is the same as t_0.

The above cases confirm the circuit operation principle proposed in the previous section. Therefore the logic circuit is considered to operate successfully.

The experimental results of the HEMT's gain-frequency character are shown in Fig. 6. The HEMT's gate length is 1μm, and the gate width is 40μm. We get the critical frequency (f_T) of 3.7GHz.

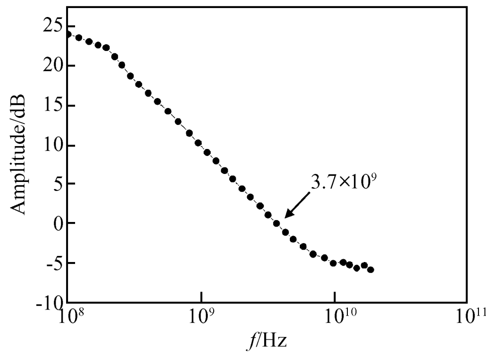

Fig. 6　Experimental results of HEMT's gain-frequency characteristics

The results of the S parameter measurements of the RTD are shown in Fig. 7. We get the RTD resistance using $Z = Z_0 \frac{1 + S_{11}}{1 - S_{11}}$. The change of the resistance's real and imaginary parts when the frequency changes is shown in Figs. 7(a) and (b). We can get the RTD's resistance critical frequency (f_R) of 7.9GHz (when the resistance's real part falls to 0).

We get frequency operations of the circuit up to 2GHz. The output signal of the device at 2GHz operation is shown in Fig. 8. $V_{in} = -1$V, and a 2GHz RF signal is added on V_{clock}. The operation status is good. Thus our logic circuit can successfully operate up to 2GHz.

The operation frequency is limited by the HEMT's gate length, the parasitic capacitance of RTDs and HEMT, and the material of the RTD and the HEMT. In order to get a higher frequency, we can reduce the HEMT's gate length and the measure of the RTD using electron beam lithography, and change the substrate to InP to get a large InAs mole fraction channel and potential well with higher electron mobility. However, this would greatly increase the cost of the circuit.

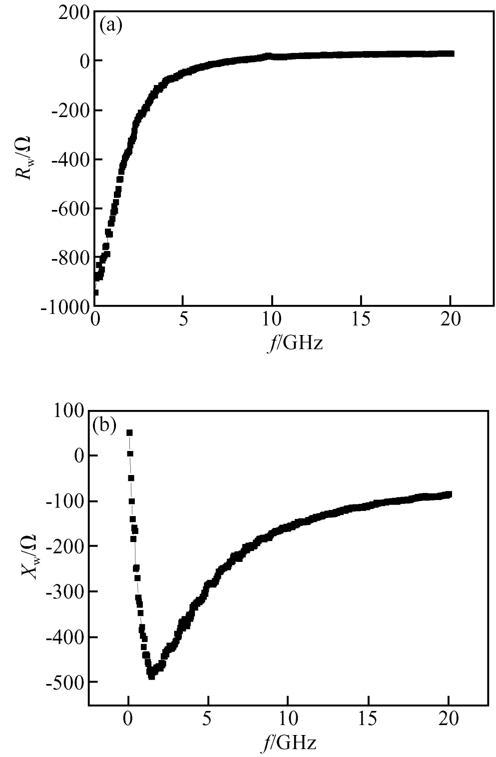

Fig. 7　(a) Real part of the resistance as a function of frequency; (b) Imaginary part of the resistance as a function of frequency

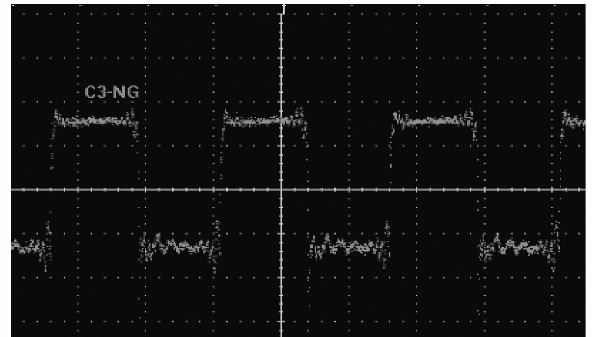

Fig. 8　Output signal at 2GHz operation

4　Conclusions

We have successfully demonstrated a simple technology for the monolithic integration of RTDs and HEMTs. This technology requires a sin-

gle epitaxial growth step and relies on established processing techniques. Using this technology, we have achieved good device performance and have demonstrated room temperature operation of a MOBILE circuit. The logic circuit operates well, and demonstrates frequency operations of up to 2GHz.

The RTD/HEMT circuit technology can reduce device count per circuit function and simplify circuit interconnect topology, enabling large improvements in circuit integration density.

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一种基于 RTD 和 HEMT 的单片集成逻辑电路

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摘要： 介绍了一种基于共振隧穿二极管(RTD)和高电子迁移率晶体管(HEMT)的单片集成电路.采用分子束外延技术在 GaAs 底层上重叠生长了 RTD 和 HEMT 结构. RTD 室温下的峰谷电流比为 5.2∶1，峰值电流密度为 22.5kA/cm^2. HEMT 采用 1μm 栅长，阈值电压为 −1V.设计电路称为单稳态-双稳态转换逻辑单元(MOBILE).实验结果显示了该电路逻辑运行成功，运行频率可达 2GHz 以上.

关键词： 单稳态-双稳态转换逻辑单元；共振隧穿二极管；高电子迁移率晶体管；InGaAs；GaAs
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