Dual Material Gate SOI MOSFET with a Single Halo

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Abstract: In order to suppress drain-induced barrier lowering in dual material gate SOI MOSFETs, halo doping is used in the channel near the source. Two-dimensional analytical models of surface potential and threshold voltage for the novel SOI MOSFET are developed based on the explicit solution of the two-dimensional Poisson’s equation. Its characteristic improvement is investigated. It is concluded that the novel structure exhibits better suppression of drain-induced barrier lowering and higher carrier transport efficiency than conventional dual material gate SOI MOSFETs. Its drain-induced barrier lowering decreases with increasing halo doping concentration but does not change monotonically with halo length. The analytical models agree well with the two-dimensional device simulator MEDICI.

Key words: dual material gate; SOI; threshold voltage; analytical model

1 Introduction

Dual material gate (DMG) SOI MOSFETs seem to be a very promising option for ultimate scaling of CMOS technology due to their excellent short channel effect (SCE) and hot carrier effect (HCE) suppression and high carrier transport efficiency. However, DMG SOI MOSFETs show considerable drain-induced barrier lowering (DIBL) in the sub-100nm regime. Locally raising the channel doping next to the drain or drain/source can improve MOSFET’s performance. In the past few years, the local high doping concentration in the channel near source/drain junctions has been implemented via lateral channel engineering, e.g., halo or pocket implantation. Single-halo MOSFET structures have been introduced for bulk as well as SOI MOSFETs to adjust threshold voltage. Halo implantation devices show excellent output characteristics with low DIBL, higher driving capacity and low leakage currents compared to conventional MOSFETs. However, such an attempt has not been reported for DMG SOI MOSFETs. In this paper, for the first time the structure of a DMG SOI MOSFET with a single halo is investigated. Two-dimensional analytical models of potential and threshold voltage for the fully depleted SOI MOSFET are developed based on the explicit solution of the two-dimensional Poisson’s equation. The characteristics of the novel SOI MOSFET are compared with the conventional DMG SOI MOSFET and the influence of the halo structures is studied. The models are verified with the two-dimensional device simulator MEDICI.

2 Model formulation

2.1 Analytical potential

The schematic structure of the DMG SOI MOSFET with a single halo (DMGH) is shown in Fig. 1. The doping concentration Nₐ near the source region is higher than Nₘ in the rest of the channel. Considering the gate and doping profile, the channel can be divided into three zones.

Neglecting the effect of the fixed oxide charges on the electrostatics of the channel, the Poisson’s equation of the potential distribution in the three silicon film zones before the onset of strong inversion can be written as.
Fig. 1  Schematic structure of DMG with a single halo

\[
\frac{\partial^2 \varphi_j(x, y)}{\partial x^2} + \frac{\partial^2 \varphi_j(x, y)}{\partial y^2} = \frac{qN_j}{\varepsilon_a},
\]

\[L_{j-1} \leq x \leq L_j, 0 \leq y \leq t_a, j = 1, 2, 3 \] (1)

\[
\varphi_j(x, y) = \varphi_{j0}(x) + \frac{\varepsilon_m}{\varepsilon_a} V_{ds} \frac{V_{ds}}{t_f} + \frac{c_a c_b (V_{pb, b} - V_{FB, b}) + c_l (c_a + c_b) (V_{pb, f} - V_{FB, f}) - (c_a c_b + c_l c_b + c_t c_u) \varphi_{j0} y^2}{t_a^2 (c_a c_b + 2c_b^2)}
\]

\[L_{j-1} \leq x \leq L_j, 0 \leq y \leq t_a, j = 1, 2, 3 \] (3)

Here \( c_a = \frac{\varepsilon_a}{t_a} \), \( c_l = \frac{\varepsilon_m}{t_f} \), and \( c_b = \frac{\varepsilon_m}{t_b} \).

Using Eq. (3) in Eq. (1) and the independence of \( x \) and \( y \), Equation (4) can be derived.

\[
\frac{d^2 \varphi_{j0}(x)}{dx^2} - \lambda^2 \varphi_{j0}(x) = \beta_j,
\]

\[L_{j-1} \leq x \leq L_j, j = 1, 2, 3 \] (4)

Here \( \lambda = \sqrt{\frac{2 (c_a c_u + c_l c_u + c_t c_b)}{t_a^2 c_a (2 c_a + c_b)}} \) and \( \beta_j = \frac{qN_j}{\varepsilon_a} - 2(V_{pb, f} + V_{FB, f}) \frac{c_l (c_a + c_b)}{t_a^2 c_a (2 c_a + c_b)} - 2(V_{pb, b} - V_{FB, b}) \frac{c_b}{t_a^2 (2 c_a + c_b)}, \) \( j = 1, 2, 3 \)

where \( V_{pb, f} \) is the front gate-to-source bias voltage, \( V_{FB, f} \) \( j = 1, 2, 3 \) is the front channel flat band voltage of zone \( j \), \( V_{pb, b} \) is the substrate bias voltage, and \( V_{FB, b} \) \( j = 1, 2, 3 \) is the back channel flat band voltage of zone \( j \).

Equation (4) is a second-order differential equation with constant coefficients, and therefore the expression for the surface potential of the front channel is of the form:

\[
\varphi_{j0}(x) = A_j e^{-\beta_j x} + B_j e^{\beta_j x},
\]

\[L_{j-1} \leq x \leq L_j, j = 1, 2, 3 \] (5)

Using the continuity of electric flux and surface potential at the boundaries of the three silicon film zones, the built-in potential drop \( V_b \) across the source-body junction, and the applied drain-source bias \( V_{ds} \), we can obtain the constants \( A_j \) and \( B_j \) \( j = 1, 2, 3 \).

\[
A_j = (V_{bi} + (1 - e^{\lambda^2}) V_{pb, f}) / 2 \sinh(\lambda L) \]

\[
B_j = (V_{bi} + e^{-\lambda^2} - 1) V_{pb, f} / 2 \sinh(\lambda L) \]

\[
A_j = A_{j-1} - e^{\lambda^2 (\beta_j - \beta_{j-1}) / 2 \lambda^2}, \quad j = 2, 3 \]

\[
B_j = B_{j-1} - e^{-\lambda^2 (\beta_j - \beta_{j-1}) / 2 \lambda^2}, \quad j = 2, 3 \] (6)

where

\[
V_{bi} = (V_b + \beta_j / \lambda^2 + V_{pb, f}) e^{\lambda^2} - (V_b + V_{ds} + \beta_j / \lambda^2 + V_{PB, f}) - \sum_{j'=1}^{j-1} \cosh[\lambda (L - L_{j'})] (\beta_{j'} - \beta_{j'-1}) / \lambda^2 \]

\[
V_{bi} = V_b + V_{ds} + \beta_j / \lambda^2 + V_{PB, f} + \sum_{j'=1}^{j-1} \cosh[\lambda (L - L_{j'})] (\beta_{j'} - \beta_{j'-1}) / \lambda^2 - (V_b + \beta_j / \lambda^2 + V_{PB, f}) e^{-\lambda^2} \]

\[
L = L_3 \]

The electric field pattern along the channel determines the electron transport velocity through the channel. The electric field component in the \( x \) direction is given by differentiating \( \varphi_{j0}(x) \) \( j = 1, 2, 3 \) with respect to \( x \):

\[
E(x) = -A_j \lambda e^{-\lambda x} + B_j \lambda e^{\lambda x}, \quad L_{j-1} \leq x \leq L_j, j = 1, 2, 3 \] (7)

2.2  Analytical threshold voltage

When the doping concentration \( N_A \) is greater than \( N_B \), the minimum surface potential \( \varphi_{min} \) lies in zone 1, as shown in Fig. 2. The threshold volt-
age of the channel is determined by $\varphi_{\text{min}}$, which occurs where the differentiation of $\varphi_{\text{ext}}(x)$ is equal to zero and is as follows:

$$\varphi_{\text{min}} = 2\sqrt{\frac{A_1\beta_1}{B_1}} - \beta_1/\lambda^2$$  \hspace{1cm} (8)

The threshold voltage is the value of the gate voltage at which a conducting channel is induced at the surface of an SOI MOSFET. In a fully depleted thin-film SOI MOSFET, it is desirable that the front channel turns on before the back channel. Therefore, the threshold voltage is taken to be the value of $V_{\text{th},t}$ for which $\varphi_{\text{min}} = 2\varphi_{\text{F}}$, where $\varphi_{\text{F}}$ is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. Considering $t_b \gg t_i$ and $t_b \gg t_u$ generally, $V_{\text{th}}$ can be derived from Eq. (8).

$$V_{\text{th}} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma}}{2\sigma}$$ \hspace{1cm} (9)

where

$$\sigma = 2\cosh(\lambda L) - 2 - \sinh^2(\lambda L)$$

$$\eta = V_{\text{bi}}(e^{-\lambda L} - 1) + V_{\text{bi}}(1 - e^{\lambda L}) + 2\sinh^2(\lambda L)(2\varphi_{\text{F}} + U_1)$$

$$\xi = V_{\text{bi}} - \sinh^2(\lambda L)(2\varphi_{\text{F}} + U_1)^2$$

$$V_{\text{bi}} = \left( V_b + U_1 \right) e^{\lambda L} - \left( V_b + V_d + U_1 \right) - \sum_{j=1}^{3} \cosh[\lambda(L - L_j)] \left( U_i - U_{i+1} \right)$$

$$V_{\text{bi}} = V_b + V_d + U_3 + \sum_{j=1}^{3} \cosh[\lambda(L - L_j)] \left( U_i - U_{i+1} \right) - \left( V_b + U_1 \right) e^{\lambda L}$$

$$U_j = \frac{qN_{\text{A}}}{c_i} \left( V_{\text{bi},b} - V_{\text{FB},b} \right) \frac{c_b}{c_i}$$

$$V_{\text{FB},b} = \frac{c_b}{c_i}$$

$$j = 1, 2, 3$$

3 Model verification and discussion

Now we will analyze the performance of a DMGH in terms of DIBL, the threshold voltage roll-off, and carrier transport efficiency, and verify the models by comparing the results with simulations in MEDI CI. Fully depleted SOI nMOSFETs are utilized in the analysis. Unless otherwise noted, the typical values of parameters are as follows.

For DMGH, $W_b = 4.77\text{V}$, $W_d = 4.10\text{V}$, $V_{\text{bi},b} = 0\text{V}$, drain and source doping concentration $N_D = 10^{20}\text{cm}^{-3}$, $N_A = 4 \times 10^{17}\text{cm}^{-3}$, $N_B = 10^{27}\text{cm}^{-3}$, $t_i = 2\text{nm}$, $t_b = 300\text{nm}$, $t_d = 12\text{nm}$, $L_1 = 20\text{nm}$, $L_2 = 50\text{nm}$, $L_3 = 100\text{nm}$, and the work function of the buried gate is equal to $W_1$. For a conventional DMG (DMG with uniform doping profile), $N_A = 10^{17}\text{cm}^{-3}$, and all the other parameters are the same as DMGH.

The surface potential along the front channel is plotted in Fig. 2. It can be seen from the figure that for a DMGH, an extra potential step profile exists near the halo boundary in addition to the one near the interface between the two gates in the DMG.

![Fig. 2 Surface potential (V) vs. Distance from source (nm)](image)

The surface electric field along the front channel is plotted in Fig. 3. It is shown that for a DMGH, there is an additional local electric field peak near the halo boundary and the peak will increase with increasing $N_A$. It can also be found that the other peak will increase when $W_1$ is increased. Because the additional electric field peak is closer to the source, carriers will be accelerated earlier and travel through the channel more quickly in a DMGH than in a DMG. Therefore, the transport efficiency of carriers in a DMGH is enhanced as compared with a DMG, and it will be further improved with the increase of $N_A$ in some scope considering the degradation of mobility with increasing impurity concentration.

![Fig. 3 Surface electric field (V) vs. Distance from source (nm)](image)
Figure 4 shows the threshold voltage roll-off with gate length, where \( V_{th} \) is the threshold voltage of devices with short gate length and \( V_{th0} \) is the \( V_{th} \) value with a gate length of 200 nm. It can be found that the threshold voltage of both structures exhibits inverse SCE, and the difference between them is small.

\[
\Delta V_{th} / \Delta V_{sa} = V_{th} \left( V_{sa} = 0 \right) - V_{th} \left( V_{sa} = 2 \right) \text{ and } \Delta V_{ds} = 2 V.
\]

It is evident from the figure that the DMGH exhibits better suppression of DIBL, which results from the double effects of the asymmetrical halo and dual material gates.

Figure 6 gives the DIBL variation in a DMGH under different halo structures. It is found that DIBL does not change monotonically with halo length and reaches a minimum when the halo length is around 20 nm. The DIBL decreases with increasing halo doping concentration.

![DIBL in DMGH under different halo structures](image)

Fig. 6 DIBL in DMGH under different halo structures

Figures 2 to 6 show that the derived models are in good agreement with MEDICI.

4 Conclusion

A novel structure called a dual material gate SOI MOSFET with a single halo is proposed to improve DIBL and carrier transport efficiency in the sub-100 nm regime. The analytical models of surface potential and threshold voltage of the novel structure in the fully depleted condition are derived, and the characteristics are examined. The novel device shows better performance in suppressing DIBL and enhancing carrier transport efficiency than conventional dual material gate SOI MOSFETs. Its DIBL is reduced when the halo doping concentration is increased but does not change monotonically with halo length. The derived analytical models are in good agreement with the two-dimensional device simulator MEDICI.

References


摘要：为了抑制异质栅 SOI MOSFET 的漏致势垒降低效应，在沟道源端一侧引入了高掺杂 Halo 结构。通过求解二维电势 Poisson 方程，为新结构器件建立了全耗尽条件下表面势和阈值电压解析模型，并对其性能进行了研究。结果表明，新结构器件比传统的异质栅 SOI MOSFETs 能更有效地抑制漏致势垒降低效应，并进一步提高了载流子输运效率。新结构器件的漏致势垒降低效应随着 Halo 区掺杂浓度的增加而减弱。但随着 Halo 区长度非单调变化，解析模型与数值模拟软件 MEDICI 所得结果高度吻合。

关键词：异质栅；SOI；阈值电压；解析模型

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