Dual Material Gate SOI MOSFET with a Single Halo*

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Abstract: In order to suppress drain-induced barrier lowering in dual material gate SOI MOSFETs, halo doping is used in the channel near the source. Two-dimensional analytical models of surface potential and threshold voltage for the novel SOI MOSFET are developed based on the explicit solution of the two-dimensional Poisson's equation. Its characteristic improvement is investigated. It is concluded that the novel structure exhibits better suppression of drain-induced barrier lowering and higher carrier transport efficiency than conventional dual material gate SOI MOSFETs. Its drain-induced barrier lowering decreases with increasing halo doping concentration but does not change monotonically with halo length. The analytical models agree well with the two-dimensional device simulator MEDICI.

Key words: dual material gate; SOI; threshold voltage; analytical model
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1 Introduction

Dual material gate (DMG) SOI MOSFETs[1~3] seem to be a very promising option for ultimate scaling of CMOS technology due to their excellent short channel effect (SCE) and hot carrier effect (HCE) suppression and high carrier transport efficiency[4,5]. However, DMG SOI MOSFETs show considerable drain-induced barrier lowering (DIBL) in the sub-100nm regime. Locally raising the channel doping next to the drain or drain/source can improve MOSFET's performance[6~8]. In the past few years, the local high doping concentration in the channel near source/drain junctions has been implemented via lateral channel engineering, e.g., halo or pocket implantation[9~11]. Single-halo MOSFET structures have been introduced for bulk[12] as well as SOI MOSFETs[13] to adjust threshold voltage. Halo implantation devices show excellent output characteristics with low DIBL, higher driving capacity and low leakage currents compared to conventional MOSFETs. However, such an attempt has not been reported for DMG SOI MOSFETs. In this paper, for the first time the structure of a DMG SOI MOSFET with a single halo is investigated. Two-dimensional analytical models of potential and threshold voltage for the fully depleted SOI MOSFET are developed based on the explicit solution of the two-dimensional Poisson's equation. The characteristics of the novel SOI MOSFET are compared with the conventional DMG SOI MOSFET and the influence of the halo structures is studied. The models are verified with the two-dimensional device simulator MEDICI.

2 Model formulation

2.1 Analytical potential

The schematic structure of the DMG SOI MOSFET with a single halo (DMGH) is shown in Fig. 1. The doping concentration N_A near the source region is higher than N_B in the rest of the channel. Considering the gate and doping profile, the channel can be divided into three zones.

Neglecting the effect of the fixed oxide charges on the electrostatics of the channel, the Poisson's equation of the potential distribution in the three silicon film zones before the onset of strong inversion can be written as[14~16]

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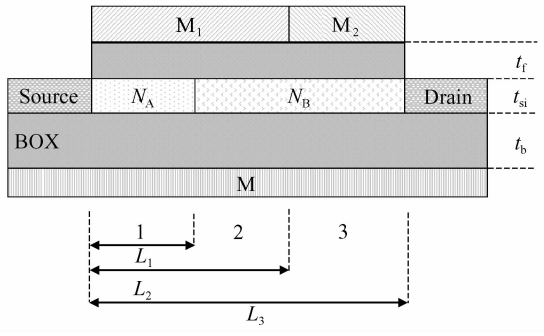

Fig. 1 Schematic structure of DMG with a single halo

$$\frac{\partial^2\varphi_j(x,y)}{\partial x^2}+\frac{\partial^2\varphi_j(x,y)}{\partial y^2}=\frac{qN_j}{\varepsilon_{si}},$$
$$L_{j-1}\leqslant x\leqslant L_j,0\leqslant y\leqslant t_{si},j=1,2,3 \quad (1)$$

where ε_{si} is the dielectric constant of silicon film, $N_1=N_A$, $N_2=N_B$, and $N_3=N_B$.

The potential profile in the vertical direction, i.e., the y-dependence of $\varphi_j(x,y)(j=1,2,3)$, can be approximated by a simple parabolic function for a fully depleted SOI MOSFET as

$$\varphi_j(x,y)=\varphi_{sj}(x)+c_{j1}(x)y+c_{j2}(x)y^2,$$
$$L_{j-1}\leqslant x\leqslant L_j,0\leqslant y\leqslant t_{si},j=1,2,3 \quad (2)$$

where $\varphi_{sj}(x)$ $(j=1,2,3)$ is the front surface potential in zone j and $L_0=0$.

According to Eq. (2) and the continuity of electric flux at the front and buried oxide-silicon interfaces, Equation (3) can be obtained.

$$\varphi_j(x,y)=\varphi_{sj}(x)+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\times\frac{\varphi_{sj}(x)-V_{gs,f}+V_{FB,fj}}{t_f}y+$$
$$\frac{c_{si}c_b(V_{gs,b}-V_{FB,bj})+c_f(c_{si}+c_b)(V_{gs,f}-V_{FB,fj})-(c_{si}c_b+c_fc_b+c_fc_{si})\varphi_{sj}}{t_{si}^2(c_{si}c_b+2c_{si}^2)}y^2,$$
$$L_{j-1}\leqslant x\leqslant L_j,0\leqslant y\leqslant t_{si},j=1,2,3 \quad (3)$$

Here $c_{si}=\frac{\varepsilon_{si}}{t_{si}}$, $c_f=\frac{\varepsilon_{ox}}{t_f}$, and $c_b=\frac{\varepsilon_{ox}}{t_b}$.

Using Eq. (3) in Eq. (1) and considering the independence of x and y, Equation (4) can be derived.

$$\frac{d^2\varphi_{sj}(x)}{dx^2}-\lambda^2\varphi_{sj}(x)=\beta_j,$$
$$L_{j-1}\leqslant x\leqslant L_j,j=1,2,3 \quad (4)$$

Here $\lambda=\left[\frac{2(c_bc_{si}+c_fc_{si}+c_fc_b)}{t_{si}^2c_{si}(2c_{si}+c_b)}\right]^{1/2}$ and

$$\beta_j=\frac{qN_j}{\varepsilon_{si}}-2(V_{gs,f}+V_{FB,fj})\frac{c_f(c_{si}+c_b)}{t_{si}^2c_{si}(2c_{si}+c_b)}-$$
$$2(V_{gs,b}-V_{FB,bj})\frac{c_b}{t_{si}^2(2c_{si}+c_b)},\quad j=1,2,3$$

where $V_{gs,f}$ is the front gate-to-source bias voltage, $V_{FB,fj}$ $(j=1,2,3)$ is the front channel flat band voltage of zone j, $V_{gs,b}$ is the substrate bias voltage, and $V_{FB,bj}$ $(j=1,2,3)$ is the back channel flat band voltage of zone j.

Equation (4) is a second-order differential equation with constant coefficients, and therefore the expression for the surface potential of the front channel is of the form:

$$\varphi_{sj}(x)=A_je^{-\lambda x}+B_je^{\lambda x}-\frac{\beta_j}{\lambda^2},$$
$$L_{j-1}\leqslant x\leqslant L_j,\ j=1,2,3 \quad (5)$$

Using the continuity of electric flux and surface potential at the boundaries of the three silicon film zones, the built-in potential drop V_b across the source-body junction, and the applied drain-source bias V_{ds}, we can obtain the constants A_j and B_j $(j=1,2,3)$.

$$A_1=(V_{b1}+(1-e^{\lambda L})V_{gs,f})/2\sinh(\lambda L)$$
$$B_1=(V_{b2}+(e^{-\lambda L}-1)V_{gs,f})/2\sinh(\lambda L)$$
$$A_j=A_{j-1}-e^{\lambda L_{j-1}}(\beta_{j-1}-\beta_j)/2\lambda^2,\quad j=2,3$$
$$B_j=B_{j-1}-e^{-\lambda L_{j-1}}(\beta_{j-1}-\beta_j)/2\lambda^2,\quad j=2,3 \quad (6)$$

where

$$V_{b1}=(V_b+\beta_1/\lambda^2+V_{gs,f})e^{\lambda L}-(V_b+V_{ds}+\beta_3/\lambda^2+V_{gs,f})-\sum_{j=1}^{2}\cosh[\lambda(L-L_j)](\beta_j-\beta_{j+1})/\lambda^2$$
$$V_{b2}=V_b+V_{ds}+\beta_3/\lambda^2+V_{gs,f}+\sum_{j=1}^{2}\cosh[\lambda(L-L_j)](\beta_j-\beta_{j+1})/\lambda^2-(V_b+\beta_1/\lambda^2+V_{gs,f})e^{-\lambda L}$$
$$L=L_3$$

The electric field pattern along the channel determines the electron transport velocity through the channel. The electric field component in the x direction is given by differentiating $\varphi_{sj}(x)(j=1,2,3)$ with respect to x:

$$E(x)=-A_j\lambda e^{-\lambda x}+B_j\lambda e^{\lambda x},$$
$$L_{j-1}\leqslant x\leqslant L_j,\ j=1,2,3 \quad (7)$$

2.2 Analytical threshold voltage

When the doping concentration N_A is greater than N_B, the minimum surface potential φ_{smin} lies in zone 1, as shown in Fig. 2. The threshold volt-

age of the channel is determined by φ_{smin}, which occurs where the differentiation of $\varphi_{s1}(x)$ is equal to zero and is as follows:

$$\varphi_{smin} = 2\sqrt{A_1 B_1} - \beta_1/\lambda^2 \tag{8}$$

The threshold voltage is the value of the gate voltage at which a conducting channel is induced at the surface of an SOI MOSFET. In a fully depleted thin-film SOI MOSFET, it is desirable that the front channel turns on before the back channel. Therefore, the threshold voltage is taken to be the value of $V_{gs,f}$ for which $\varphi_{smin} = 2\varphi_F$, where φ_F is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. Considering $t_b \gg t_f$ and $t_b \gg t_{si}$ generally, V_{th} can be derived from Eq. (8).

$$V_{th} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma} \tag{9}$$

where

$$\sigma = 2\cosh(\lambda L) - 2 - \sinh^2(\lambda L)$$

$$\eta = V_{b3}(e^{-\lambda L} - 1) + V_{b4}(1 - e^{\lambda L}) + 2\sinh^2(\lambda L)(2\varphi_F + U_1)$$

$$\xi = V_{b3} V_{b4} - \sinh^2(\lambda L)(2\varphi_F + U_1)^2$$

$$V_{b3} = (V_b + U_1)e^{\lambda L} - (V_b + V_{ds} + U_3) - \sum_{j=1}^{2} \cosh[\lambda(L - L_j)](U_j - U_{j+1})$$

$$V_{b4} = V_b + V_{ds} + U_3 + \sum_{j=1}^{2} \cosh[\lambda(L - L_j)](U_j - U_{j+1}) - (V_b + U_1)e^{-\lambda L}$$

$$U_j = \frac{qN_j t_{si}}{c_f} - (V_{gs,b} - V_{FB,bj})\frac{c_b}{c_f} + V_{FB,fj}, \quad j = 1,2,3$$

3　Model verification and discussion

Now we will analyze the performance of a DMGH in terms of DIBL, the threshold voltage roll-off, and carrier transport efficiency, and verify the models by comparing the results with simulations in MEDICI. Fully depleted SOI nMOSFETs are utilized in the analysis. Unless otherwise noted, the typical values of parameters are as follows.

For DMGH, $W_1 = 4.77$V, $W_2 = 4.10$V, $V_{gs,b} = 0$V, drain and source doping concentration $N_D = 10^{20}\,cm^{-3}$, $N_A = 4\times10^{17}\,cm^{-3}$, $N_B = 10^{17}\,cm^{-3}$, $t_f = 2$nm, $t_b = 300$nm, $t_{si} = 12$nm, $L_1 = 20$nm, $L_2 = 50$nm, $L_3 = 100$nm, and the work function of the buried gate is equal to W_1. For a conventional DMG (DMG with uniform doping profile), $N_A = 10^{17}\,cm^{-3}$, and all the other parameters are the same as DMGH.

The surface potential along the front channel is plotted in Fig. 2. It can be seen from the figure that for a DMGH, an extra potential step profile exists near the halo boundary in addition to the one near the interface between the two gates in the DMG.

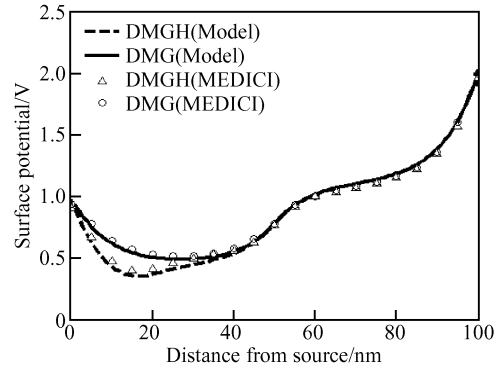

Fig. 2　Surface potential ($V_{ds} = 1$V, $V_{gs,f} = 0.3$V)

The surface electric field along the front channel is plotted in Fig. 3. It is shown that for a DMGH, there is an additional local electric field peak near the halo boundary and the peak will increase with increasing N_A. It can also be found that the other peak will increase when W_1 is increased. Because the additional electric field peak is closer to the source, carriers will be accelerated earlier and travel through the channel more quickly in a DMGH than in a DMG. Therefore the transport efficiency of carriers in a DMGH is enhanced as compared with a DMG, and it will be further improved with the increase of N_A in some scope considering the degradation of mobility with increasing impurity concentration.

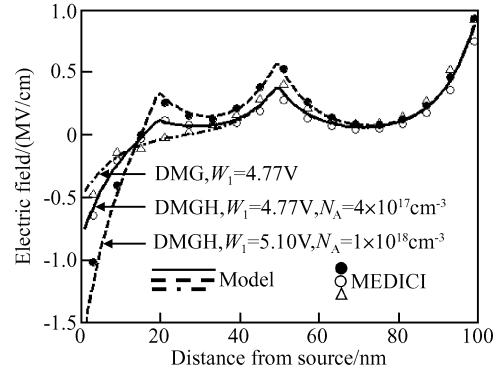

Fig. 3　Surface electric field ($V_{ds} = 1$V, $V_{gs,f} = 0.3$V)

Figure 4 shows the threshold voltage roll-off with gate length, where V_{th} is the threshold voltage of devices with short gate length and V_{th0} is the V_{th} value with a gate length of 200nm. It can be found that the threshold voltage of both structures exhibits inverse SCE, and the difference between them is small.

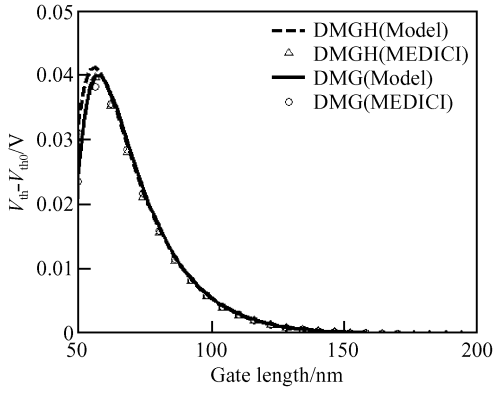

Fig. 4 Threshold voltage roll-off

The DIBL can be expressed by $\Delta V_{th}/\Delta V_{ds}$. Figure 5 shows the DIBL variation in a DMGH and a DMG with gate length, where $\Delta V_{th} = V_{th}|_{V_{ds}=0} - V_{th}|_{V_{ds}=2}$ and $\Delta V_{ds} = 2$V. It is evident from the figure that the DMGH exhibits better suppression of DIBL, which results from the double effects of the asymmetrical halo and dual material gates.

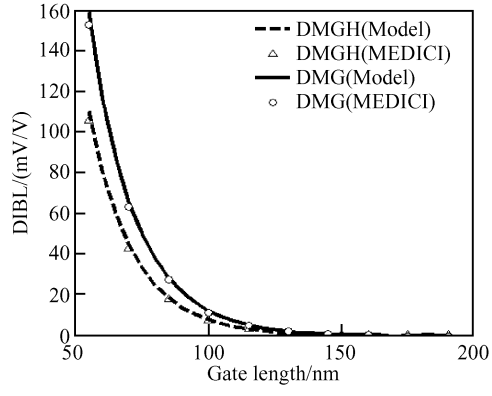

Fig. 5 DIBL in DMGH and DMG ($L_1 : L_2 : L_3 = 1 : 3 : 9$)

Figure 6 gives the DIBL variation in a DMGH under different halo structures. It is found that DIBL does not change monotonically with halo length and reaches a minimum when the halo length is around 20nm. The DIBL decreases with increasing halo doping concentration.

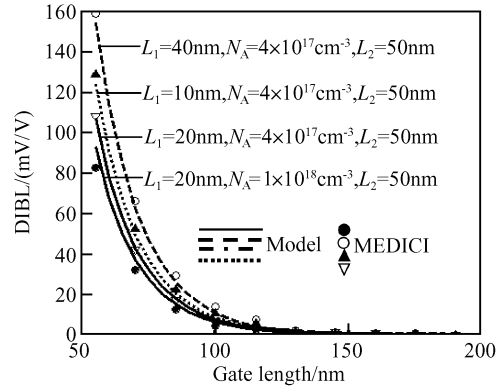

Fig. 6 DIBL in DMGH under different halo structures

Figures 2 to 6 show that the derived models are in good agreement with MEDICI.

4 Conclusion

A novel structure called a dual material gate SOI MOSFET with a single halo is proposed to improve DIBL and carrier transport efficiency in the sub-100nm regime. The analytical models of surface potential and threshold voltage of the novel structure in the fully depleted condition are derived, and the characteristics are examined. The novel device shows better performance in suppressing DIBL and enhancing carrier transport efficiency than conventional dual material gate SOI MOSFETs. Its DIBL is reduced when the halo doping concentration is increased but does not change monotonically with halo length. The derived analytical models are in good agreement with the two-dimensional device simulator MEDICI.

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异质栅非对称 Halo SOI MOSFET*

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摘要：为了抑制异质栅 SOI MOSFET 的漏致势垒降低效应，在沟道源端一侧引入了高掺杂 Halo 结构.通过求解二维电势 Poisson 方程，为新结构器件建立了全耗尽条件下表面势和阈值电压解析模型，并对其性能改进情况进行了研究.结果表明，新结构器件比传统的异质栅 SOI MOSFETs 能更有效地抑制漏致势垒降低效应，并进一步提高载流子输运效率.新结构器件的漏致势垒降低效应随着 Halo 区掺杂浓度的增加而减弱，但随 Halo 区长度非单调变化.解析模型与数值模拟软件 MEDICI 所得结果高度吻合.

关键词：异质栅；SOI；阈值电压；解析模型
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