A Fast Acquisition PLL with Wide Tuning Range*

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Abstract: We present a design for an adaptive gain phase-locked loop (PLL) that features fast acquisition, low jitter, and wide tuning range. A dual-edge-triggered phase frequency detector (PFD) and a self-regulated voltage controlled oscillator (VCO) are employed in this design to realize the aforementioned properties. Measured results show that the experimental chip, implemented in a standard 0.5μm 5V CMOS logic process, has an acquisition time of about 150ns at 37% frequency variation and an output RMS jitter of 39ps at 640MHz.

Key words: PLL; fast acquisition; low jitter; wide tuning range
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1 Introduction

Recently, phase-locked loops (PLL) have played a key role in many integrated circuit fields, such as clock generation in VLSI/SoC (system-on-chip) and frequency synthesizers in communication systems. Fast acquisition, low jitter, and wide tuning range are required in nearly all PLL applications in modern IC systems. According to linear system theory, the bandwidth of a PLL should be broad enough to achieve fast locking. However, a narrow bandwidth is required to reduce output jitter. Thus there is a tight tradeoff between the acquisition time and output jitter when designing a PLL.

Recently, several schemes for adjustable bandwidth PLLs have been proposed to balance the performance requirements of fast acquisition and low jitter, such as dynamic gain adjustment of the VCO[1,2], charge current dynamic adjustment[3], and double loop architecture[4].

In dynamic gain adjustment[1,2], complicated digital circuits and switch capacitors are used to control the gain of the VCO. The acquisition time is quite long because the calibration process resets the control word when the power is turned on or the input frequency changes. In charge current dynamic adjustment[3], the loop filter (LF) is driven by an external charge pulse at the beginning of the frequency transition to accelerate the decay of phase error, and then another charge pulse is generated to reduce frequency error to zero as the phase error goes to zero. In this scheme, an additional charge pump is needed to realize the two-stage current pulse injection. However, it is difficult to determine the right amount of charge injection at the proper time. Moreover, the external circuits of two-stage charge current generation introduce problems of stability and noise. The two-loop architecture[4] adopts both a coarse-tuning loop for fast convergence and a fine-tuning loop for fine adjustment. Nevertheless, in this architecture two PFDs and two charge pumps are used at the cost of circuit complexity, power consumption, and area.

For dealing with these problems, a fast acquisition, low jitter, wide tuning range PLL with adaptive dual-edge-triggered PFD and self-regulated (SR) VCO is presented in this paper. Although the underlying principle of this scheme is similar to that of the two-loop architecture, this PLL features only one PFD and a charge pump that has adaptive gain. The PLL works alternatively under two modes: wide bandwidth mode, when the phase difference is larger than the conversion threshold; and narrow bandwidth mode otherwise. In this scheme, fast acquisition is achieved by the wide bandwidth mode while low jitter is acquired by the narrow mode.

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2 Architecture and realization of the proposed PLL

In this section the architecture and the detailed realization of the fast acquisition PLL with wide tuning range and low jitter are presented. After the overview of the architecture, the design of the dual-edge-triggered PFD is described, and then we introduce the charge pump and LF. Moreover, we present the design of a low noise, wide tuning range SR VCO. Finally, the operation principle of our PLL is also described.

2.1 Overview of fast acquisition PLL architecture

The charge pump phase locked loop (CP-PLL) is widely used in PLL design for its properties of wide pull-in range and zero steady state phase error[5]. In this paper, we propose a fast acquisition CPPLL with wide tuning range and low jitter, which has the scheme shown in Fig. 1. The main components of our PLL are designed deliberately to acquire the desired properties. First, a

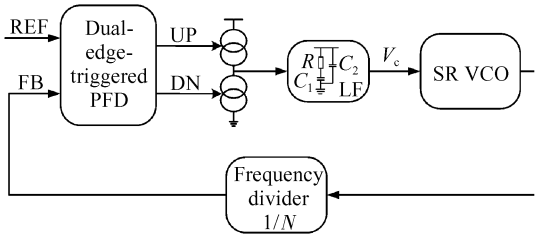

Fig. 1 Diagram of the proposed PLL

dual-edge-triggered PFD is used in the proposed PLL. Unlike the scheme of the two-loop architecture[4], in which two PFDs and charge pumps are used to achieve different tuning processes, the dual-edge-triggered PFD can adjust the PLL acquisition process with only one PFD because of its varied gain at different states of the PLL. When the PLL is in the out-of-lock state, the large gain state of the PFD is activated to accelerate the rate of convergence. On the other hand, the PFD works with small gain to achieve fine adjustment when the PLL is in or near the locked state. Second, a symmetric charge pump is employed to reduce unmatched charge current. Moreover, a second order LF is also combined with dual-edge-triggered PFD to reduce the control line ripple. Finally, an SR differential VCO is adopted to reduce the noise and jitter of the PLL further and achieve a wide tuning range. The detailed circuits and principles of these components are described in the following sections.

2.2 PFD circuit design

A traditional PFD[6] consists of flip-flops and has the disadvantages of a large dead zone and slow speed due to the delay along the reset loop. To overcome these disadvantages, we adopt the adaptive dual-edge-triggered PFD,[7] which consists of dynamic latches and static logic gates, as shown in Fig. 2(a). This kind of PFD features zero dead zone, dual slope gain, and rapid response.

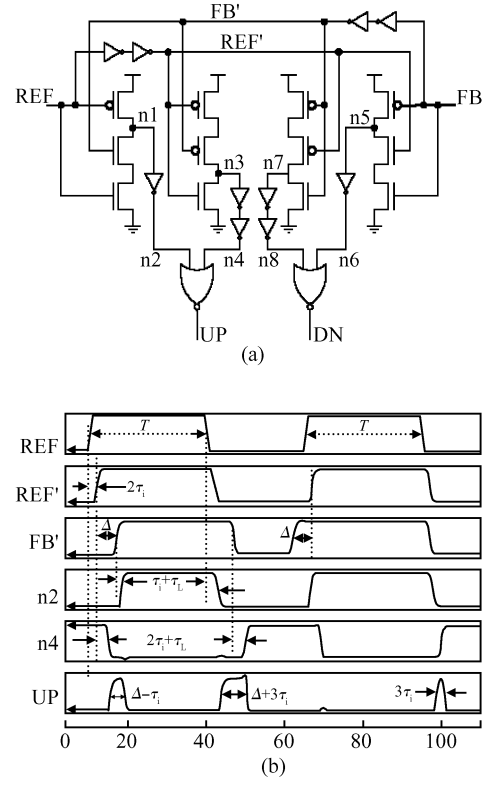

Fig. 2 Schematic (a) and waveforms (b) of dual-edge-triggered PFD

The principle of the PFD is demonstrated by signal UP in the case that the reference signal (REF) precedes the feedback signal (FB) by about Δ as shown in Fig. 2(b). Within one cycle, the signal UP has two pulses. One is trigged by the positive edge of REF and the other by negative edge. We assume that all inverters share the same delay of τ_i and that the delay of N-latch and P-latch is identical to τ_L in the PFD. According to

the schematic and the waveforms, it is easy to derive the pulse width of T_{UP-p}, which is at the rising edge of REF, and T_{UP-n}, which is at the falling edge, as

$$T_{UP-p} = (\Delta + \tau_i + \tau_L) - (2\tau_i + \tau_L) = \Delta - \tau_i \quad (1)$$

$$T_{UP-n} = (\Delta + 2\tau_i + 2\tau_i + \tau_L) - (\tau_i + \tau_L) = \Delta + 3\tau_i \quad (2)$$

Following an analysis similar to that of signal UP, the pulse width of signal DN is given as follows in the case in which REF precedes FB:

$$T_{DN-n} = 3\tau_i \quad (3)$$

Accordingly, the effective pulse that drives the charge pump has the width of

$$T_{eff} = T_{UP-p} + T_{UP-n} - T_{DN-n} = 2\Delta - \tau_i$$

When the input difference is smaller than τ_i, from Eq. (1), we can derive $T_{UP-p} < 0$. This means that the width of the pulse located at the positive edge of REF, T_{UP-p}, fades and vanishes finally when Δ diminishes while the loop state changes from out-of-lock to near or in lock. Then the effective pulse has a width of $T_{eff} = \Delta$, which is just the difference between the two input signals. The results are similar when FB precedes REF, so the detailed analysis is omitted because of space limitation.

Therefore, in the case that the phase difference Δ is larger than τ_i, the PFD works as a large slope detector. It is easy to derive that the gain of the PFD is as almost twice that when the phase difference is less than τ_i. Figure 3 shows the simulation result of the relation between the gain of the PFD and the difference between REF and FB.

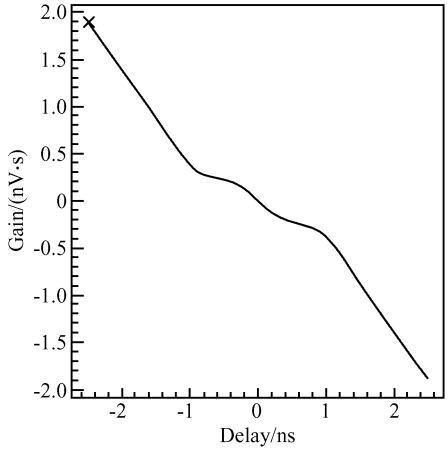

Fig. 3　Gain of the dual-edge-triggered PFD

According to the waveforms and operation principle of the PFD, we can derive that a narrow pulse with width of $3\tau_i$ is located at UP and DN when the phase difference Δ is zero. These narrow pulses are used to erase the dead zone of the PFD[8].

Note that other kinds of delay cells can be used to substitute to inverters from n1 to n2 and from n3 to n4 to adjust the pulse width of UP and DN. Their delay time determines the conversion threshold on which PFD depends to switch between large and small gain modes. If the conversion threshold is too small, the power consumption and fluctuation on the VCO control line cannot be improved effectively. On the other hand, the acquisition time becomes too long to be tolerant if the conversion threshold is too large. In this design we assign the conversion threshold as $\Delta D \times T + t_{p-p}$, where ΔD is the duty cycle difference between REF and FB, T is the period of REF, and t_{p-p} is the estimated peak-to-peak jitter of FB.

2.3　Charge pump and LF design

According to the previous section, the PFD delivers output in the form of three-state digital logic. A charge pump and LF are utilized in the PLL to convert the timed logic levels into analog quantities as voltage V_c for controlling the oscillator. V_c remains stable, resulting in a stable VCO output frequency under the locked condition. In practice, V_c fluctuates even if REF and FB are in phase. This fluctuation, known as control line ripple, which is caused by frequency leakage of input signals and mismatch of charge pump, must be kept as small as possible because it is the key source of the output sidebands and jitters. Decreasing the filter cutoff frequency is an easy method to reduce the ripple on V_c, but at the cost of a narrower loop bandwidth and therefore a long acquisition time. A symmetric loads charge pump[9] is employed in our design to reduce the unmatched charge current induced by defective effects such as charge injection. In addition, a second order LF is adopted with dual-edge-triggered PFD to filter the high frequency components in the VCO control signal and suppress the ripple effectively.

According to the z-plane characteristic equation of a third order PLL with a passive second order LF, the criterion for stability[5], the condic-

tion that all poles are inside the unit circle is satisfied if:

$$K\tau < \frac{4(1+a)}{\frac{2\pi(b-1)}{b\omega_i\tau}\left[\frac{2\pi(1+a)}{b\omega_i\tau}+\frac{2(1-a)(b-1)}{b}\right]} \tag{4}$$

where $b = 1 + C_1/C_2$, $\tau = RC_1$, ω_i is the input frequency, $a = \exp[-2\pi b/\omega_i\tau]$, K is the loop gain, and R, C_1 and C_2 are the resistor and capacitors of LF, respectively. Thus the charge current should satisfy the following limitation:

$$I_{ch} < \frac{4(1+a)N}{K_{VCO}R\,\frac{(b-1)}{b\omega_i}\times\left[\frac{2\pi(1+a)}{b\omega_i\tau}+\frac{2(1-a)(b-1)}{b}\right]} \tag{5}$$

Here K_{VCO} is the gain of VCO, I_{ch} is the charge current of charge pump, and N is the division ratio of the frequency divider (FD). In addition to meeting the specification of settling time as defined in Ref. [10], according to the equation:

$$t_{settling} \approx (\xi\omega_n)^{-1} = 4\pi N/RI_{ch}K_{VCO} \tag{6}$$

the charge current of the loop should satisfy the following equation:

$$I_{ch} > 4\pi N/RK_{VCO}\,t_{settling} \tag{7}$$

2.4 VCO circuit design

The VCO generates the output signal with a frequency f_{VCO} in proportional to the control voltage V_c. K_{VCO} is known as the VCO gain and is defined as

$$K_{VCO} = \frac{f_{max}-f_{min}}{V_{cmax}-V_{cmin}} \tag{8}$$

As mentioned in the section 2.3, the problem of ripple on the VCO control line becomes more serious when the supply voltage is scaled down or the operation frequency increases. The relative magnitude of the primary sidebands at the output of VCO is given by $A_m K_{VCO}/2\omega_{ref}$, where A_m is the peak amplitude of the first harmonic of the ripple, and ω_{ref} is the reference frequency. Then if K_{VCO} and ω_{ref} are fixed by design specification, the ripple is limited to guarantee spectral density of the sidebands.

Moreover, a wide tuning range is an important feature of the VCO to expand the operation range of the PLL. Transmission gates have recently been adopted as voltage control resistance to explore the tuning range of VCOs[11,12]. We consider a transmission gate designed to act as a voltage controlled switch. When the gate voltage biases the transmission gate into the conduction region, the switch is closed and the resistance of the transmission gate is very small. When both MOS transistors are cut off and the switch performs like an open circuit, we can consider the transmission gate resistance infinite. A wide resistance range, which is controlled by gate voltage, is speculated from the above discussion.

A differential SR VCO[11] equipped with transmission gates is involved in our design in order to not only decrease the common mode noise but also increase the immunity of supply noise to overcome the disadvantage of poor noise performance of a ring oscillator. The SR delay cell (Fig. 4) is equipped with a circuit that can adjust cell delay induced by noise fluctuation via the transmission gate and a built-in compensation function to make the cell delay insensitive to the fluctuation, thereby regulating the noise. Suppression of supply noise is illustrated as compensation of noise fluctuation in the following analysis. Assume that V_{OP-} is rising and V_{ON+} is falling at the initial time. For example, a small decrease at the V_{DD} node causes the node of V_{OP-} to charge to V_{DD} more slowly. MP1 monitors this situation by accelerating the speed of discharge at the node of V_{OP+}, and thus speeds the charging of V_{ON-}. Therefore the supply variation can be compensated. This circuit design has good noise rejection performance for device noise such as supply voltage variation. In addition, the absence of tail cur-

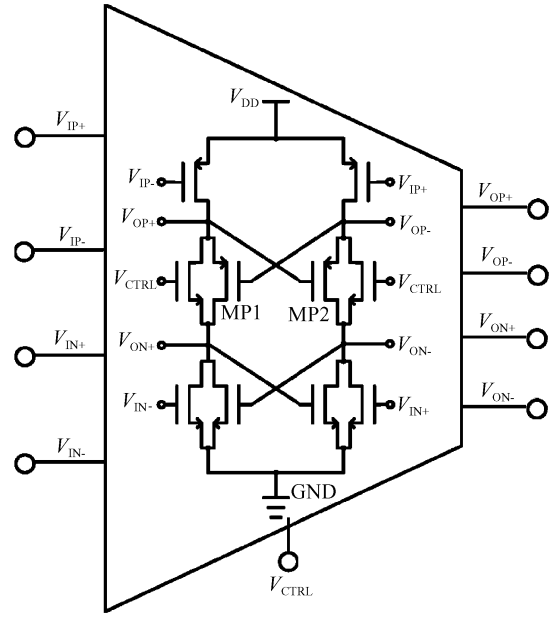

Fig. 4 Self-regulated VCO delay cell

rent and voltage-to-current converter also benefits the SR VCO for low noise performance.

2.5 Operation principles of the proposed PLL

Generally, the open loop transfer function of a PLL can be expressed as

$$\mathrm{GH}(s) = \frac{I_{\mathrm{ch}} K_{\mathrm{VCO}} R C_1}{2\pi N (C_1 + C_2)} \times \frac{s + \dfrac{1}{RC_1}}{s^3 \dfrac{RC_1 C_2}{C_1 + C_2} + s_2} \tag{9}$$

which has a crossover frequency of

$$\omega_{\mathrm{c}} = \frac{I_{\mathrm{ch}} K_{\mathrm{VCO}}}{2\pi N} \times \frac{RC_1}{C_1 + C_2} \tag{10}$$

From section 2.2, there are two cases in the behavior of the proposed PLL.

Case 1: When the PFD works under large gain, that is, $\Delta > \tau_{\mathrm{i}}$, the effective charge current I_{ch} is given as follows:

$$I_{\mathrm{ch}}(1) = \frac{I_{\mathrm{cp}}}{2\pi}(2\Delta - \tau_{\mathrm{i}})\omega_{\mathrm{i}} \approx \frac{I_{\mathrm{cp}}}{\pi}\omega_{\mathrm{i}}\Delta|_{\Delta \gg \tau_{\mathrm{i}}}$$

Case 2: When the PFD works under small gain, that is, $0 < \Delta < \tau_{\mathrm{i}}$, the current is

$$I_{\mathrm{ch}}(2) = \frac{I_{\mathrm{cp}}}{2\pi}\Delta\omega_{\mathrm{i}} \approx \frac{I_{\mathrm{ch}}(1)}{2}\ |_{\Delta \gg \tau_{\mathrm{i}}}$$

where ω_{i} is the REF frequency, and I_{cp} is the average current of the charge pump. According to Eq. (10), bandwidth is proportional to the value of charge current when other parameters are fixed. If the phase difference Δ is larger than τ_{i} (case 1), the PLL is in the out-of-lock state. The loop bandwidth is increased because of large charge current. The settling time is decreased so that the phase difference tends to τ_{i} rapidly. On the other hand, as the PLL moves toward locking state (case 2), the phase difference Δ is less than τ_{i}, the loop bandwidth decreases with small charge current, and thus the acquisition speed is gradually reduced until it reaches the optimized value. Once the steady state is reached, the PLL maintains narrow bandwidth operation to achieve low jitter performance.

3 Experiment setup and test results

3.1 Experiment setup

To test the proposed PLL, an experimental chip was designed based on the 0.5μm 1P3M CMOS logic process with 5V supply voltage. Following the process in Ref. [6] and considering the analysis in section 2, the parameters of charge current, gain of the VCO, resistor and capacitors in the LF are designed.

In our scheme, the gain of the VCO is about 136MHz/V, as required by design specification. Thus, when the input reference frequency is 12.5MHz, according to the formulation of relative magnitude of primary sidebands, $A_{\mathrm{m}} K_{\mathrm{VCO}}/2\omega_{\mathrm{ref}}$, the fundamental ripple amplitude must be less than 0.6mV to guarantee the sidebands are 60dB below the carrier. A second order passive LF is adopted in our design, where C_1 determines the settling time, whereas C_2 decreases the ripple in the control voltage. Usually C_2 is about 1/10 of C_1 so as not to affect the frequency response of the PLL. The maximum value of charge current is defined according to ripple specification as

$$I_{\mathrm{ch}} < \frac{A_{\mathrm{m}}}{L(s)} \tag{11}$$

where $L(s)$ is the equivalent resistance of LF. A lower charge current is chosen considering the system stability (Eq. (5)) and ripple suppression (Eq. (11)). According to settling time (Eq. (7)), the minimum value is $4\pi N/RK_{\mathrm{VCO}} t_{\mathrm{settling}}$. Note that the charge current of a large slope state is about twice of that of a small slope state. Finally, a 40μA charge current is chosen in our design.

3.2 Measurements

The chip is measured by the Agilent 93k SoC test system and HP 54121T digitizing oscilloscope. Figure 5(a) shows a photo of the experimental die. Because of the bandwidth limitation of the measurement instruments, we can only measure a signal less than 400MHz directly. We denote the output signal of divided by two as F2 and the signal of divided by 32 as F32 and use the data of these two signals to deduce the properties of the original output signal, Fo. Figure 5(b) is the output waveform of F2 at 320MHz.

The measured results show that the PLL can work well from 96 to 640MHz. The measured lock time of the proposed PLL, as illustrated in Fig. 6, is about 150ns when the input frequency changes from 6.25 to 12.5MHz, corresponding to Fo from 200 to 400MHz, which is about 37% of the whole tuning range. At the beginning of the locked curve, the fluctuation is a bit large, and after a while it settles.

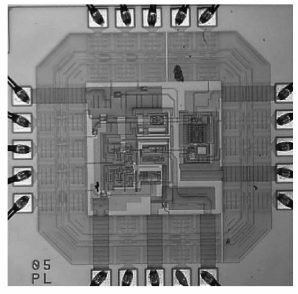

Fig. 5 (a) Die photo; (b) Output wave of 320MHz

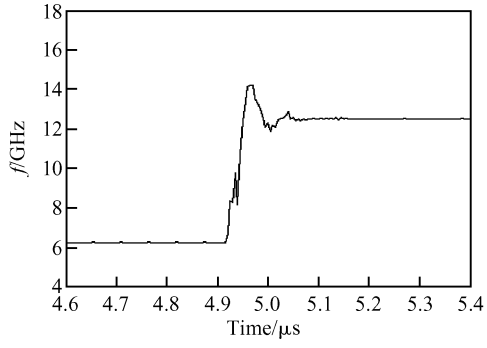

Fig. 6 Acquisition process while input frequency changes from 6.25 to 12.5MHz

The jitter was measured by TIA (DTS1000) embedded in the 93k test system. The measured RMS jitter of F2 is 47ps at 320MHz and 70ps at 20MHz of F32. Because cascaded dividers are adopted in the design and we assume the noise of PLL is independent of that of each divider, we can derive that the jitter after m frequency dividers has the form of

$$\sigma_{T_{FN}}^2 = \sigma_0^2 + \sum_m \sigma_{dn}^2 \tag{12}$$

where $\sigma_{T_{FN}}$ and σ_0 are the RMS jitters of the mth divider output signal and Fo respectively, and σ_{dn} is the jitter caused by the mth divider. According to Eq. (12), the RMS jitter of Fo is calculated to be about 39ps at 640MHz. Figure 7 shows that the measured peak-to-peak jitter of F32 is about 280ps at 12.5MHz, and Figure 8 shows the spectral density in which the amplitude of the sidebands is about 100dB below the carrier.

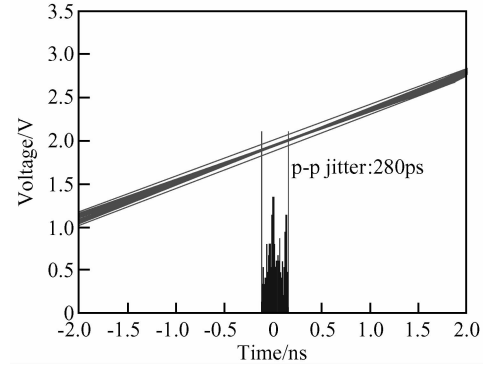

Fig. 7 Jitter of the proposed PLL at 12.5MHz

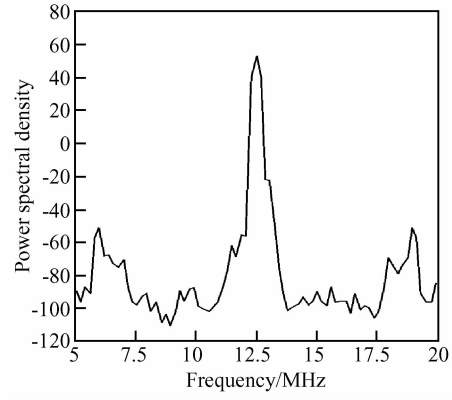

Fig. 8 Spectral density of F32 at 12.5MHz

The measured power consumption of the core circuits is about 50mW, and the die area is about 0.72mm^2. A performance summary of this work is listed in Table 1.

Table 1 Performance summary

Parameter	JSSC2006[13]	This work
Process	0.5μm CMOS	0.5μm 1p3M CMOS
Power supply/V	—	5
Area/mm^2	1.96	0.72
Operating frequency /MHz	80～350	96～640
RMS jitter/ps	16 at 320MHz	39 at 640MHz
Acquisition time/ns	240 at 7% acquisition range	150 at 37% acquisition range
Power consumption /mW	300	50(excluding I/O)

4 Conclusion

This paper presents a design of a PLL with fast acquisition, low jitter, and wide tuning range

through a dual-edge-triggered PFD and an SR VCO. The dual-edge-triggered PFD adaptively changes the bandwidth of the PLL according to the phase difference of the input signals, and therefore balances the settle time and the noise performance well. The SR VCO contributes good noise immunity with a wide tuning range. The die is fabricated in standard 0.5μm 1P3M 5V CMOS logic technology and operates from 96 to 640MHz with core power consumption of about 50mW. The measured results show that acquisition time is about 150ns when the frequency variation is about 37%. The output RMS jitter is 39ps at 640MHz.

References

[1] Wilson W B, Moon U K, Lakshmikumar K R. A CMOS self-calibrating frequency synthesizer. IEEE J Solid-State Circuits, 2000, 35(10): 1437

[2] Yang R J, Liu S I. A 200-Mbps～2-Gbps continuous rate clock and data recovery circuit. IEEE Trans Circuits Syst II: Regular Papers, 2006, 53(4): 842

[3] Hakkinen J, Kostamovaara J. Speeding up and integer-N PLL by controlling the loop filter charge. IEEE Trans Circuits Syst II: Analog and Digital Processing, 2003, 50(7): 343

[4] Tang Y, Ismail M. A new fast-settling gearshift adaptive PLL to extend loop bandwidth enhancement in frequency synthesizers. IEEE Symposium on Circuit and Systems, 2002: 787

[5] Gardner F M. Charge-pump phase-lock loops. IEEE Trans Commun, 1980, 28(11): 1849

[6] Best R E. Phase-locked loops design, simulation and application. 5th ed. McGraw-Hill Press, 2003

[7] Ge Yan, Ji Lijiu. A fast locking charge pump PLL with adaptive bandwidth. International Conference on ASIC Proceedings, 2005: 431

[8] Ahola R, Routama J, Lindfors S, et al. A phase detector with no dead zone and a very wide output voltage range charge pump. IEEE Proc CICC, 1998, 156

[9] Maneatis J G. Low-jitter process-independent DLL and PLL based on self-biased techniques. IEEE J Solid-State Circuits, 1996, 31(11): 1723

[10] Lee T C, Razavi B. A stabilization technique for phase-locked frequency synthesizers. IEEE J Solid-State Circuits, 2003, 38(6): 888

[11] In-Chul H, Kim C, Kang S M. A CMOS self-regulating VCO with low supply sensitivity. IEEE J Solid-State Circuits, 2004, 39(3): 421

[12] Sheu M L, Lin T W, Hsu W H. Wide frequency range voltage controlled ring oscillators based on transmission gates. IEEE ISCAS, 2005: 2731

[13] Zhang R, Rue G S L. Fast acquisition clock and data recovery circuit with low jitter. IEEE J Solid-State Circuits, 2006, 41(5): 1016

一种快捕获宽调节范围的锁相环*

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摘要： 提出了一种快捕获，低抖动，宽调节范围的增益自适应锁相环的设计. 在这个方案中，采用了双边触发的鉴频鉴相器(dual-edge-triggered phase frequency detector)和自调节压控振荡器(self-regulated voltage controlled oscillator)并进行了详细的分析. 芯片的加工工艺是 0.5μm 1P3M CMOS 标准数字逻辑工艺. 测试结果表明输入频率变化在捕获范围的 37%时，捕获时间为 150ns；输出频率为 640MHz 时，均方根抖动为 39ps.

关键词： 锁相环；快捕获；低抖动；宽调节范围

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