Single-Stage Wide-Range CMOS VGA with Temperature Compensation and Linear-in-dB Gain Control

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Abstract: A novel wide-range CMOS variable gain amplifier (VGA) topology is presented. The proposed VGA is composed of a variable transconductor and a novel variable output resistor and can offer a high gain variation range of 80dB while using a single variable-gain stage. Temperature-compensation and decibel-linear gain characteristic are achieved by using a control circuit that provides a gain error lower than ±1.5dB over the full temperature and gain ranges. Realized in 0.25μm CMOS technology, a prototype of the proposed VGA provides a total gain range of 64.5dB with 55.6dB-linear range, a P_{-1dB} varying from −17.5 to 11.5dBm, and a 3dB-bandwith varying from 65 to 860MHz while dissipating 16.5mW from a 2.5V supply voltage.

Key words: linear-in-dB; temperature compensation; variable-gain amplifier; automatic gain control
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1 Introduction

The variable gain amplifier (VGA) is an indispensable block at the front end of many communication systems for maximizing the dynamic range of the receivers, and it is also used in other applications such as medical equipment, hearing aids, and disk drives[1~4]. To buffer receiver electronics from changes in input signal strength by producing a known output voltage magnitude, a VGA is typically employed in a feedback loop to realize an automatic gain control (AGC) circuit. The linear-in-dB gain control characteristic for a VGA is usually required to achieve a constant settling time for the AGC loop[5]. There are two options to achieve variable gain, depending on whether the control signal is digital or analog. Digitally controlled VGAs or programmable gain amplifiers (PGA) use a series of switchable resistors or switched capacitors to control gain. In PGAs, the gain varies as a discrete function of the control signal, which can lead to discontinuous signal phases that can cause problems in many systems. In order to reduce the step of jumps, a large number of control bits are required with digitally-controlled VGAs. Therefore, for applications that require smooth gain transition, VGAs controlled by analog signal are preferred, and they need only one gain-control signal line.

Wide gain control range is one of the most important specifications for VGAs. For example, a gain dynamic range of at least 80dB is required for CDMA systems. There are practical limitations in realizing a wide dynamic range from a single variable-gain stage because of device nonlinearity and parasitics associated with a large excursion of the operating point. A typical gain control range is less than about 30dB in a single-stage system[1~4,6,7]. A gain dynamic range of 50dB was realized in a Gilbert-type variable transconductor in Ref. [8], but the relationship between the gain and the control signal is linear-in-magnitude instead of linear-in-dB, which is another requirement for VGAs for use in AGC loops. In order to cover a wide dynamic gain range, existing VGAs use multiple stages of amplification or attenuation[1,3,6,7]. Multiple stages require a greater supply current, and the noise and linearity degrade at the output of each stage as more stages are cascaded. Additionally, a multiple-stage amplifier introduces another problem: DC-offset cancellation. Single-stage VGAs with more than 70dB gain dynamic range were proposed in Refs. [9] and [10], but they are all implemented in BiCMOS, which is not cost-effective.

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In this paper, a CMOS variable gain amplifier with a wide gain control range realized in a single stage that uses a variable transconductor and a novel variable output resistor simultaneously is proposed. Theoretically, the gain dynamic range of the proposed VGA is improved by a factor of two compared to a conventional one, which is composed of only a variable transconductor. Furthermore, temperature compensation and linear-in-dB gain control characteristics corresponding to the control voltage are achieved by using a control circuit accomplishing voltage-to-current conversion.

2 Limitation on gain range of conventional VGA topologies

A Gilbert-type four-quadrant multiplier can be used as a variable transconductor since its output is equal to the product of the two inputs[4,8,11], as depicted in Fig. 1(a). The analytic transconductance of the multiplier is[8,11]

$$G_m=(g_{m1,2}-g_{m3,4})=\sqrt{2K_N(W/L)}(\sqrt{I_{C1}}-\sqrt{I_{C2}}) \tag{1}$$

where I_{C1} and I_{C2} are the tail currents of two parallel differential pairs, respectively, and $K_N=\mu_n C_{ox}$. In a typical implementation, the sum of the two tail currents is a constant current I_{SS}. The gain dynamic range in dB without change in polarity of the voltage gain is given as[11]

$$\mathrm{GDR(dB)} \approx 20\lg\frac{\sqrt{I_{SS}}}{\sqrt{\frac{I_{SS}}{2}}-\sqrt{\frac{I_{SS}}{2}-I_\Delta}}=20\lg\frac{1}{\sqrt{\frac{1}{2}}-\sqrt{\frac{1}{2}-\frac{I_\Delta}{I_{SS}}}} \tag{2}$$

where I_Δ is the difference between I_{C1} and I_{C2} at the minimum gain setting. Consequently, the gain control range achieved from the variable transconductance is limited by the mismatch between the two differential pairs. For example, the equivalent mismatch factor I_Δ/I_{SS} is about 2% and 1.5% for the VGAs proposed in Refs. [8] and [11], which in turn lead to about 40 and 50dB gain variation ranges, respectively. Another drawback of the VGA depicted in Fig. 1(a) is that an exponential voltage/current generator must be adopted to achieve linear-in-dB gain control[4,8], which is not an easy job, especially while implemented in CMOS technology, since there are no intrinsic exponential-law devices.

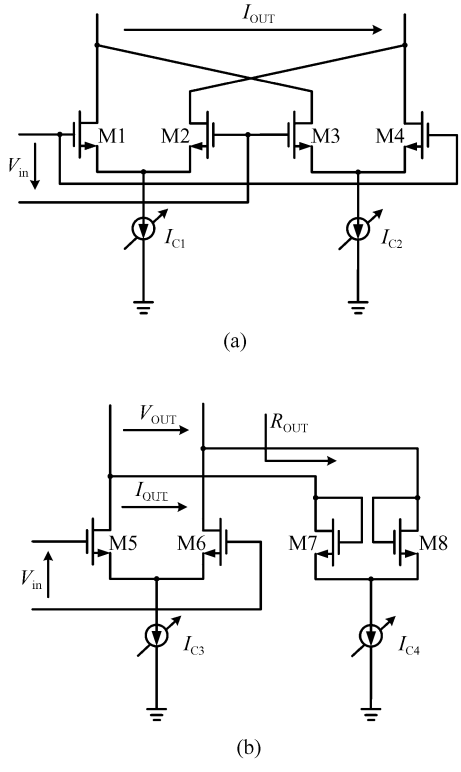

Fig. 1　Conventional VGA topologies using variable transconductor and/or variable resistor

Figure 1(b) shows another VGA topology, which is composed of a differential pair (M5 and M6) that serves as a variable transconductor, and diode connected loads (M7 and M8) that serve as a variable resistor[1,2,12]. Considering that all transistors in Fig. 1(b) are in the saturation region, the voltage gain can be expressed as[2]

$$\mathrm{gain}=\frac{g_{m5,6}}{g_{m7,8}}=\sqrt{\frac{K_N(W/L)_{5,6}I_{C3}}{K_N(W/L)_{7,8}I_{C4}}}=\beta\sqrt{\frac{I_{C3}}{I_{C4}}} \tag{3}$$

where β is a constant related to sizes of transistors M5～M8, and I_{C3} and I_{C4} are the tail currents as shown in Fig. 1(b). By means of the rational expression proposed by Harjani[1], a linear-in-dB gain control characteristic was realized. However, due to the square root function in Eq. (3), half the effective dB-linear variation range provided by I_{C3}/I_{C4} was lost, resulting in only a 15dB-linear variation range, as described in Refs. [1] and [2]. A second-order rational expression was adopted which can provide a linear range of about 60dB[12]; however, the gain variation achieved

from a single variable-gain stage implemented with Fig. 1(b) was reduced by 1/2.

3 Circuit implementation

3.1 Amplifier block

Here we present a compact VGA topology to realize wide-range gain control. The gain variation is doubled compared to the Gilbert-type VGA [in Fig. 1(a)], and the linear-in-dB range is not halved due to the square-root of the current ratio. Detailed discussion of the circuit implementation is given below.

Figure 2 shows the circuit of the amplifying block of the proposed VGA, including the common-mode feedback circuit. The amplifier consists of a variable transconductor implemented with a modified Gilbert-cell (M1～M4) and a novel variable output resistor (M5～M8). The variable resistor is composed of a pair of diode-connected devices (M7, M8) and a pair of cross-coupled devices (M5, M6), which are responsible for implementing a positive resistor and a negative resistor separately. Four tail currents are used to control the magnitude of the transconductance and the resistance as shown in Fig. 2, where $I_{C1} + I_{C2} \approx I_{SS}$. Assuming that M1～M8 are of the same size, the voltage gain can be derived as

$$A_v = G_m R_o = (g_{m1,2} - g_{m3,4})[(-2/g_{m5,6}) \parallel (2/g_{m7,8})] = 2 \times \frac{g_{m1,2} - g_{m3,4}}{g_{m7,8} - g_{m5,6}} = 2 \times \frac{\sqrt{I_{SS}} - \sqrt{I_{C1}}}{\sqrt{I_{SS}} - \sqrt{I_{C2}}} \quad (4)$$

Therefore, the maximum voltage gain occurs when the current I_{C1} approaches zero and the current I_{C2} approach I_{SS}, while the minimum gain occurs when I_{C1} approaches I_{SS} and I_{C2} approaches zero. In order to avoid the phase inversion problem and ensure stability, the maximum of the currents I_{C1} and I_{C2} is chosen by design to be

$$\max(I_{C1}, I_{C2}) = I_{SS} - I_{\Delta} \quad (5)$$

where I_{Δ} is the mismatch current between I_{C1} or I_{C2} and I_{SS} at the gain limits. From Eqs. (4) and (5), the gain dynamic range provided by Fig. 2 can be expressed as

$$\mathrm{GDR(dB)} \approx 20\lg\left(\frac{\sqrt{I_{SS}}}{\sqrt{I_{SS}} - \sqrt{I_{SS} - I_{\Delta}}}\right)^2 = 40\lg\frac{1}{1 - \sqrt{1 - \frac{I_{\Delta}}{I_{SS}}}} \quad (6)$$

Compared to the VGA as shown in Fig. 1(a), the dynamic range of the proposed VGA is doubled. For example, about 80dB is provided from Eq. (6), while only 37dB is provided from Eq. (2) for the same mismatch factor I_{Δ}/I_{SS} of 2%. Cascode transistors (M9～M12) are used to improve the frequency response, as shown in Fig. 2, and their gate voltage VGC is designed as functions of the gain to improve the linearity[7,11].

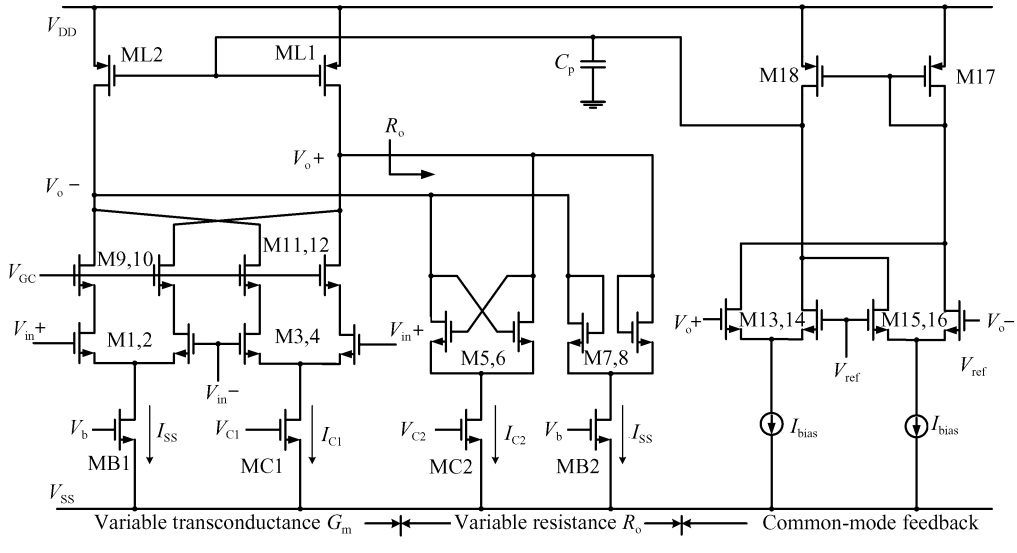

Fig. 2 Circuit schematic of the amplifying stage

3.2 Control circuit block

Considering $I_{C1} + I_{C2} \approx I_{SS}$, the voltage gain of the proposed VGA shown in Fig. 2 can be rearranged from Eq. (4) as

$$A_v \approx 2 \times \frac{\sqrt{I_{SS}} - \sqrt{I_{SS} - I_{C2}}}{\sqrt{I_{SS}} - \sqrt{I_{C2}}} = 2 \times \frac{1 - \sqrt{1 - I_{C2}/I_{SS}}}{1 - \sqrt{I_{C2}/I_{SS}}}, \quad 0 \leqslant \frac{I_{C2}}{I_{SS}} < 1 \qquad (7)$$

Substituting $x = \frac{1}{2} - \frac{I_{C2}}{I_{SS}}$ into Eq. (7), we have

$$A_v \approx 2 \times \frac{1 - \sqrt{\frac{1}{2} + \left(\frac{1}{2} - I_{C2}/I_{SS}\right)}}{1 - \sqrt{\frac{1}{2} - \left(\frac{1}{2} - I_{C2}/I_{SS}\right)}} = 2 \times \frac{1 - \sqrt{\frac{1}{2} + x}}{1 - \sqrt{\frac{1}{2} - x}}, \quad -\frac{1}{2} \leqslant x < \frac{1}{2} \qquad (8)$$

For $x \to 0$, Equation (8) can be simplified using a Taylor series approximation to

$$A_v \approx 2 \times \frac{1 - \frac{\sqrt{2}}{2}(1 + x)}{1 - \frac{\sqrt{2}}{2}(1 - x)} = 2 \times \frac{(\sqrt{2} - 1) - x}{(\sqrt{2} - 1) + x} = b \times \frac{1 - ax}{1 + ax} \sim b\exp(-2ax) \qquad (9)$$

where $a = \frac{1}{\sqrt{2} - 1}$ and $b = 2$. Therefore, the voltage gain expressed in Eq. (7) can provide linear-in-dB gain control characteristic. The plot of Eq. (7) in dB-scale as a function of I_{C2}/I_{SS} is shown in Fig. 3.

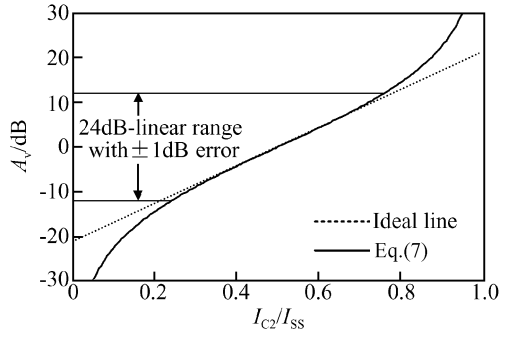

Fig. 3　dB-scale plot of Eq. (7) where the constant "2" in Eq. (7) is omitted for clarity

As can be seen from Fig. 3, a linear range of only about 24dB with a linearity error less than ±1dB is provided. From Fig. 3, we see that in order to increase the dB-linear range I_{C2} should be compressed compared to the linear variation around the center where $I_{C2}/I_{SS} = 0.5$. This idea is just the same as what was proposed in Ref. [13].

A control circuit that generates three control currents I_{C1}, I_{C2} and I_{SS} is shown in Fig. 4. A differential pair (M19, M20) with two diode connected loads (M23, M24) is used to generate I_{C1} and I_{C2}, which realizes a relatively linear function of I_{C2}/I_{SS} (or I_{C1}/I_{SS}) to small variation of V_C, and a nonlinear compression function with increasing V_C. Transistor M27 is designed to be size-controllable to realize a controllable gain variation range, as shown in Fig. 4, where three digital bits are used to control the mismatch current I_Δ. Gain variation ranges provided by the proposed VGA are given in Table 1 for different mismatch

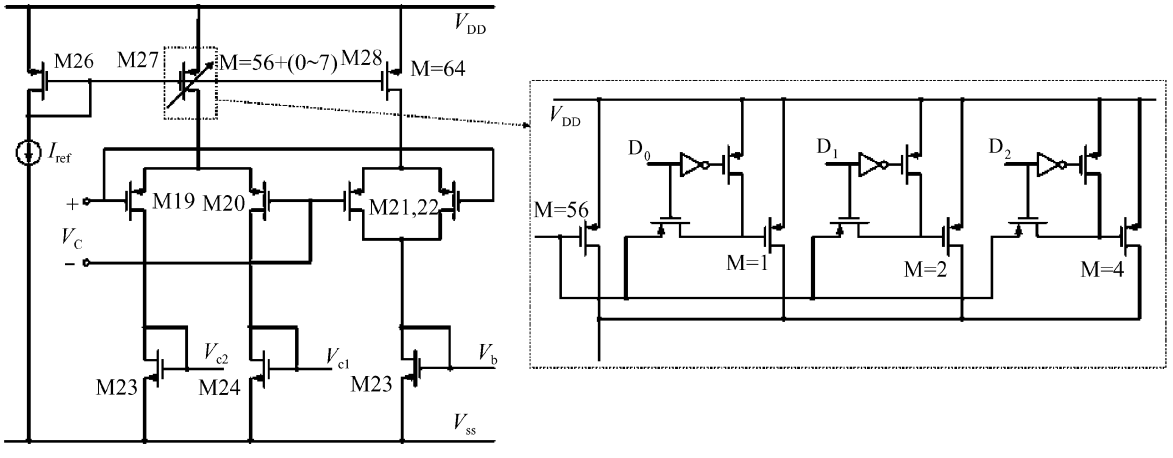

Fig. 4　Circuit schematic of the control stage

currents. The gain error between theory and simulation is mainly caused by the accuracy of the current mirrors. From Table 1, the largest gain variation range is about 80dB for a mismatch factor of 1/64, which is close to that in Refs. [8] and [11]. To ensure performance stability with the process variation, we choose a mismatch factor of 3/64 as the default design parameter; the following simulation results are all based on this assumption.

Table 1 Gain variation range of the proposed VGA for different mismatch currents

Mismatch factor I_Δ/I_{SS}	$D_2D_1D_0$	Total gain variation range/dB		dB-linear range within ±1.5dB error
		Theoretical	Simulation	
1/64	111	84.22	79.6	64.6
2/64	110	72.11	70.1	62
3/64	101	65	64.5	56.5
4/64	100	59.93	57.2	52.2
5/64	011	55.98	53.1	48.2
6/64	010	52.74	49.8	44.5
7/64	001	49.99	47.6	42.6
8/64	000	47.59	45.2	40.7

3.3 Design consideration for temperature variations

A temperature-insensitive gain control characteristic over wide temperature and gain ranges is desired. Figure 5 gives the simulation result of the temperature variation of the proposed VGA without temperature compensation. It shows poor temperature-independence, with the largest gain error being about 8dB.

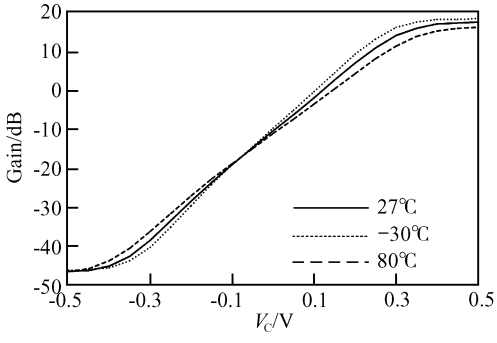

Fig. 5 Gain versus control voltage V_C at different temperatures without temperature compensation

In order to analyze the temperature sensitivity of voltage gain to gain control voltage V_C, we need to reconsider the voltage gain expressed in Eq. (4) including the gain control stage as shown in Fig. 4. We define the differential output of control currents I_{C1} and I_{C2} as

$$\Delta I_{C,d} = I_{C1} - I_{C2} \approx \frac{\partial I_{C,d}}{\partial V_C}\Delta V_C = g_{m19,20}\Delta V_C \approx \sqrt{K_P(W/L)_{19,20}I_{SS}}\Delta V_C \quad (10)$$

where $K_P = \mu_p C_{ox}$, and I_{SS} is the tail current of the differential pair (M26, M27). Thus, I_{C1} and I_{C2} can be expressed as

$$I_{C1} = \frac{I_{SS}}{2} + \frac{\Delta I_{C,d}}{2} \quad (11)$$

$$I_{C2} = \frac{I_{SS}}{2} - \frac{\Delta I_{C,d}}{2} \quad (12)$$

Substituting Eqs. (10) ~ (12) into Eq. (4) and using Taylor series approximation, we obtain

$$A_v = 2 \times \frac{\sqrt{I_{SS}} - \sqrt{\frac{I_{SS}}{2} + \frac{\Delta I_{C,d}}{2}}}{\sqrt{I_{SS}} - \sqrt{\frac{I_{SS}}{2} - \frac{\Delta I_{C,d}}{2}}} \approx 2 \times \frac{\sqrt{2} - 1 - \frac{\Delta I_{C,d}}{I_{SS}}}{\sqrt{2} - 1 + \frac{\Delta I_{C,d}}{I_{SS}}} = 2 \times \frac{\sqrt{2} - 1 - \sqrt{\frac{K_P(W/L)_{19,20}}{I_{SS}}}\Delta V_C}{\sqrt{2} - 1 + \sqrt{\frac{K_P(W/L)_{19,20}}{I_{SS}}}\Delta V_C} \quad (13)$$

Therefore, in order to realize temperature-independent gain, the current I_{SS} should be of the same temperature coefficient as K_P, which is a decreasing function of temperature. The easiest way to get a current preoperational to K_P is to bias a pMOS transistor in the saturation region by a temperature-independent VGS, but independence from power supply and process cannot be ensured. A practical bias circuit to generate I_{ref} in Fig. 4 is shown in Fig. 6, which consists of a temperature-independent current I_2, a preoperational-to-temperature current (PTC)[14], and a current subtraction circuit. The bias current I_{ref} is given as

$$I_{ref} = I_2 - I_1 = I_2 - \frac{2}{\mu_n C_{ox}(W/L)} \times \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right) \quad (14)$$

In Eq. (14), I_1 is proportional to temperature while I_2 is independent of temperature; therefore, I_{ref} is a decreasing function of temperature.

4 Simulation results

The proposed VGA with bias generator is implemented in 0.25μm CMOS technology and verified using Agilent advance design system (ADS). The simulation results are all based on the mismatch factor of 3/64 as depicted in Fig. 4. The VGA dissipates a constant current of less than

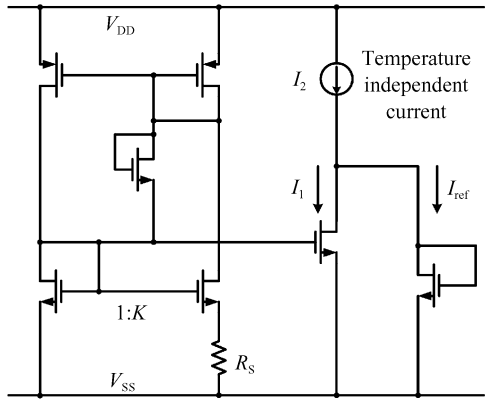

Fig. 6　Proposed bias circuit to generate I_{ref} for temperature-independent gain

6.6mA from a 2.5V supply voltage.

Figure 7 shows the small-signal voltage gain versus control voltage V_C at 20MHz for three temperatures (−30, 27, 80℃). Compared to the gain control characteristic of the uncompensated VGA (as shown in Fig. 5), the linear-in-dB gain control characteristic is achieved over the full temperature and gain range. The total gain variation range obtained from a single variable-gain stage is 64.5dB, and the linear-in-dB gain range with less than ±1.5dB error is 56.5dB as shown in Fig. 8.

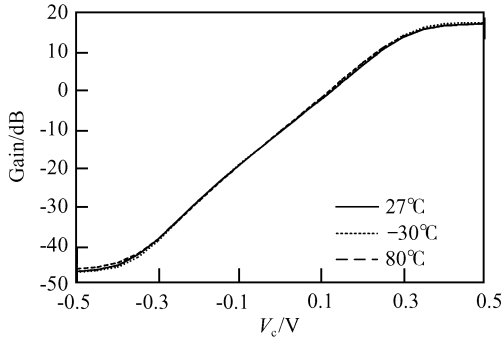

Fig. 7　Gain versus control voltage V_C at different temperatures of the proposed VGA with the bias generator shown in Fig. 6

The frequency response of the proposed VGA is shown in Fig. 9. The 3dB bandwidth is 65MHz at a maximum gain of 18.5dB, and 860MHz at a minimum gain of −46dB. Figure 10 shows the simulated P_{-1dB} of the proposed VGA as a function of gain, which varies from −17.5 to 11.5dBm. The overall VGA performance and a comparison with other works are given in Table 2. As shown in Table 2, the proposed VGA achieves the largest gain variation range using a single variable-gain stage, while maintaining other performances (power consumption, bandwidth, linearity) comparable with other works. Although, at present, only the simulation results are given, the measurement results of the proposed VGA are expected soon, thanks to related works contributed by Duong[12] and Yun[11], in which similar variable cells (as shown in Fig. 1) were used.

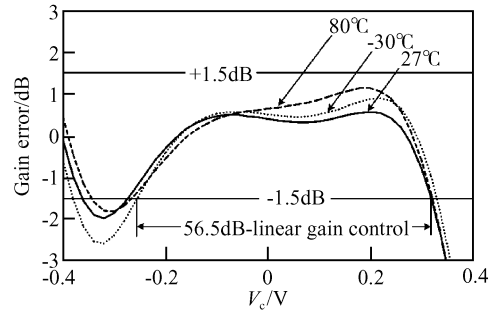

Fig. 8　Decibel-linear gain error versus control voltage V_C at different temperatures (f = 20MHz)

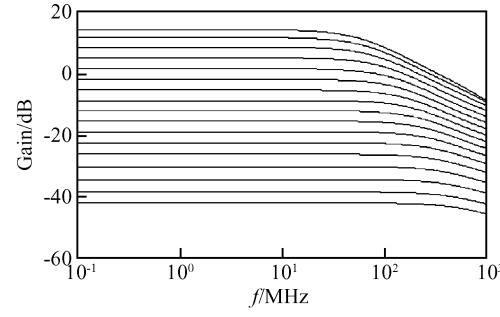

Fig. 9　Frequency response for different control voltage V_C (V_C = −0.3～0.3, step = 37.5mV)

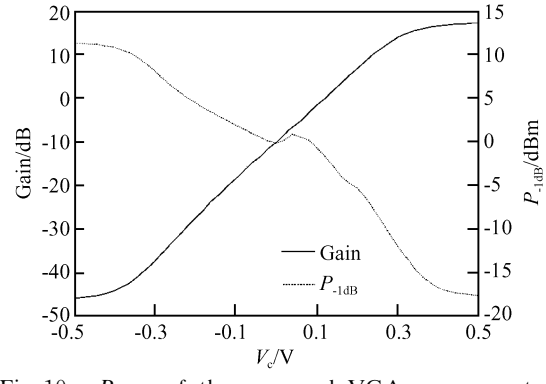

Fig. 10　P_{-1dB} of the proposed VGA versus control voltage

Table 2 Overall performance summary of the proposed VGA and comparison

Ref.	Year	CMOS technology	3dB bandwidth /MHz	P_{-1dB} /dBm	Power consumption	Gain range/Number of stages	Gain variation in one stage/dB
[1]	1995	2μm	85	*	10mW	30/2	15
[6]	1997	0.4μm	71	−57.6～13	6mW/3V	81/3	27
[2]	1998	0.5μm	150	*	12.5mW/3.3V	15/1	15
[4]	1998	2μm	6	*	2.9mW/3V	30/1	30
[3]	2002	0.25μm	30～210	−40～−8	27.5mW/2.5V	80/4	20
[7]	2003	0.18μm	350	−32～10	5.4mW/1.8V	84/3	28
[8]	2004	0.18μm	2000	*	40mW/1.8V	50/1	50*
[11]	2005	0.25μm	106	−40～−4	76.8mW/3.3V	40/1	40
[12]	2006	0.18μm	32～1050	−48～−17	6.5mW/1.8V	95/2	47.5
This work	2006	0.25μm	65～860	−17.5～11.5	16.5mW/2.5V	64.5/1	64.5

* Linear-in-magnitude gain control

5 Conclusions

An all-CMOS variable gain amplifier with a wide gain control range realized in a single variable-gain stage is proposed. The VGA is composed of a variable transconductor and a novel variable output resistor. Theoretically, the gain dynamic range of the proposed VGA is improved by a factor of 2 compared to the traditional one, which is only composed of a variable transconductor. Furthermore, a control circuit realizing *V-I* conversion is also proposed to achieve temperature-independent and wide-range linear-in-dB gain control characteristics corresponding to the control voltage. Simulated in 0.25μm CMOS technology, the proposed VGA provides a total gain variation of 64.5dB and a 56.5dB-linear range with a linearity error of less than ±1.5dB. The current dissipation is less than 6.6mA from a 2.5V supply voltage.

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具有温度补偿及 dB 线性增益控制的单级宽范围 CMOS 可变增益放大器

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摘要：提出了一种新颖的宽范围 CMOS 可变增益放大器结构.利用可变跨导和新颖的可变输出电阻，基于单独可变增益级的放大器可提供 80dB 的宽范围调节.同时控制电路的设计完成了温度补偿及 dB 线性增益特性，实现在整个温度及增益调节范围内绝对增益误差小于 ± 1.5dB.基于 0.25μm CMOS 工艺验证表明，放大器可提供 64.5dB 的增益变化范围，其中 dB 线性范围为 55.6dB.输入 1dB 压缩点为 − 17.5 到 11.5dBm，3dB 带宽为 65MHz 到 860MHz，2.5V 电源供电下功耗为 16.5mW.

关键词：dB 线性；温度补偿；可变增益放大器；自动增益控制

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