Integrated Delta-Sigma 1. 5bit Power DAC with 100dB Dynamic Range

Li Dan[1,†]， Liang Jiayi[1]， Hong Zhiliang[1]， and Xu Gang[2]

（1 *State-Key Laboratory of ASIC & System*，*Fudan University*，*Shanghai*　201203，*China*）
（2 *Accel Semiconductor*，*Shanghai*　201203，*China*）

Abstract：A stereo 1. 5bit delta-sigma digital-analog converter（$\Delta\Sigma$ DAC）integrated with a filterless class D power amplifier is introduced. It consumes no static power，and its maximum output power is 436mW with an 8Ω load. Its output dynamic range exceeds 100dB. The circuit is implemented with a TSMC 0. 18μm process. The die area is 0. 28mm². The supply voltage is 1. 8V for the digital part and 3. 3V for class D.

Key words：delta-sigma DAC；filterless class D power amplifier；interpolator；power DAC
EEACC：1265H；1270F；1265A
CLC number：TN432　　　**Document code**：A　　　**Article ID**：0253-4177(2007)05-0651-04

1　Introduction

The past five years have been a golden time for the development of consumer electronic products. According to the prediction of the Internet Data Corporation（IDC），the multimedia market，including MP3 players，PDAs，DV cameras，and portable phones，will increase by at least 230% from 2004 to 2007. Therefore，the design of audio DACs，which are necessary components of these multimedia products，is also attracting much attention.

The delta-sigma DAC is the most popular structure for audio signal processing. A typical $\Delta\Sigma$ DAC consists of a digital interpolator，a digital $\Delta\Sigma$-modulator（DSM），a 1bit DAC，and an analog signal reconstruction filter[1]. Since multimedia products require portability and low power-consumption，today's audio DACs are often integrated with linear power amplifiers（PA）to drive a load such as a speaker directly[2].

The majority of the silicon area of DACs is occupied by digital circuitry whose area and power consumption are dropping dramatically with the development of technology scaling. The analog part，including a reconstruction filter and a PA，then becomes the bottle-neck for further improving DAC technology. In the new generation of CMOS processes，it is becoming more and more expensive to implement linear capacitors in the SC reconstruction filter. Moreover，the filter and linear PA introduce harmonic distortion and consume much power.

In this paper，a delta-sigma power DAC with filterless class D power amplifier is introduced. The proposed power DAC removes the reconstruction filter and replaces the linear PA with a filterless bridge-tied-load（BTL）differential-drive class D amplifier whose power efficiency is much higher. Its 3-level（1. 5bit）output can reduce the circuit's current consumption further. The proposed DAC can be conveniently applied as macro blocks in audio codecs and can more easily undergo a process migration following the fast evolution of the digital processes than can traditional structures. The supply voltage is 1. 8V for the digital circuitry and 3. 3V for the class D amplifier. The maxim output power is 436mW，and the measured dynamic range exceeds 100dB.

2　Architecture of the 1. 5bit DS power DAC

Figure 1 shows the signal flow diagram of the 1. 5bit DS power DAC. The 16bit digital input is first interpolated 64 times and then applied to the digital 4th-order 1. 5bit DSM. The output of the modulator is converted to three voltage levels and drives headphones or speakers through a BTL class D amplifier. Since the DAC is used for audio codecs and people's ears can only perceive signals

between 20Hz and 20kHz, no filters are needed to remove the noise beyond 20kHz. The power supply for the class D amplifier is 3.3V, while the digital circuit operates at 1.8V to reduce the digital power consumption and switching noise.
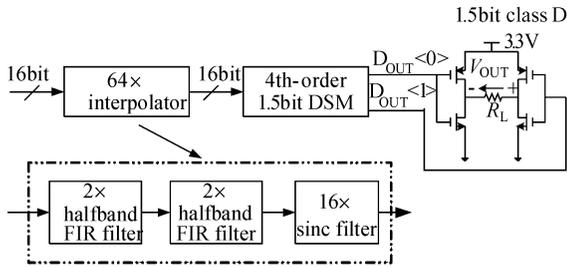

Fig.1   Signal flow diagram of the 1.5bit $\Delta\Sigma$ power DAC

2.1   Interpolator design

A high over-sampling rate (OSR) can depress the in-band quantization noise and reduce the order needed for the $\Delta\Sigma$ modulator[3]. Thus an interpolator is used here to enhance the OSR and filter the image. The order of the interpolator increases with the sample frequency and the width of the filter's transition band[4]. To reduce the order of the interpolator, a cascade structure is used with two FIR half-band interpolation filters and one band-pass interpolation filter (as shown in Fig.1). The half-band filters increase the OSR of the input digital signal by 2 times, and the band-pass filter increases the OSR by 16 times. Since the transition bandwidth of the first filter is the narrowest, its order is the highest. To reduce the circuit cost, this filter is designed as one prototype filter with several sub-filters[1,4]. The structures and coefficients of the sub-filters are completely identical. As expressed in Eqs.(1) and (2), if the prototype filters consist of $2m - 1$ sub-filters whose order is $2n - 1$, the order of the prototype filter (F_{prot}) is $(2m-1)(2n-1)+1$:

$$F_{\text{sub}}(z) = z^{-m} \sum_{k=0}^{m-1} f_2(m-k)(z^{m-k} + z^{-m+k}) \quad (1)$$

$$F_{\text{prot}}(z) = z^{-(2n-1)(2m-1)} + 2\sum_{i=0}^{n-1}\{f_1(n-i) \times$$
$$[F_{\text{sub}}(z^{-2})]^{2i+1}(z^{-2})^{(2m-1)(n-i-1)}\} \quad (2)$$

Then only one sub-filter needs to be realized with hard-ware, which can be reused $2n - 1$ times to implement the high order prototype filter.

2.2   Design of the 1.5bit $\Delta\Sigma$ modulator

The structure of the 4th digital $\Delta\Sigma$ modulator is shown in Fig.2. It shapes the quantization noise to a higher frequency band and then satisfies the required in-band SNR. To drive a low resistive load such as speakers or headphones, the output power of the modulator must be amplified. For a traditional linear PA, the quantization noise at high frequency must be filtered by the reconstruction filter in advance, and the order of the filter must be higher than that of the delta-sigma modulator[5]. Such a high order filter occupies a large area, consumes great power, and introduces some distortion as well.
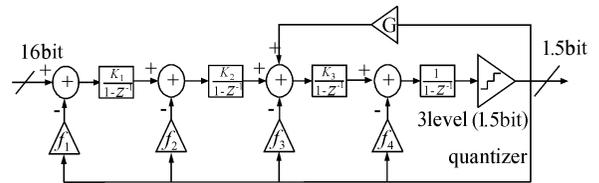

Fig.2   1.5bit 4th $\Delta\Sigma$ modulator

To solve these problems, a 1.5bit $\Delta\Sigma$ modulator is proposed in this paper. Its output is a 3-level code ("00", "10", and "01") that is applied directly as the input of a class D amplifier. Since this power DAC is applied for audio codecs, the person's ear is an initial low pass filter (pass band is 20Hz～20kHz), so no post-filter is needed for the class D power amplifier. Compared with the traditional structure, the 1.5bit structure can achieve better SNR and equally good linearity.

Moreover, the efficiency of the 1.5bit filterless class D amplifier is also higher than that of a 1bit one. As shown in Fig.3, the differential output varies between positive and negative power supply for a 1bit class D amplifier because its load is low resistance. Then the current through the load is always high, which causes high power loss.
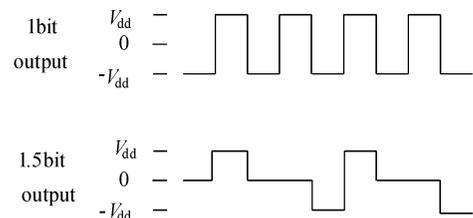

Fig.3   Class D amplifier output voltage across load

For a 1.5bit class D amplifier, the voltage across the load is set at 0 during most of the working time when the output of the modulator is "00". This greatly reduces both the I^2R loss in the load and the switching power loss.

2.3 Class D amplifier

The class-D output stage not only provides large driving to the load, but also acts as a 1.5bit DAC. It is critical to ensure that the signals in each branch of the differential path have equal rise and fall times. Then the layout of the output stage transistor should be designed to be as compact and symmetric as possible. Compared with conventional finger transistors, the bent-gate transistor as shown in Fig.4 can increase the gate width while simultaneously allowing the gate strips to be packed more closely. The use of 135° bends is less prone to localized avalanche than 90° bends and can improve robustness under extreme conditions, such as those encountered during ESD testing. Moreover, it simplifies metallization and backgate contact distribution. The source and substrate of the transistor can be very close. Then this layout pattern is insusceptible to backgate debiasing and latchup.
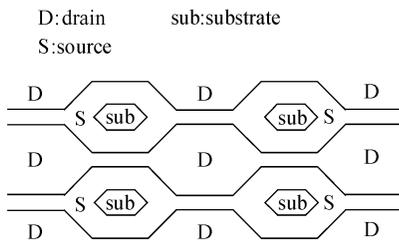
3 Measured results

The chip micrograph of the integrated stereo delta-sigma power DAC is shown in Fig.5. The chip is implemented with a TSMC 0.18μm CMOS process. The power supply is 1.8V for digital circuits and 3.3V for the class D amplifier. The scale of the digital circuit is 47,000 gates and the die area for the two-channel class D amplifier is 0.28mm^2. The maximum output power of the useful audio signal is 436mW with an 8Ω load. The chip was measured with an ATS-2 audio test system. As shown in Fig.6, the floor noise is about -100dBv（7.75μV）and the output dynamic range exceeds 100dB. The total harmonic distortion（THD）is less than 0.02% and the THD + N （in-band noise）is less than -72dB. The detailed measured results are listed in Table 1.

D:drain   sub:substrate
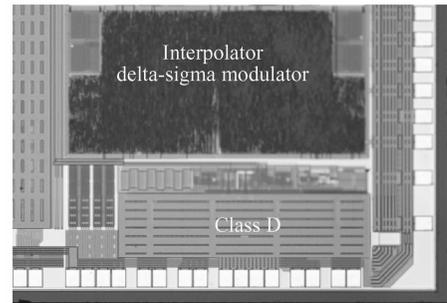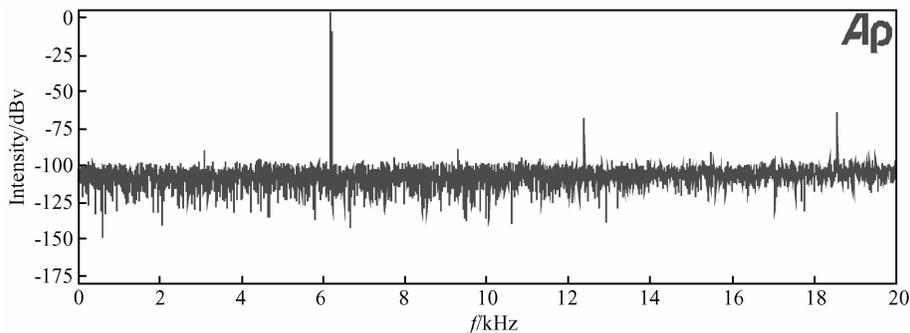S:source

Fig.4   Bent-gate transistor

Fig.5   Chip microphotograph

Fig.6   Measured output spectrum of the power DAC

Table 1　Measured results of the chip

Specification	Performance	Comment
Output swing	± 2.64V	Differential, $R_{\text{load}} = 8\Omega$
Dynamic range	100dB	20kHz BW, $f_s = 48$kHz
THD	$<0.02\%$	@ 6kHz (20kHz BW, $f_s = 48$kHz)
THD + Noise	<72dB	@ 6kHz (20kHz BW, $f_s = 48$kHz)
Maxim output power	436mW	$R_{\text{load}} = 8\Omega$
Chip size	0.28mm^2	Two channel
Power supply	$V_{\text{DDD}} = 1.8$V $V_{\text{DDP}} = 3.3$V	V_{DDD} for digital circuit, V_{DDP} for class D amplifier

4　Conclusion

In this paper, a novel audio power DAC was presented. Compared with the traditional structure, it avoids the usage of a reconstruction filter and replaces the linear PA with a 3-level (1.5bit) class D amplifier whose efficiency is much higher. It consumes no static power. The 3-level output greatly reduces the I^2R losses in the load and the switching power loss. The tested output dynamic range of the power DAC exceeds 100dB.

References

[1]　Peng Yunfeng, Kong Derui, Zhou Feng. Design and implementation of a novel area-efficient interpolator. Chinese Journal of Semiconductors, 2006, 27(7): 1164

[2]　Pernici S. Fully integrated voiceband codec in a standard digital CMOS technology. IEEE J Solid-State Circuits, 2004, 39(8): 1331

[3]　Steven R N, Schreier R, Temes G C. Delta-Sigma data converters. New York: Institute of Electrical and Electronics Engineers, 1996

[4]　Tapio S. Design of FIR filters as a tapped cascaded interconnection of identical sub-filters. IEEE Trans Circuits Syst, 1987, 34(9): 1011

[5]　Fujimori I, Nogi A, Sugimoto T. A multibit delta-sigma audio DAC with 120-dB dynamic range. IEEE J Solid-State Circuits, 2000, 35(8): 1066

[6]　Chang J S. Analysis and design of power efficient class D amplifier output stages. IEEE Trans Circuits Syst, 2000, 47(6): 897

一种 100dB 输出动态范围的 1.5bit 功率数模转换器

李　丹[1,†]　梁嘉义[1]　洪志良[1]　许　刚[2]

(1 复旦大学专用集成电路与系统国家重点实验室，上海　201203)
(2 捷顶微电子有限公司，上海　201203)

摘要：介绍了一种 1.5bit 的双声道过采样数模转换器. 它把过采样数模转换器和 D 类功率放大器这两部分集成在一起，不需要额外的低通滤波器即可直接驱动耳机扬声器等语音设备. 它无需消耗直流功耗，对于常用的 8Ω 扬声器负载，其最大输出功率可达 436mW，输出动态范围大于 100dB. 该电路采用 TSMC 0.18μm 工艺实现. 芯片面积为 0.28mm^2，其中数字电路的电源电压为 1.8V，D 类功率放大器的电源电压为 3.3V.

关键词：过采样数模转换器；不带滤波器的 D 类功率放大器；插值滤波器；功率数模转换器