Sensitivity Design for a CMOS Optoelectronic Integrated Circuit Receiver*

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Abstract: A sensitivity design method for a CMOS optoelectronic integrated circuit (OEIC) receiver is reported. The receiver consists of a regulated cascade (RGC) transimpedance amplifier (TIA) and a double photodiode (DPD) detector. The noise and sensitivity of the receiver are analyzed in detail. The noise mainly comes from the thermal noise of resistors and the flicker noise of MOSFETs. The relationship between noise and receiver sensitivity is presented. The sensitivity design method for the receiver is given by a set of equations. The OEIC receiver was implemented in a CSMC 0.6μm standard CMOS process. The measured eye diagram shows that the CMOS OEIC receiver is able to work at bit rates of up to 1.25GB/s and the sensitivity is -12dBm.

Key words: CMOS; OEIC; receiver; sensitivity; noise
EEACC: 4250; 1220
CLC number: TN303 **Document code**: A **Article ID**: 0253-4177(2007)05-0676-05

1 Introduction

With the increase of chip and system clock frequencies, electrical interconnects on boards and between boards have become a bottleneck of IC systems. Optical interconnects and optical data transmission via fibers are alternatives to avoid the problem[1]. The photoreceiver is a key device in optical interconnects and optical data transmission. Generally, photoreceivers must have high sensitivity, high speed, and a high gain-bandwidth product. A large number of photoreceivers have been proposed and studied over the past few decades for improving their performances with respect to the above characteristics. The integration of the photodetector with the required circuitry is desirable for a photoreceiver. Optoelectronic integrated circuit (OEIC) receivers will be needed in future years for optical interconnection and optical data transmission.

CMOS OEICs can eliminate some parasitic effects caused by wire-bonding between optoelectronic devices and Si-based signal processing circuits, thus increasing the band-width and decreasing the noise of the optoelectronic system. Some work on this field has been reported[1~3] by Woodward and Krishnamoorthy[3,4], showing that DPD detectors can be fabricated in commercial CMOS technology without any process modification. Their OEIC receiver can operate at 1Gbit/s in a 0.35μm CMOS process[4,5]. However, no noise analysis or sensitivity design method for the OEIC receiver was presented. Park and Yoo[6,7] demonstrated a 2.5GHz regulated cascade (RGC) TIA in a 0.6μm CMOS process, but they only gave the noise analysis of the RGC TIA, not including the photodiode. The important performance and sensitivity of the OEIC receiver were not given.

In this paper, we demonstrate the noise analysis and sensitivity design method for a CMOS OEIC receiver. A photograph of the fabricated chip and the measured results will be also illustrated.

2 System structure

As shown in Fig. 1, the CMOS OEIC receiver front-end consists of one DPD, one RGC TIA used to convert the weak current detected by the PD into a voltage signal, and an MA that amplifies the voltage signal of the TIA and boots the signal

* Project supported by the National Natural Science Foundation of China (Nos. 60536030, 60676038) and the Key Project for Fundamental Research of Tianjin (No. 06YFJZJC00200)
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Received 30 October 2006, revised manuscript received 20 December 2006

swing to logic levels. An output buffer is used to make measurement convenient. For the design of high sensitivity, we should optimize the noise of the CMOS OEIC receiver system, especially of the DPD and TIA, because the noise of other units can be neglected when compared to these two parts.

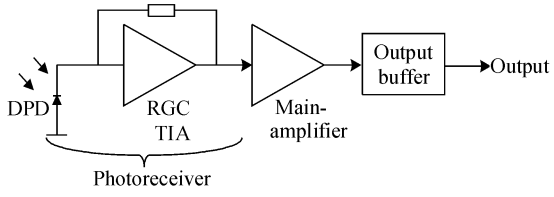

Fig. 1　System structure of the OEIC receiver

3　TIA circuit topology

Figure 2 shows a schematic diagram of the RGC TIA. M1 and M2 make up the RGC input stage and form the first gain stage. Due to the low impedance characteristics of the RGC circuit, the total input capacitance determines the non-dominant pole of the amplifier. A common drain stage (M3) is inserted between the RGC input stage and the trans-conductance stage, and works as a voltage follower. Without this voltage follower stage, the large input capacitance of M4 will restrict the circuit bandwidth. Meanwhile, this inserted voltage follower increases the total noise and reduces the open-loop gain. Therefore it is necessary to optimize the size of M3 for the desired bandwidth, gain, and noise. The common source stage (M4) is the second voltage gain stage. For wide bandwidth, its gate-width should be selected to be small because of C_{gs4}. M5 and M6 are output buffers.

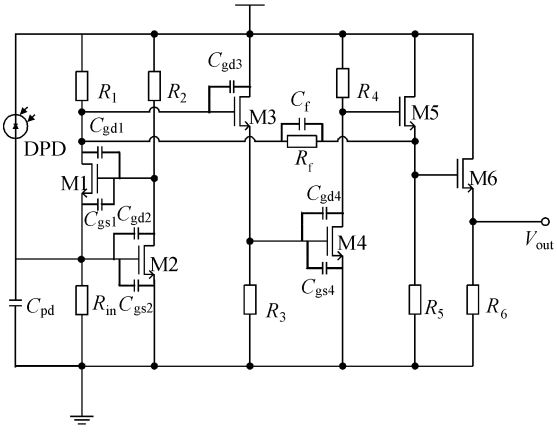

Fig. 2　Schematic diagram of the RGC TIA (with capacitors used in the noise analysis)

The feedback resistor R_f is not applied to the source of M1, but to the drain of M1. There are two reasons[8,9] for this scheme. First, it is desirable for the DC bias conditions not to be altered along with adding the feedback resistor R_f; otherwise, the DC voltages at each node of R_f should be as close as possible, and hence the feedback resistor is preferably fed back to the drain of M1. Second, the bandwidth extends a few times due to the parallel combination of R_1 and R_f with the Miller gain. Also, due to the Miller effect, the feedback resistor R_f can be made larger than R_1, providing lower thermal noise and higher transimpedance gain.

4　Noise and sensitivity analysis

4.1　Noise analysis of DPD

The noise of the DPD detector system is caused mainly by the surface leakage current[10] and the equivalent input noise current. The surface leakage current spectral density can be described by

$$\langle \overline{i_{DPD}^2} \rangle = 2qI_{du} \tag{1}$$

Here, I_{du} is the surface leakage current of the DPD detector.

4.2　Noise analysis of the RGC TIA

According to the noise analysis steps in Ref. [11], by a series of complex derivation, the equivalent input noise current spectral density of the RGC TIA can be described by

$$\begin{aligned}\langle \overline{i_{RGC}^2} \rangle = {} & \frac{4kT}{R_f} + \frac{4kT}{R_{in}} + \frac{4kT}{R_1} + 2qI_{g1} + 2qI_{g2} + 2qI_{g3} + \\ & \frac{3kT}{3g_{m2}}\left[\frac{1}{R_{in}^2} + \omega^2(C_{pd} + C_f + C_{gs2} + C_{gd2} + C_{gs1})^2\right] + \\ & \frac{3kT}{3g_{m3}}\left[\left(\frac{1}{R_1} + \frac{1}{R_f}\right)^2 + \omega^2(C_f + C_{gd1} + C_{gd3})^2\right] + \\ & \left\{4kTR_3 + 2qI_{g4}R_3^2 + \frac{3kT}{3g_{m4}}[1 + \omega^2 R_3^2(C_{gs4} + C_{gd4})^2]\right\} \times \\ & \left[\left(\frac{1}{R_1} + \frac{1}{R_f}\right)^2 + \omega^2(C_f + C_{gd1} + C_{gd3})^2\right]\end{aligned} \tag{2}$$

The first three terms in Eq. (2) represent the thermal noise contributions given by R_f, R_{in}, and R_1, respectively. The next three terms are noise contributions caused by gate leakage currents of M1, M2, and M3, which can be assumed to be negligible. The rest represent the equivalent current noise at the gate of M3. The voltage and current

noise sources of M4 are referred back to the gate of M3 and shown as an equivalent voltage noise source. This voltage noise source, plus the voltage noise source of M3, is converted to the current noise source at the drain of M1.

According to Eq. (2), R_f, R_{in}, R_1, g_{m2}, g_{m3}, and g_{m4} should be made as large as possible to reduce the total noise. To increase g_{m2}, either the width of M2 or the bias current of M2 can be increased. Large W_2 means a large capacitance C_{gs2}, which will increase noise and reduce the stability due to the decrease of the non-dominant pole at the input terminal. Large bias current means that R_2 should be reduced, but the noise will be increased again consequently. In this design, an advisable choice of the optimal width and the optimal bias current gives a minimum noise and maximum R_f and bandwidth.

The total equivalent input noise current spectral density of the COMS OEIC receiver is the sum of the two components and is thus given by

$$\langle \overline{i_{total}^2} \rangle = \langle \overline{i_{DPD}^2} \rangle + \langle \overline{i_{RGC}^2} \rangle \tag{3}$$

4.3 Sensitivity analysis of the CMOS OEIC receiver

The mean-squared input noise current can be deduced from Eq. (3) and is given by[10]

$$\overline{i_n^2} = \int_0^B \langle \overline{i_{total}^2} \rangle \mathrm{d}f \tag{4}$$

Here B is the operation bandwidth of the receiver.

In CMOS OEIC receivers the number of photo-generated electrons contained in a single bit is usually very large (i. e. $\geqslant 10^4$). Thus, the use of Gaussian statistics is justified for describing the detection probabilities in p-i-n or the DPD photodiodes. The equal probability or the so called bit-error-rate (BER) can be expressed as[10]

$$\mathrm{BER} = \exp\left(-\frac{Q^2}{2}\right)/\sqrt{2\pi}Q \tag{5}$$

This expression readily yields the conclusion that for the standard BER of 10^{-9}, the value of Q is 6. For all practical purposes, $Q = \sqrt{S/N}$, where S/N stands for the signal-to-noise ratio. The RMS (root mean square) detected photocurrent can be expressed as $i_p = I_p/\sqrt{2}$ for 100% modulation, where I_p is the product of responsivity (R_0) and the incident optical power (P_{opt}), we can express the mean-squared signal current as[12]

$$\overline{i_p^2} = \frac{1}{2}\left(\frac{\eta q P_{opt}}{h\nu}\right)^2 \tag{6}$$

where h is Plank's constant, ν is the optical frequency, and η is the quantum efficiency. The signal-to-noise ratio (S/N) is the same as $\overline{i_p^2}/\overline{i_n^2}$. The sensitivity ($S_n$) is defined as the detectable minimum optical power, i. e. $P_{opt}/\sqrt{2}$, for a specified value of S/N, and it can be expressed as

$$S_n = \frac{P_{opt}}{\sqrt{2}} = \frac{h\nu}{\eta q}\sqrt{S/N}\sqrt{\overline{i_n^2}} \tag{7}$$

Here the responsivity is $R_0 = \eta q/h\nu$.

The mean-squared equivalent noise current is thus given by

$$\sqrt{\overline{i_n^2}} = \frac{P_{opt}}{\sqrt{2}} \times \frac{R_0}{\sqrt{S/N}} \tag{8}$$

For a BER of 10^{-9} it has been shown that $\sqrt{S/N} = 6$.

When the area of the DPD detector is increased, the noise current of the CMOS OEIC receiver will not change a lot. The reason is that though $\langle \overline{i_{DPD}^2} \rangle$ will increase along with the increase of the area of the DPD detector, it is only a very small proportion of $\langle \overline{i_{total}^2} \rangle$. At the same time, for a larger detector area, more photo-current is generated when the optical power is constant, and then more signal current can be obtained. As a consequence, S/N becomes larger; that is to say, BER of the CMOS OEIC receiver can be improved.

5 Simulated results

The simulated results of sensitivity and noise versus frequency characteristics are shown in Fig. 3. The curves in the left coordinate are the sensitivity when the responsivity of the DPD detector is 0.01 and 0.04A/W[2,3], respectively. The curve in the right coordinate is the equivalent input noise current. When the bandwidth is 1.25GHz and the responsivity is 0.01 and 0.04A/W, the sensitivity of the CMOS OEIC receiver is approximately -6.38 and -12.4dBm, and the equivalent input noise current is 0.27μA. As the bandwidth is 1.71GHz and the responsivity changes from 0.01 to 0.04A/W, the sensitivity of the OEIC receiver shows approximately -5.62 and -11.65dBm, correspondingly. Thus the sensitivity of the CMOS OEIC receiver is evidently improved with a higher responsivity. Nevertheless, a

larger area of the detector is necessary for a better S/N, which becomes a pressure to the RGC TIA. Thus, an appropriate trade-off among these many parameters is important.

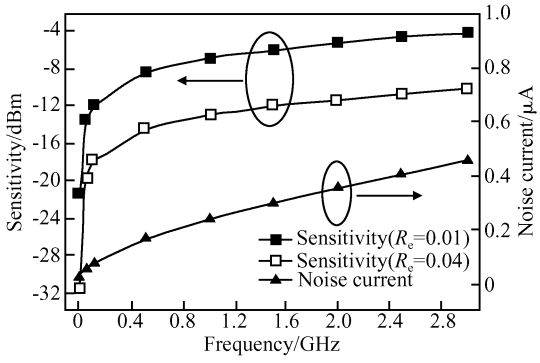

Fig. 3　Detectable minimum optical power (sensitivity) and equivalent input noise current of the CMOS OEIC receiver versus frequency characteristics

6　Chip implementation and measurement results

This CMOS OEIC receiver has been realized in a CSMC-HJ (a foundry in Wuxi, China) 0.6μm CMOS process. Figure 4 shows a photograph of the photoreceiver.

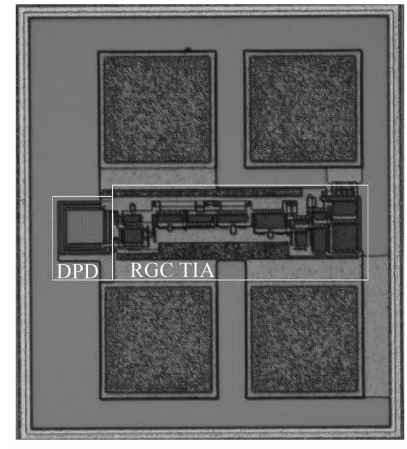

Fig. 4　Photograph of the CMOS OEIC receiver

The achieved CMOS OEIC receiver is measured with a 1.25GB/s pseudorandom bit sequence (PRBS) signal at the input. The responsivity of the DPD is 0.04A/W, and the sensitivity of the CMOS OEIC receiver is estimated to be −12dBm. That is to say, the achieved CMOS OEIC receiver can respond when the optical signal is about 63μW. Figure 5 shows the eye diagram at −12dBm signal input. From the eye diagram, the signal output voltage swing is 288.84mV, RMS jitter is 40ps, and the signal to noise ratio (S/N) is about 36, so the value of Q is 6.

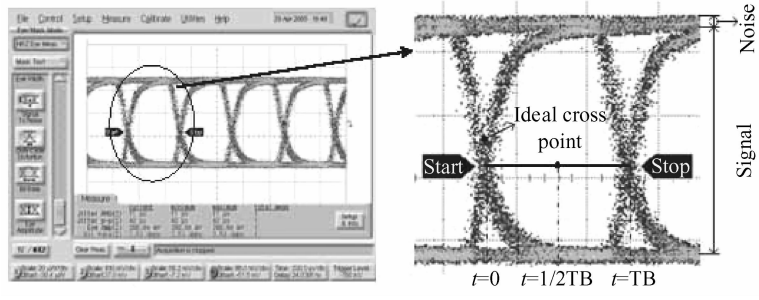

Fig. 5　Eye diagram of the OEIC receiver

The sensitivity of the real chip is a little lower than simulated value. That is partially because in simulating we use the operating frequency (1.25GHz) and when measuring the chip we use PRBS (1.25GB/s) signal; and partially due to the difference between real processing parameters and the model parameters used in simulation.

7　Conclusions

In this paper, a CMOS OEIC receiver with 1.25GHz bandwidth and −12dBm sensitivity was introduced. The noises in the receiver are mainly from the DPD and RGC TIA. Reducing the noise from these two parts can optimize the sensitivity of the whole receiver. The chip was fabricated using a CSMC 0.6μm standard CMOS process. From the measured eye diagram we can see that the receiver can be operated at bit rates of 1.25GB/s with 10^{-9} BER. The simulated and measured results show that the achieved CMOS OEIC receiver has the merits of low noise, low

cost, and monolithic integration, and can be used in ultra high-speed optoelectronic communication systems.

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高灵敏度 CMOS 光电集成接收机设计*

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摘要： 设计了一个由调节型级联跨阻抗放大器(TIA)和双光电二极管(DPD)构成的 CMOS 光电集成(OEIC)接收机.具体分析了这个光电集成接收机的噪声和灵敏度及其相互关系.接收机中的噪声主要是电路中电阻的热噪声和 MOS 器件的闪烁噪声.提出了优化接收机灵敏度的方法.通过低成本的 CSMC 0.6μm CMOS 工艺流片并对芯片进行了测试.从测试眼图可知，该 CMOS 光电集成接收机可工作在 1.25GB/s 的传输速率下，灵敏度为 −12dBm.

关键词： CMOS；光电集成电路；光接收机；灵敏度；噪声

EEACC： 4250；1220

中图分类号： TN303 **文献标识码：** A **文章编号：** 0253-4177(2007)05-0676-05

* 国家自然科学基金(批准号:60536030,60676038)和天津市基础研究重点项目(批准号:06YFJZJC00200)资助项目

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2006-10-30 收到，2006-12-20 定稿