Models and Related Mechanisms of NBTI Degradation of 90nm pMOSFETs

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Abstract: We investigate the negative bias temperature instability (NBTI) of 90nm pMOSFETs under various temperatures and stress gate voltages (Vg). We also study models of the time (t), temperature (T), and stress Vg dependence of 90nm pMOSFETs NBTI degradation. The time model and temperature model are similar to previous studies, with small difference in the key coefficients. A power-law model is found to hold for Vg, which is different from the conventional exponential Vg model. The new model is more predictive than the exponential model when taking lower stress Vg into account.

Key words: NBTI; 90nm; pMOSFETs; model
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1 Introduction

Negative bias temperature instability (NBTI) is an important effect in pMOSFETs. It didn’t receive much attention for the larger devices of the past. However, as device sizes are continually scaling down without appropriate reduction of supply voltages, NBTI is getting more and more serious and has become one of the most important limiting factors of pMOSFET lifetime, especially for device sizes in the ultra-deep sub-micron region[1–3].

Many people have studied NBTI and obtained lots of results, which count for much. However, there is still no model that explains NBTI exactly. In most studies, NBTI is thought to be related to H species[4–6]. As its name NBTI implies, negative bias and temperature play the most important roles in the degradation of pMOSFETs. With the effects of electric field and temperature, SiH bonds break, and therefore generate interface states and oxide positive charges[4–7], which cause the degradation of parameters Vth, Ioff, Ion, Gm and more. To model the effect of severe NBTI on the performance of a pMOSFET, it is important to treat the degradation as dependent on Vg and temperature. In addition, the time model, which has been studied for a long time, is also significant.

In this paper, we examine NBTI degradations of 90nm devices in long term stresses under different conditions, including various Vg and T. Based on the results, models dependent on t, T, and Vg are studied.

2 Devices and experiments

The pMOSFETs used here were fabricated in 90nm process technology with a lightly doped drain (LDD) structure and a shallow trench isolation (STI) scheme. The devices have a channel length of 90nm, width of 10μm, and gate oxide thickness of 1.4nm. The gate oxides of all devices were annealed in N2O gas ambient after thermal growth. The operation voltage is 1.0V. An Agilent B1500A high precision semiconductor parameter analyzer was used to complete the tests. NBTI stress was applied to the gate electrode, with the source, drain, and substrate grounded at elevated
temperatures. Stress testing combined with $I-V$ measurement were performed at 90~150°C in a dark box.

3 Results and discussion

Figure 1 shows the degradation of the transfer characteristics of the pMOSFETs. The pMOSFETs were stressed under $V_{g} = -1.8$ V at 90°C. After 10000s, the drain current appears clearly degraded, and the current in the saturation region is degraded more than that in the linear region. The threshold voltage $V_{th}$ becomes larger than the former. From the inset in Fig. 1, we can see that $G_m$ after 10000s decreases, and the peak point shifts left. This is due to the interface states and fixed oxide charges produced during NBTI stress. From the figure, we can see the serious degradation caused by NBTI clearly. This degradation will result in the final failure of the devices and affect the circuits badly. Therefore, it is important to study NBTI and to found models for key factors.

![Fig. 1 Degradation of transfer characteristics of 90nm pMOSFETs pre- and post-NBTI stress with $V_{g} = -1.8$ V at 90°C for 10000s](image)

The shifts of the pMOSFET parameters with stress $V_{g} = -1.8$ V versus stress time are shown in Fig. 2. $I_{d}(t)$ shifts more than $I_{d}(t)$, indicating that the interface states and oxide fixed charges produced during NBTI stress are located not in the overlap region but in the channel region. The degradation of the threshold voltage $V_{th}$ is the most severe. We will study it to model the degradation caused by pivotal factors.

Figure 3 shows the relation of $V_{th}$ degradation to time at different temperatures or under different stresses $V_{g}$. All data are plotted in a log-log scale. $V_{th}$ shifts show excellent accordance to $t^n$. Though this time model was brought forward a long time ago, and has been confirmed by most studies, the parameter $n$ is different for different devices manufactured by different technologies. And when the device scale reaches 90nm, it is important to identify the $t^m$ model. In Fig. 3 (a), at different temperatures, $n$ shows a nearly constant value of 0.21, and in Fig. 3 (b), $n$ decreases from 0.26 to 0.21 as the stress $V_{g}$ increases. All of these results are similar to those of previous studies and show that the model $\Delta V_{th} = C t^n$ can also account for NBTI degradation of 90nm pMOSFETs.

![Fig. 2 Shifts of 90nm pMOSFET parameters with $V_{g} = -1.8$ V versus stress time](image)

![Fig. 3 $V_{th}$ shift versus stress time at different temperatures (a) or under different $V_{stress}$ (b)](image)
The shift of $V_{th}$ versus temperature under different stresses $V_{g}$ is plotted in Fig. 4 with a log-linear scale. All data under different stresses $V_{g}$ are fitted with $\Delta V_{th} = C \exp(-E_a / KT)$, where $E_a$ is the activation energy. The activation energy $E_a$ of $\Delta V_{th}$ for each stress $V_{g}$ is extracted from the data of Fig. 4. The results are shown in Fig. 5. $E_a$ represents the difficulty of NBTI degradation. In Fig. 5, $E_a$ decreases with increasing stress $V_{g}$, which implies that stress $V_{g}$ plays an important role in NBTI degradation. The range of $E_a$ in Fig. 5 is 0.11 to 0.13 eV, which is smaller than that in previous studies, in which the device scale was larger. From these results, we conclude that higher stress $V_{g}$ and smaller device scale result in the easier occurrence of NBTI degradation. Therefore, we can also use $\Delta V_{th} = C \exp(-E_a / KT)$ as the $T$ model of 90nm pMOSFET NBTI degradation. However, the activation energy is smaller.

From studies on NBTI with regard to time and temperature, we have known the importance of stress $V_{g}$. Accelerated testing is usually used to evaluate the lifetime of devices. A high gate voltage $V_g$ is applied to a pMOSFET to measure its lifetime in NBTI studies. Some researchers have proposed a model of the dependence of lifetime $(\tau)$ on $V_g$ to estimate the lifetime at operation voltages. The conventional exponential model is $\tau = C \exp (-\beta V_g)$, where $C$ and $\beta$ are constants. From this lifetime model, we deduce that the model of $\Delta V_{th}$ is dependent on $V_{g}$ as $\Delta V_{th} = C_1 \exp (\beta_1 V_{g})$, where $C_1$ and $\beta_1$ are also constants. Both of these models are used by manufacturers to estimate the $V_{th}$ shift and lifetime of devices. In this paper, we take the 10% shift of $V_{th}$ as the lifetime definition. The data gained under higher stress $V_{g}$ agree well with both exponential models. However, when the stress $V_{g}$ reaches a smaller value, but still higher than operation voltage, the exponential model departs from the experimental data, as shown in Fig. 6. We change the log-linear scale into a log-log scale, and therefore
make the exponential model into the power-law model \( \tau = C V_{\varepsilon}^\beta \), where \( C \) and \( \beta \) are constants. For all data, lifetime under higher and lower stresses \( V_{\varepsilon} \), the power-law model is more predictive than the exponential model, as shown in Fig. 6 (b). Taking lower stress \( V_{\varepsilon} \) into account, the exponential model underestimates the NBTI lifetime of 90nm pMOSFETs. Therefore, the power-law \( V_{\varepsilon} \) model should be instead of the exponential model to predict the NBTI lifetime of ultra-deep sub-micron MOSFETs. We deduce the \( \Delta V_{th} \) model dependent on \( V_{\varepsilon} \) from the power-law model of lifetime. The NBTI lifetime of the power-law \( V_{\varepsilon} \) model is \( \tau = C V_{\varepsilon}^\beta \), which can be expressed in another form:

\[
\log \tau = \log C - \beta \log V_{\varepsilon} \tag{1}
\]

We use \( t \) (time) instead of \( \tau \) and both sides are multiplied by \( n \) (the parameter of the time model):

\[
\log t^n = \log C^n - \beta \log V_{\varepsilon}^n = \log( C_1 V_{\varepsilon}^{-\beta_1} ) \tag{2}
\]

Here \( C_1 \) is equal to \( C^n \), and \( \beta_1 \) is equal to \( n \beta \). From Eq. (2), we can get

\[
t^n = C_1 V_{\varepsilon}^{-\beta_1} \tag{3}
\]

\[
C_2 t^n = \Delta V_{th}^n V_{\varepsilon}^{-\beta_2} \tag{4}
\]

where \( \Delta V_{th}/C_2 \) is equal to \( C_1 \), \( \beta_2 \) is equal to \( \beta_1 \), and \( \Delta V_{th} \) is the lifetime definition of the devices. Therefore, taking no account of the time \( t \), we can get the \( \Delta V_{th} \) model dependent on \( V_{\varepsilon} \):

\[
\Delta V_{th} = C_3 V_{\varepsilon}^{\beta_3} \tag{5}
\]

Here \( C_3 \) and \( \beta_3 \) are constants.

Figure 7 shows that the power-law \( V_{\varepsilon} \) model for \( V_{th} \) shift agrees well with the experimental data. Figure 7 shows \( V_{th} \) shift at different times (a) and at different temperatures (b). All data fit well with the new deduced power-law \( V_{\varepsilon} \) model.

4 Conclusions

We examine NBTI degradations of 90nm devices in long term stresses under different conditions. Based on the results, we studied the models of the dependence of NBTI degradation of 90nm pMOSFETs on time, temperature, and stress \( V_{\varepsilon} \). The \( t \) model \( \Delta V_{th} = C t^n \) is also used, where \( n \) is similar to that of previous studies. \( \Delta V_{th} = C \times \exp \left( -E_a / K T \right) \) can be used as the \( T \) model of 90nm pMOSFET NBTI degradation. However, the activation energy is smaller. The conventional exponential model is not precise for predicting the

NBTI lifetime of 90nm pMOSFETs taking lower stress \( V_{\varepsilon} \) into account. We found a power-law \( V_{\varepsilon} \) model which is more predictive. Finally, the NBTI degradation model dependent on stress \( V_{\varepsilon} \) is deduced: \( \Delta V_{th} = CV_{\varepsilon}^\beta \). All data show that the models are good approximations.

References

**90nm pMOSFETs NBTI 退化模型及相关机理**

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摘要：对90nm pMOSFETs在不同温度及栅压应力下的NBTI效应进行了研究，从而提出了90nm pMOSFETs NBTI退化对时间、温度及栅压应力的模型。时间模型及温度模型与过去研究所提出的模型相似，但是关键参数有所改变。栅压应力模型遵循双对数关系，这与传统的单对数栅压应力模型不同。将较低的栅压应力也考虑在内时，双对数栅压应力模型较单对数栅压应力模型更为准确。

关键词：NBTI；90nm；pMOSFETs；模型

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