Models and Related Mechanisms of NBTI Degradation of 90nm pMOSFETs*

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Abstract: We investigate the negative bias temperature instability (NBTI) of 90nm pMOSFETs under various temperatures and stress gate voltages (V_g). We also study models of the time (t), temperature (T), and stress V_g dependence of 90nm pMOSFETs NBTI degradation. The time model and temperature model are similar to previous studies, with small difference in the key coefficients. A power-law model is found to hold for V_g, which is different from the conventional exponential V_g model. The new model is more predictive than the exponential model when taking lower stress V_g into account.

Key words: NBTI; 90nm; pMOSFETs; model
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1 Introduction

Negative bias temperature instability (NBTI) is an important effect in pMOSFETs. It didn't receive much attention for the larger devices of the past. However, as device sizes are continually scaling down without appropriate reduction of supply voltages, NBTI is getting more and more serious and has become one of the most important limiting factors of pMOSFET lifetime, especially for device sizes in the ultra-deep sub-micron region[1~3].

Many people have studied NBTI and obtained lots of results, which count for much. However, there is still no model that explains NBTI exactly. In most studies, NBTI is thought to be related to H species[4~6]. As its name NBTI implies, negative bias and temperature play the most important roles in the degradation of pMOSFETs. With the effects of electric field and temperature, SiH bonds break, and therefore generate interface states and oxide positive charges[4,7], which cause the degradation of parameters V_{th}, I_{dsat}, I_{dlin}, G_m and more. To model the effect of severe NBTI on the performance of a pMOSFET, it is important to treat the degradation as dependent on V_g and temperature. In addition, the time model, which has been studied for a long time, is also significant.

In this paper, we examine NBTI degradations of 90nm devices in long term stresses under different conditions, including various V_g and T. Based on the results, models dependent on t, T, and V_g are studied.

2 Devices and experiments

The pMOSFETs used here were fabricated in 90nm process technology with a lightly doped drain (LDD) structure and a shallow trench isolation (STI) scheme. The devices have a channel length of 90nm, width of 10μm, and gate oxide thickness of 1.4nm. The gate oxides of all devices were annealed in N_2O gas ambient after thermal growth. The operation voltage is 1.0V. An Agilent B1500A high precision semiconductor parameter analyzer was used to complete the tests. NBTI stress was applied to the gate electrode, with the source, drain, and substrate grounded at elevated

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temperatures. Stress testing combined with I-V measurement were performed at 90～150℃ in a dark box.

3 Results and discussion

Figure 1 shows the degradation of the transfer characteristics of the pMOSFETs. The pMOSFETs were stressed under $V_g = -1.8V$ at 90℃. After 10000s, the drain current appears clearly degraded, and the current in the saturation region is degraded more than that in the linear region. The threshold voltage V_{th} becomes larger than the former. From the inset in Fig. 1, we can see that G_m after 10000s decreases, and the peak point shifts left. This is due to the interface states and fixed oxide charges produced during NBTI stress. From the figure, we can see the serious degradation caused by NBTI clearly. This degradation will result in the final failure of the devices and affect the circuits badly. Therefore, it is important to study NBTI and to found models for key factors.

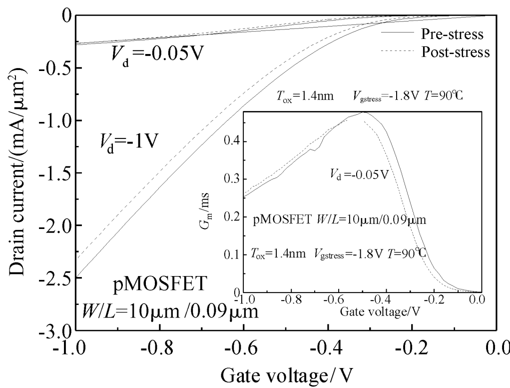


Fig. 1 Degradation of transfer characteristics of 90nm pMOSFETs pre- and post-NBTI stress with $V_g = -1.8V$ at 90℃ for 10000s

The shifts of the pMOSFET parameters with stress $V_g = -1.8V$ versus stress time are shown in Fig. 2. I_{dsat} shifts more than I_{dlin}, indicating that the interface states and oxide fixed charges produced during NBTI stress are located not in the overlap region but in the channel region. The degradation of the threshold voltage V_{th} is the most severe. We will study it to model the degradation caused by pivotal factors.

Figure 3 shows the relation of V_{th} degradation to time at different temperatures or under different stresses V_g. All data are plotted in a log-log scale. V_{th} shifts show excellent accordance to

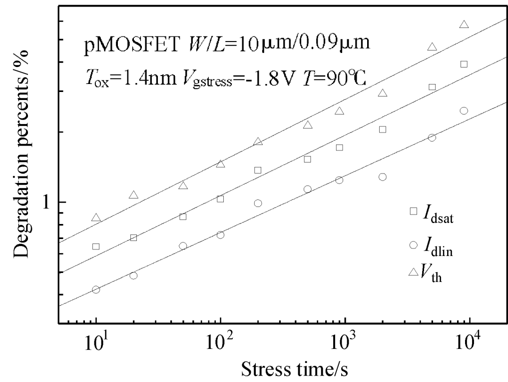


Fig. 2 Shifts of 90nm pMOSFET parameters with $V_g = -1.8V$ versus stress time

t^n. Though this time model was brought forward a long time ago, and has been confirmed by most studies, the parameter n is different for different devices manufactured by different technologies[5,8,9]. And when the device scale reaches 90nm, it is important to identify the t model. In Fig. 3 (a), at different temperatures, n shows a nearly constant value of 0.21, and in Fig. 3 (b), n decreases from 0.26 to 0.21, as the stress V_g increases. All of these results are similar to those of previous studies and show that the model $\Delta V_{th} = Ct^n$ can also account for NBTI degradation of 90nm pMOSFETs.

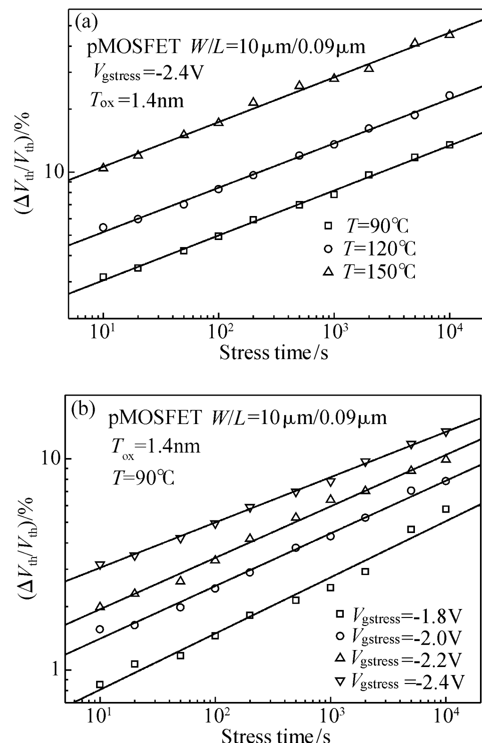


Fig.3 V_{th} shift versus stress time at different temperatures (a) or under different $V_{gstress}$ (b)

The shift of V_{th} versus temperature under different stresses V_g is plotted in Fig. 4 with a log-linear scale. All data under different stresses V_g are fitted with $\Delta V_{th} = C\exp(-E_a/KT)$, where E_a is the activation energy. The activation energy E_a of ΔV_{th} for each stress V_g is extracted from the data of Fig. 4. The results are shown in Fig. 5. E_a represents the difficulty of NBTI degradation. In Fig. 5, E_a decreases with increasing stress V_g, which implies that stress V_g plays an important role in NBTI degradation. The range of E_a in Fig. 5 is 0.11～0.13eV, which is smaller than that in previous studies, in which the device scale was larger[10]. From these results, we conclude that higher stress V_g and smaller device scale result in the easier occurrence of NBTI degradation. Therefore, we can also use $\Delta V_{th} = C\exp(-E_a/KT)$ as the T model of 90nm pMOSFET NBTI degradation. However, the activation energy is smaller.

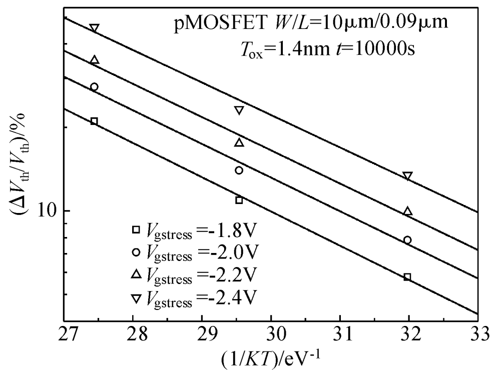


Fig. 4　V_{th} shift versus temperature under different $V_{gstress}$

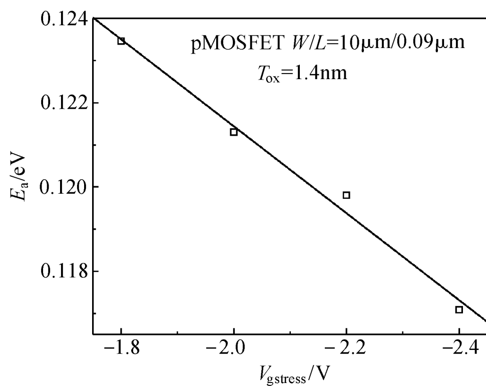
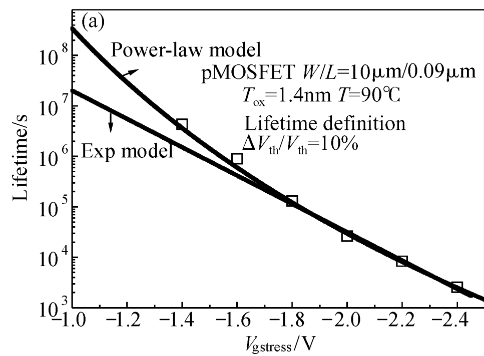


Fig. 5　Activation energy (E_a) of V_{th} shift versus $V_{gstress}$

From studies on NBTI with regard to time and temperature, we have known the importance of stress V_g. Accelerated testing is usually used to evaluate the lifetime of devices. A high gate voltage V_g is applied to a pMOSFET to measure its lifetime in NBTI studies. Some researchers have proposed a model of the dependence of lifetime (τ) on V_g to estimate the lifetime at operation voltages[2]. The conventional exponential model is $\tau = C\exp(-\beta V_g)$, where C and β are constants. From this lifetime model, we deduce that the model of ΔV_{th} is dependent on V_g as $\Delta V_{th} = C_1\exp(\beta_1 V_g)$, where C_1 and β_1 are also constants. Both of these models are used by manufacturers to estimate the V_{th} shift and lifetime of devices. In this paper, we take the 10% shift of V_{th} as the lifetime definition. The data gained under higher stress V_g agree well with both exponential models. However, when the stress V_g reaches a smaller value, but still higher than operation voltage, the exponential model departs from the experimental data, as shown in Fig. 6 (a). We change the log-linear scale into a log-log scale, and therefore



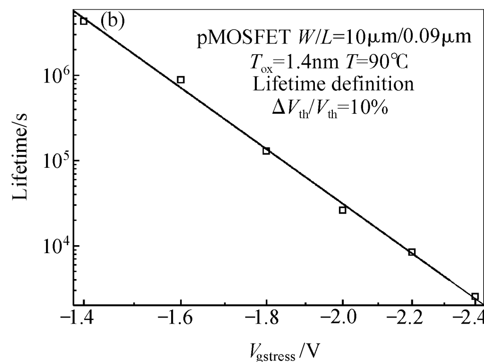


Fig. 6　(a) Comparison of exp model and power-law model; (b) Power-law model: $\tau = CV_g^{-\beta}$　All data fit well with power-law model.

make the exponential model into the power-law model $\tau = C\, V_g^{-\beta}$, where C and β are constants. For all data, lifetime under higher and lower stresses V_g, the power-law model is more predictive than the exponential model, as shown in Fig. 6 (b). Taking lower stress V_g into account, the exponential model underestimates the NBTI lifetime of 90nm pMOSFETs. Therefore, the power-law V_g model should be instead of the exponential model to predict the NBTI lifetime of ultra-deep sub-micron MOSFETs. We deduce the ΔV_{th} model dependent on V_g from the power-law model of lifetime. The NBTI lifetime of the power-law V_g model is $\tau = C\, V_g^{-\beta}$, which can be expressed in another form:

$$\lg\tau = \lg C - \beta \lg V_g \tag{1}$$

We use t (time) instead of τ, and both sides are multiplied by n (the parameter of the time model):

$$\lg t^n = \lg C^n - \lg V_g^{n\beta} = \lg(C_1\, V_g^{-\beta_1}) \tag{2}$$

Here C_1 is equal to C^n, and β_1 is equal to $n\beta$. From Eq. (2), we can get

$$t^n = C_1\, V_g^{-\beta_1} \tag{3}$$

$$C_2\, t^n = \Delta V_{th}\, V_g^{-\beta_2} \tag{4}$$

where $\Delta V_{th}/C_2$ is equal to C_1, β_2 is equal to β_1, and ΔV_{th} is the lifetime definition of the devices. Therefore, taking no account of the time t, we can get the ΔV_{th} model dependent on V_g:

$$\Delta V_{th} = C_0\, V_g^{\beta_0} \tag{5}$$

Here C_0 and β_0 are constants.

Figure 7 shows that the power-law V_g model for V_{th} shift agrees well with the experimental data. Figure 7 shows V_{th} shift at different times (a) and at different temperatures (b). All data fit well with the new deduced power-law V_g model.

4 Conclusions

We examine NBTI degradations of 90nm devices in long term stresses under different conditions. Based on the results, we studied the models of the dependence of NBTI degradation of 90nm pMOSFETs on time, temperature, and stress V_g. The t model $\Delta V_{th} = Ct^n$ is also used, where n is similar to that of previous studies. $\Delta V_{th} = C \times \exp(-E_a/KT)$ can be used as the T model of 90nm pMOSFET NBTI degradation. However, the activation energy is smaller. The conventional exponential model is not precise for predicting the NBTI lifetime of 90nm pMOSFETs taking lower stress V_g into account. We found a power-law V_g model which is more predictive. Finally, the NBTI degradation model dependent on stress V_g is deduced: $\Delta V_{th} = CV_g^{\beta}$. All data show that the models are good approximations.

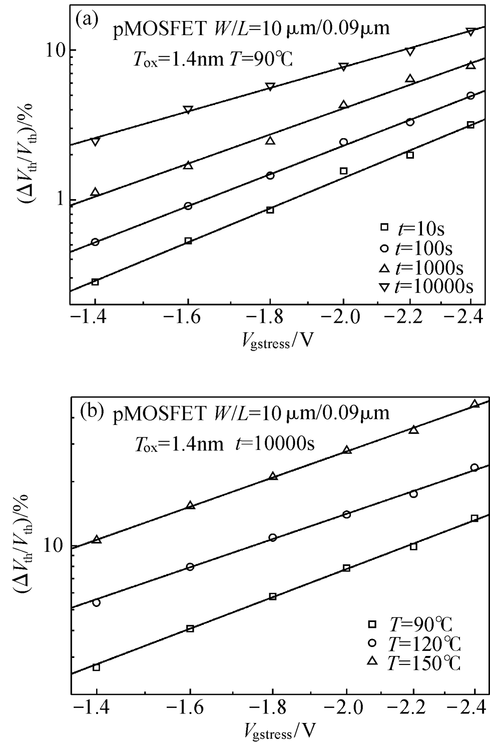


Fig. 7 Power-law V_g model for V_{th} shift: $\Delta V_{th} = C_0 V_g^{\beta_0}$ at different times (a) and at different temperatures (b) All data fit well with power-law V_g model.

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90nm pMOSFETs NBTI 退化模型及相关机理*

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摘要：对90nm pMOSFETs在不同温度及栅压应力下的NBTI效应进行了研究，从而提出了90nm pMOSFETs NBTI退化对时间 t、温度 T 及栅压应力 V_g 的模型.时间模型及温度模型与过去研究所提出的模型相似，但是关键参数有所改变.栅压应力模型遵循双对数关系，这与传统的单对数栅压应力模型不同.将较低的栅压应力也考虑在内时，双对数栅压应力模型较单对数栅压应力模型更为准确.

关键词：NBTI；90nm；pMOSFETs；模型

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