

Effect of Pt Addition on the Stress of NiSi Film Formed on Si (100)*

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Abstract: In order to clarify the effect of Pt addition on the stress of NiSi film, *in situ* stress measurements were taken to evaluate the stress evolution during heating and cooling treatment of Ni_{1-x}Pt_xSi alloy films with different Pt concentrations. The room temperature stress, which is mainly thermal stress, was measured to be 775MPa and 1.31GPa for pure NiSi and pure PtSi films grown on Si (100) substrates, respectively. For Ni_{1-x}Pt_xSi alloy film, the room temperature stress was observed to increase steadily with Pt concentration. From the temperature dependent stress evolution curves, the stress relaxation temperature was found to increase from 440°C (for pure NiSi film) to 620°C (for pure PtSi film) with increasing Pt concentration, thus influencing the residual stress at room temperature.

Key words: NiSi; Ni_{1-x}Pt_xSi; stress

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1 Introduction

Silicides have been widely used in VLSI circuits as source/drain contact materials for many years. The study of NiSi has drawn much attention since it is regarded as a substitute for CoSi₂ for 65nm CMOS and beyond. NiSi has many advantages, such as low resistivity, low thermal budget, and low ratio of Si consumption by Ni during formation. However, the transformation of NiSi into the high resistivity disilicide phase (NiSi₂) at temperatures over 750°C may be a problem^[1,2]. In recent years, it was verified that the phase thermal stability can be improved by adding small amount of Pt to the NiSi film^[2,3].

From the view of stress study, large stress induced by a silicide layer may generate dislocation loops in the Si substrate underneath, which are detrimental to device performance^[4~6]. To avoid this problem, it is important to keep a low stress level in the formed silicide film. As has been reported, NiSi has a lower stress building compared

to TiSi₂ and CoSi₂^[4]. However, when adding Pt to NiSi film, the stress performance may be changed.

In this work, the effect of added Pt on the stress performance of NiSi film will be presented for the first time. *In situ* stress measurements show that the room temperature stress of the formed NiSi film increases with Pt addition. This can be attributed to the increase of the stress relaxation temperature with Pt addition.

2 Experiment

n type Si(100) wafers were used in this work. The wafers, after standard RCA cleaning, were dipped in a dilute HF solution to remove residual surface oxide. After being dried, they were immediately loaded into the vacuum chamber of a magnetic sputtering system. The base pressure of the chamber was lower than 2.67×10^{-5} Pa. Ni and Pt were then deposited onto the wafer at a pressure of 0.67Pa in argon atmosphere.

Our samples are divided into three groups.

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Each group corresponds to one type of structure. The structures are Ni/Pt/Si, Pt/Ni/Si, and a Ni-Pt fully mixed metal layer on Si. For the Pt/Ni and Ni/Pt stacks, the thickness of the stack was kept at 50nm and different Pt sublayers of 1, 3, 5, 10, 20, 30, and 40nm in thickness were formed. 50nm thick samples of pure Ni and pure Pt were also prepared for comparison. The thickness was controlled by changing the deposition rate and time. For the third structure, Ni (49nm) and Pt (1nm) were simultaneously sputtered onto the silicon wafer to form a fully mixed Ni-Pt layer. The same was done for Ni (47nm) and Pt (3nm), and so on. This was done to ensure that the Pt percentages in each structure would be comparable.

The Pt atomic percentage is then calculated to be 1.4%, 4.3%, 7.2%, 14.9%, 31.8%, 51.2% and 73.6%, respectively for the different samples with added Pt layers, assuming the atomic density is $6.622 \times 10^{22} \text{cm}^{-3}$ for Ni and $9.14 \times 10^{22} \text{cm}^{-3}$ for Pt^[7].

The samples were then loaded into the heating chamber for *in situ* stress measurement. The ramping rate was controlled to be 3°C/s. When the temperature reached 700°C, the sample was immediately cooled down to room temperature at 6°C/s. Helium gas flow was used to prevent oxidation of the sample during the heat treatment. At the same time, two parallel laser beams were reflected onto the sample's surface. Reflected beams were collected by a position-sensitive CCD camera. Historical positions of the beams were recorded to calculate the surface curvature evolution.

The film stress is assumed to be isotropic in the film plane and can be calculated from the surface curvature by Stoney's equation,^[8]

$$\sigma_f = \frac{1}{6R} \times \left(\frac{E_s}{1 - \nu_s} \right) \times \frac{t_s^2}{t_f} \quad (1)$$

where σ_f is the film stress, E_s is the Young's modulus of the substrate, ν_s is the Poisson's ratio of the substrate, t_s and t_f are the thicknesses of the substrate and the film, respectively, and R is the net change in the radius of curvature, which has been measured *in situ* in our experiments.

3 Results and discussion

During the heating process, Ni reacts with Si to form NiSi, and Pt reacts with Si to form PtSi.

PtSi is completely miscible with NiSi because of the crystal lattice similarity (both NiSi and PtSi are of orthorhombic MnP structure)^[2,3]. Thus in our experiment, a layer of $\text{Ni}_{1-x}\text{Pt}_x\text{Si}$ alloy will form at 700°C, regardless of the initial structure. The thickness ratio from metal to silicide ($t_{\text{sil}}/t_{\text{M}}$) is 2.01 for NiSi formed from a Ni layer. The ratio for PtSi film formed from Pt is 1.98. As we consider the lattice of $\text{Ni}_{1-x}\text{Pt}_x\text{Si}$ alloy, Vegard's law indicates that when Ni-Pt reacts with Si to form silicide alloy, the thickness increase ratio $t_{\text{sil}}/t_{\text{M}}$ should be between 2.01 and 1.98. Nevertheless, both 2.01 and 1.98 are so close to 2.00 that we may simply take 2.00 as a general thickness increase ratio for $\text{Ni}_{1-x}\text{Pt}_x\text{Si}$ alloy, disregarding the different Pt concentrations. According to this assumption, the silicide films formed in our samples have nearly the same thickness of 100nm.

According to sheet resistance measurements, the pure NiSi film has a sheet resistance of $1.36 \Omega/\square$, corresponding to $13.6 \mu\Omega \text{cm}$ in resistivity. For the pure PtSi film, the resistivity is about $42.7 \mu\Omega \text{cm}$. Before annealing, samples of different structures show different sheet resistance. The fully mixed Ni-Pt samples obviously have higher resistance due to the enhanced carrier scattering of the metallic films. However, after annealing, curves of sheet resistance plotted versus Pt thickness percentage for different initial structures more closely resemble each other (Fig. 1). Regardless of whether the Pt is used as interlayer or cap layer or is fully mixed with Ni, the sheet resistance of the formed silicide alloy film increases steadily with Pt concentration. For instance,

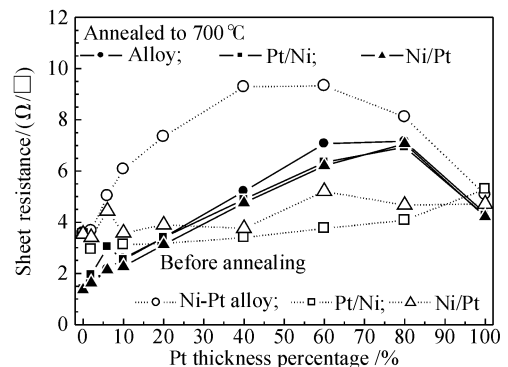


Fig.1 Sheet resistances of the samples before and after 700°C *in situ* annealing versus Pt thickness percentage

when adding a 10nm layer of Pt to a 40nm layer of Ni, the sheet resistance of the formed silicide increased from $1.36\Omega/\square$ (for pure NiSi film) to around $3.31\Omega/\square$.

Three sources of stress can be considered for silicide film; intrinsic stress, thermal stress, and epitaxial stress. Epitaxial stress is only possible in the case of epitaxial growth and is thus not applicable in our case. The intrinsic stress is the part of the film stress that is built during the film deposition or film growth. When a metal film reacts with a Si substrate, the moving species, metal atoms or silicon atoms, change the local volume greatly, resulting in increasing intrinsic stress. When the silicidation is finished, stress relaxation takes place because of the high temperature. The enhanced atom mobility is helpful for silicide grain growth. The rearrangement of atoms makes the stress relaxation possible.

During the cooling process, the difference in thermal expansion of the silicide and the Si substrate caused the thermal stress. The thermal stress can be expressed as^[4]

$$\sigma = (T - T_0) \left[-(\alpha_{\text{sil}} - \alpha_{\text{Si}}) \left(\frac{E}{1 - \nu} \right)_{\text{sil}} \right] \quad (2)$$

where α_{sil} and α_{Si} are the thermal expansion coefficients of the silicide film and the Si substrate, respectively, and T_0 is the stress relaxation temperature at which the stress of the film is fully relaxed. The thermal expansion coefficient is usually larger for silicide than for Si (Si: $2.6 \times 10^{-6} \text{ K}^{-1}$, CoSi_2 : $10.4 \times 10^{-6} \text{ K}^{-1}$, NiSi: $16 \times 10^{-6} \text{ K}^{-1}$)^[4]. Thus, a strong tensile thermal stress builds up during cooling and will dominate the film stress at room temperature.

Figures 2~4 show the film stress evolution during the heating and cooling processes. The samples shown in each figure have the same structure, i. e., Pt is used as interlayer or capping layer or is fully mixed with Ni. For simplicity, a universal film thickness of 100nm is used to calculate the stress of silicide as well as metal by Eq. (1). This is correct for the cooling parts of the stress curves, but not correct for the heating parts, especially before the final silicide phases have been completely formed. Therefore, in the heating parts, the actual stress should lie between one and two times the value plotted in Figs. 2~4.

Some work has been done on the intrinsic stress evolution of Ni film on Si substrate or Pt

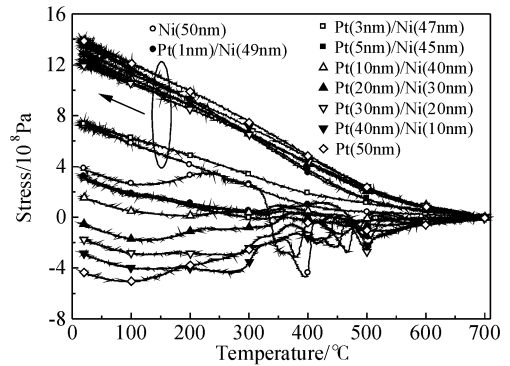


Fig. 2 *In situ* stress measurement of Pt/Ni stack films on Si (100) substrates. The ramping rate is 3°C/s and the cooling rate is 6°C/s .

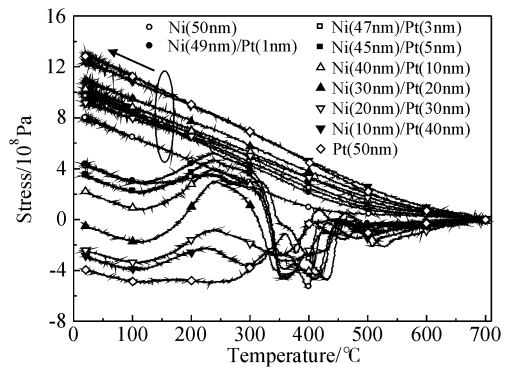


Fig. 3 *In situ* stress measurement of Ni/Pt stack films on Si (100) substrates. The ramping rate is 3°C/s and the cooling rate is 6°C/s .

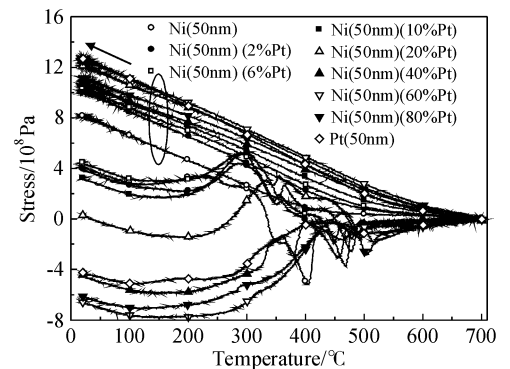


Fig. 4 *In situ* stress measurement of Ni-Pt alloy films on Si (100) substrates. The ramping rate is 3°C/s and the cooling rate is 6°C/s . Percentages of Pt of the alloy samples are given in terms of thickness.

film on Si substrate during annealing^[4,9,10]. Generally speaking, the intrinsic stress is very complicated. The study of intrinsic stress is beyond the scope of this work. We pay more attention to the stress building up during the cooling stage as well as the final stress at room temperature since most

devices that use silicide films work at room temperature.

As we checked the performance of pure NiSi and pure PtSi shown in Figs. 2 ~ 4, the room temperature stress values were found to be 721, 798, and 816MPa for NiSi films (775MPa on average) and 1.39, 1.28, and 1.27GPa for PtSi films (1.31GPa on average). These data are in agreement with the previously reported values of 720MPa for NiSi^[4] and 1.5GPa for PtSi^[10] on Si (100) substrates.

The difference between the values, for instance, 1.39, 1.28, and 1.27GPa stress for PtSi film in our measurement, indicates a large error bar. The fluctuation can be explained by the non-ideal flatness of the wafer used in the test. The non-ideal flatness of the wafer (when the stress is zero) can be regarded as many local curvatures existing inside the surface. The local curvatures will inevitably be incorporated into the measurement of the global curvature of the wafer because the latter is actually measured from the very two spots of the surface where the laser beams are reflected. Further experimental verification shows that the error of the final room temperature stress measurement related to the non-ideal flatness of the substrate can be as large as 80MPa.

For all of the silicide films in our study, the stress evolution during the cooling stage exhibits a linear building up behavior as the temperature is decreased, as shown in Figs. 2 ~ 4. The linear building up behavior of the tensile stress has been observed in many silicide films grown on Si substrates, such as CoSi₂ and TiSi₂, and the increasing tensile stress during cooling is mainly the thermal stress^[11,12]. As explained by Eq. (2), the tensile thermal stress is caused by the difference of the thermal expansion coefficients between the silicide and the Si substrate. The stress relaxation temperature of the silicide film, together with the difference in the thermal expansion coefficients of the silicide film and the Si substrate determines the final stress at room temperature.

The stress relaxation temperature can be determined by fitting the cooling part of each stress curve with Eq. (2). The intersection of the fitting line with zero stress is defined to be the point where the stress in the films is zero. The corresponding temperature is then defined as the stress

relaxation temperature T_0 . The determined stress relaxation temperatures are plotted in Fig. 5. As can be seen, Pt addition increases T_0 of the formed silicide film from 440°C (for pure NiSi film) to 620°C (for pure PtSi film), thus influencing the final film stress at room temperature.

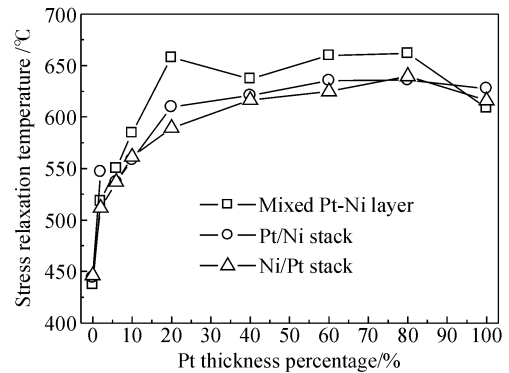


Fig. 5 Stress relaxation temperature of Ni_{1-x}Pt_xSi alloy films annealed from Pt/Ni, Ni/Pt stacks or mixed Pt-Ni layers on Si (100) substrates versus Pt percentage in thickness

In each structure group, the pure PtSi film exhibits the highest room temperature film stress and the pure NiSi film has the lowest room temperature stress. The cooling parts of the stress curves for Ni_{1-x}Pt_xSi alloy films are distributed between the two for pure NiSi and pure PtSi. The room temperature stress values are plotted versus Pt thickness percentage in Fig. 6. Each curve stands for one structure group. Although the residual stress at room temperature does not change monotonically with increasing Pt percentage due to the large measurement error as discussed above, there is a clear trend by which Pt addition increases the room temperature tensile stress in the formed Ni_{1-x}Pt_xSi alloy film.

4 Conclusion

The effect of added Pt on the film stress evolution of Ni_{1-x}Pt_xSi film is studied by *in situ* stress measurement. The room temperature stress, which is mainly thermal stress, is measured to be 775MPa for pure NiSi film and 1.31GPa for pure PtSi film. Both films are grown on Si (100) substrates. When Pt is added to Ni, the room temperature stress of the formed Ni_{1-x}Pt_xSi alloy film

increases steadily with Pt concentration, as does the stress relaxation temperature, which increases from 440°C (for pure NiSi film) to 620°C (for pure PtSi film).

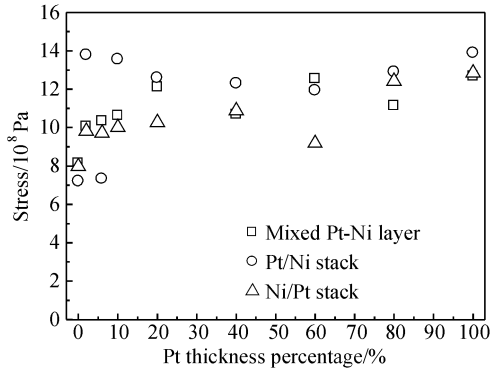


Fig.6 Residual stresses at room temperature (20°C) for $Ni_{1-x}Pt_xSi$ alloy films annealed from Pt/Ni stacks, Ni/Pt stacks, and mixed Pt-Ni layers on Si (100) substrates versus Pt percentage in thickness

References

- [1] Xu D X, Das S R, Peters C J, et al. Material aspects of nickel silicide for ULSI applications. *Thin Solid Films*, 1998, 326: 143
- [2] Lauwers A, Kittle J A, Van Dal M J H, et al. Ni based silicides for 45nm CMOS and beyond. *Mater Sci Eng B*, 2004, 114/115:29
- [3] Mangelinck D, Dai J Y, Pan J S, et al. Enhancement of thermal stability of NiSi films on (100) Si and (111) Si by Pt addition. *Appl Phys Lett*, 1999, 75:1736
- [4] Steegen A, Maex K. Silicide-induced stress in Si; origin and consequences for MOS technologies. *Mater Sci Eng R*, 2002, 38:1
- [5] Steegen A, Maex K, De Wolf I. Local mechanical stress induced defects for Ti and Co/Ti silicidation in sub-0.25 μ m MOS-technologies. *Symp VLSI Tech*, 1998:200
- [6] Steegen A, Stucchi M, Lauwers A, et al. Silicide induced pattern density and orientation dependent transconductance in MOS transistors. *IEDM Technical Digest*, 1999:497
- [7] Maex K, Van Rossum M. Properties of metal silicides. London: INSPEC, 1995
- [8] Milton O. The materials science of thin films. San Diego: Academic Press, 1992
- [9] Rivero C, Gergaud P, Thomas O, et al. *In situ* study of stress evolution during the reaction of a nickel film with a silicon substrate. *Microelectron Eng*, 2004, 76:318
- [10] Pan J T, Blech I A. *In situ* study of film stress and kinetics of platinum silicide formation on Si. *Thin Solid Films*, 1984, 113:129
- [11] D'Heurle F M, Thomas O. Stresses during silicides formation: a review. *Defect Diffusion Forum*, 1996, 129/130:137
- [12] Pan J T, Blech I A. *In situ* stress measurement of refractory metal silicides during sintering. *J Appl Phys*, 1984, 55:2874

掺 Pt 对 Si(100) 上形成的 NiSi 薄膜应力的影响*

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摘要: 利用在线应力测试技术表征了掺入 Pt 后对镍硅化物薄膜应力性质的影响. 通过改变 NiSi 薄膜中 Pt 含量以及控制热处理的升温、降温速率实时测量了薄膜应力, 发现在 Si(100) 衬底上生长的纯 NiSi 薄膜和纯 PtSi 薄膜的室温应力主要是热应力, 且分别为 775MPa 和 1.31GPa, 而对于 $Ni_{1-x}Pt_xSi$ 合金硅化物薄膜, 室温应力则随着 Pt 含量的增加而逐渐增大. 应力随温度变化曲线的分析表明, $Ni_{1-x}Pt_xSi$ 合金硅化物薄膜的应力弛豫温度随 Pt 含量的增加, 从 440°C (纯 NiSi 薄膜) 升高到 620°C (纯 PtSi 薄膜). 应力弛豫温度的变化影响了最终室温时的应力值.

关键词: 硅化镍; 镍铂硅化物; 应力

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