Chip Design of Li-Ion Battery Charger Operating in Constant-Current/Constant-Voltage Modes

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Abstract: A design for a Li-ion battery charger IC that can operate in a constant current-constant voltage (CC-CV) charge mode is proposed. In the CC-CV charge mode, the charger IC provides a constant charging current at the beginning, and then the charging current begins to decrease before the battery voltage reaches its final value. After the battery voltage reaches its final value and remains constant, the charging current is further reduced. This approach prevents charging the battery with full current near its saturated voltage, which can cause heating. The novel design of the core of the charger IC realizes the proposed CC-CV charge mode. The chip was implemented in a CSMC 0.6μm CMOS mixed signal process. The experimental results verify the realization of the proposed CC-CV charge mode. The voltage of the battery after charging is 4.1833V.

Key words: Li-ion battery charger; constant current-constant voltage charge modes; CMOS analog circuit
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1 Introduction

Lithium-ion batteries have become the most widely used rechargeable batteries due to their many advantages. Research on charge management circuits is meaningful for practical use. The Li-ion battery charger IC developed in several phases. In order to avoid the overheating of batteries during the charging process, the earliest charger IC only supplied a constant but small charging current, and was terminated manually. It required a long time to complete a charge cycle. Moreover, manual termination lowers the reliability, because it may result in inefficient charge or overcharge. Cope *et al*.[1] proposed a charging approach that uses a constant, large charging current to shorten the charge time. However, a large charging current not only makes a battery susceptible to overcharge, but may also overdrive the available chemical reactions in the battery, resulting in heating and finally reducing the capacity and cycle life of the battery.

The charge method with constant current-constant voltage (CC-CV) modes[2,3] has been employed as an improvement over the constant current approach. Under this arrangement, a constant current is applied until the battery voltage rises to a predetermined value, i.e., the saturated voltage, and then the charge current gradually decreases while the battery voltage remains constant. When the current reaches a minimum value, the charge cycle is complete. This approach is more precise than the constant current approach. The characteristic graph of the CC-CV approach is illustrated in Fig. 1(a). Nevertheless, this approach also has disadvantages. When the battery voltage is near its saturated value, the quantity of materials available for chemical reactions inside the battery is low. If a large charging current is still supplied to the battery, the fast charge may cause the reaction rate to exceed that allowed by the concentration of the reactants. This will result in over-heating of the battery.

To solve this problem, we propose an improved CC-CV charge method. In this method, the charging current begins to decrease before the battery voltage reaches its final value, as illustrated in Fig. 1(b). After the battery voltage reaches its final value and remains stable, the charging current is further reduced. The charging current begins to decrease around 4.1V when there is sufficient reactant. Thus, overheating of the battery caused by the chemical reaction rate exceeding

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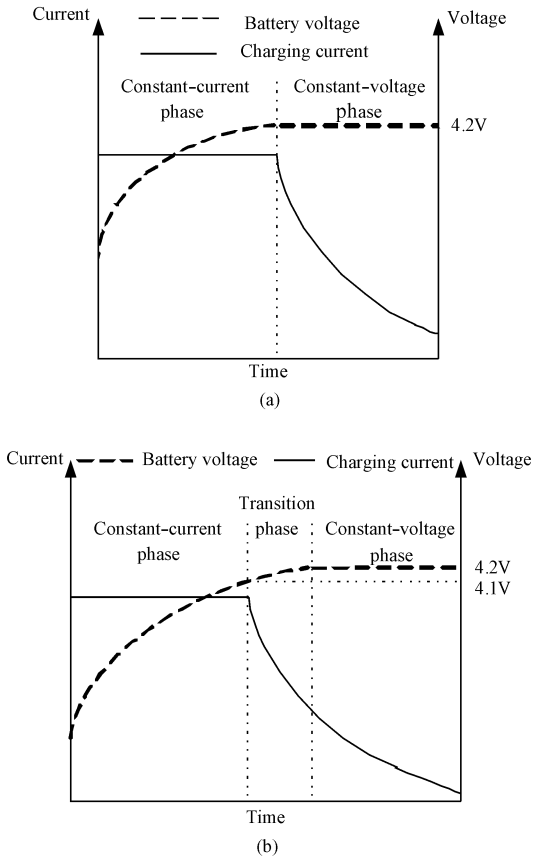

Fig. 1　Characteristic graphs of the traditional CC-CV approach (a) and the improved CC-CV approach (b)

that allowed by the reactant concentration can be avoided. As a result, this improved CC-CV method is much more secure and reliable than the traditional method. While rudimentary charge methods based on the CC-CV approach have already been introduced[2,3], no concrete circuit using a CMOS process has yet been reported.

In this paper, we focus on realizing the improved CC-CV approach using a CMOS process. The chip was implemented in a CSMC 0.6μm CMOS mixed signal process. The experimental results verify the function of the charger IC.

2　Circuit design

2.1　System structure

The system of the Li-ion battery charger circuit is shown in Fig. 2, which includes the charger IC in the dashed block, as well as a Li-ion battery and an external resistor R_{MON} to program the charging current. In the dashed block, a pair of pMOS transistors M0 and M1 form a current mirror, and M1 provides the charging current. The priority module chooses a higher output voltage from the CC-CV control module and the temperature control module to control the current mirror. The priority module can be simply implemented with diodes. The CC-CV control module carries out the constant current phase, the transition phase, and the constant voltage phase, as shown in

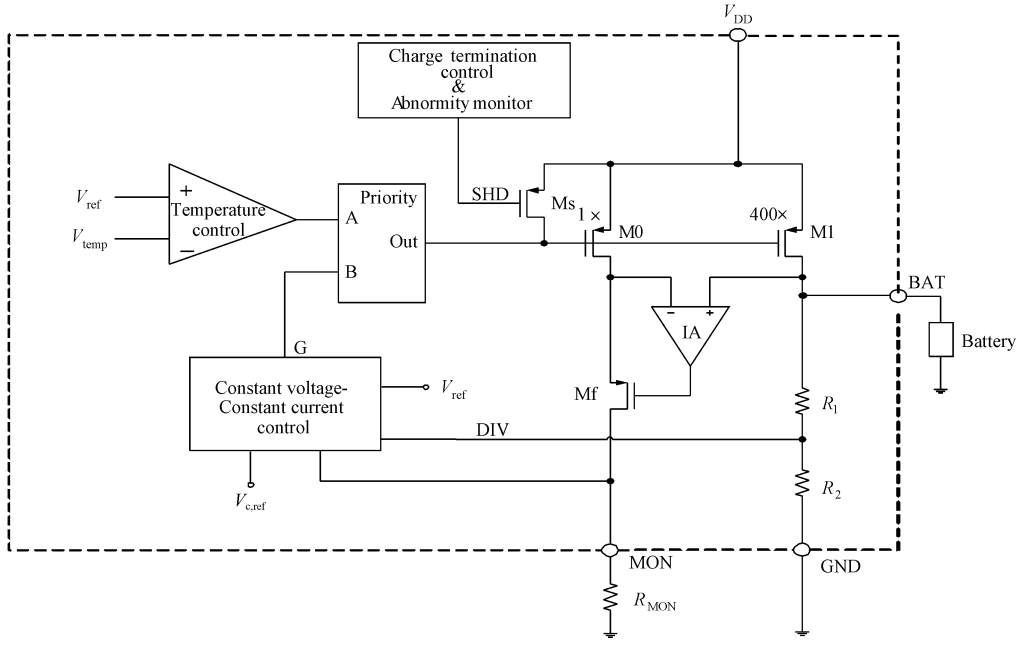

Fig. 2　Block diagram of Li-ion battery charger circuit

Fig. 1 (b). The temperature control module prevents the temperature from exceeding the safety limit of 120℃ by reducing the charging current. Only at high temperatures will the output voltage of the temperature control module exceed the CC-CV control module. The W/L ratio of M1 and M0 is 400 : 1. The op-amp, IA, makes the V_{DS} of M0 and M1 identical, which guarantees that the branch current in M1, $I_{ds,M1}$, is precisely 400 times that in M0, $I_{ds,M0}$. On the other hand, since the current in R_1 and R_2 can be neglected when compared to the current flowing into the battery, it can be assumed that the charging current is approximately equal to the branch current in M1. Thus, the charging current can be monitored through the external resistor R_{MON}. Neglecting the current in R_1 and R_2, the relationship between the charging current I_{BAT} and the current through R_{MON} satisfies the following equation:

$$I_{BAT} = 400 \times \frac{V_{MON}}{R_{MON}} \quad (1)$$

In the constant voltage phase, once the charging current is reduced to 1/10 of its maximum value, i. e., the charging current at the constant current phase, the charge termination control circuit sends the signal SHD to turn on the switch Ms, pulling up the gate voltage of M0, M1 to V_{DD} and terminating the charge cycle. Then, the charger IC enters the standby mode. When the battery voltage descends to 4.05V, the charger IC begins to recharge. The abnormity monitor circuit shuts down the current mirror via the signal SHD, too, if the power supply voltage is lower than 3.6V or the temperature is higher than 120℃. When the application circumstance comes out of the abnormal situation, the charge cycle restarts.

2.2 Module of the proposed CC-CV control circuit

The scheme of the improved CC-CV control circuit is shown in Fig. 3. Node G is the output of this module. When the battery voltage is lower than 4.1V, VC has no output current, i.e. $I_{ovc} = 0$. VC is not effective in the feedback loop. The preamplifier CF, the pull-up pMOS transistor Mp, and the current source I_0 constitute the amplifier for constant current control. $V_{c,ref}$ equals 0.1V when the battery voltage V_{BAT} is lower than 2.9V, and 1V otherwise. Due to the amplifier for constant current control, under the constant current phase, $V_{MON} = V_{c,ref}$. Since V_{MON} and the charging current I_{BAT} satisfy Eq. (1), the maximum charging current can be programmed via R_{MON}.

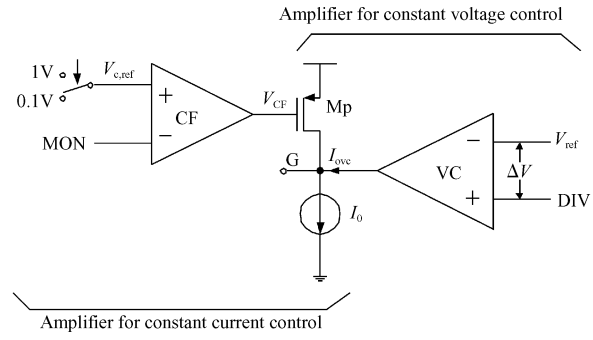

Fig. 3 Schematic of the improved CC-CV control module

When the battery voltage is in the range of 4.1～4.2V, the charge cycle enters the transition phase as shown in Fig. 1 (b). At this phase, VC works as a transconductance amplifier, and thus $I_{ovc} = G_m \Delta V$, where G_m is the transconductance of VC. The amplifier for constant current control and its feedback network are shown in Fig. 4. As a result of the non-zero output current I_{ovc}, the amplifier for constant current control plus its feedback network will change V_{CF}, the gate voltage of the pMOS transistor Mp, and thus adjust the operation points. Meanwhile, as shown in Fig. 1(b), in the transition phase, the charging current I_{BAT} decreases. Since I_{BAT} and V_{MON} satisfy Eq. (1), V_{MON} also decreases observably in the transition phase. To realize the function in the transition

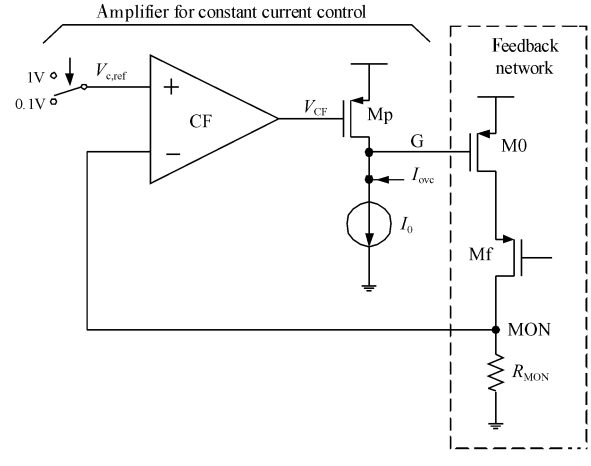

Fig. 4 Amplifier for constant current control and its feedback network ($I_{ovc} = 0$ in the constant current phase and $I_{ovc} \neq 0$ in the transition phase)

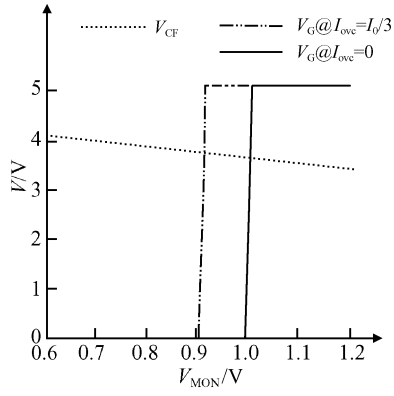

Fig. 5　DC characteristics graph of the amplifier for constant current control

phase, the gain of the pre-amplifier CF must be on the order of 10^0. The DC characteristics graph of the amplifier for constant current control is illustrated in Fig. 5. As seen in Fig. 5, due to the small gain of CF, the offset voltage of the amplifier for constant current control changes notably as V_{CF} changes. This is the basic principle underlying the transition phase. For the same reason, in the constant current phase, V_{MON} approximates $V_{c,ref}$ with an error. However, this error is insignificant to the charger IC and the battery.

When the battery voltage reaches 4.2V, the output current of VC fits the current source I_0 in Fig. 3, with no current flowing out from Mp. CF and Mp are not effective in the feedback loop. VC and the pull down current source I_0 form the amplifier for constant voltage control, which realizes the constant voltage phase. The amplifier for constant voltage control and its feedback network are redrawn in Fig. 6.

Figures 7 (a) and (b) are the schematics of CF and VC, respectively. As shown in Fig. 7(a),

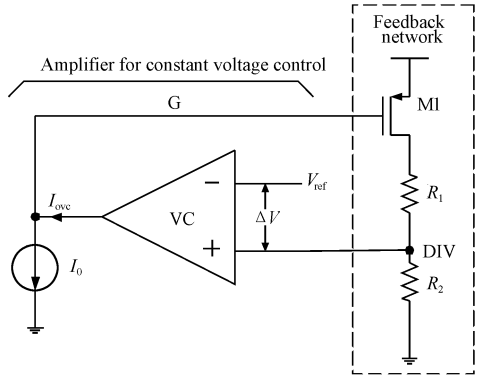

Fig. 6　Amplifier for constant voltage control and its feedback network

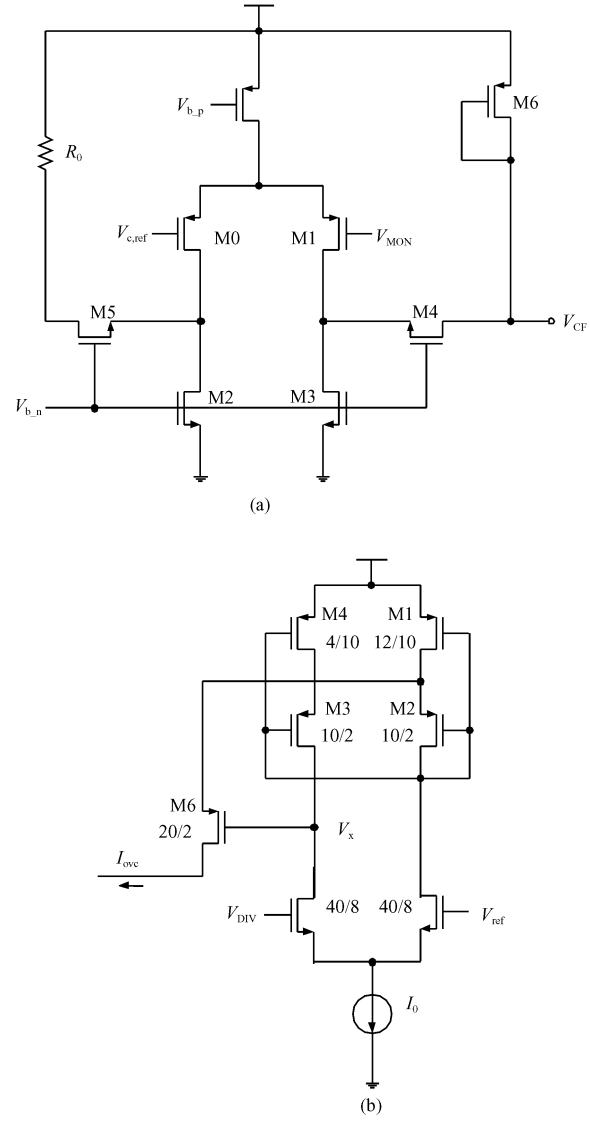

Fig. 7　(a) Schematic of CF; (b) Schematic of VC

CF is a two-stage amplifier. In the differential stage, M2 and M3 work in the triode region, since $V_{GD,M2,3} = V_{GS,M4,5} > V_{th,n}$. In order to lower the gain, the second stage uses a common gate circuit, both the input impedance and the gain of which are small. The low output impedance of the first stage and the low input impedance of the second stage make the gain of the differential stage small. On the other hand, the second stage is in fact an amplifier with a single input and a single output. Thus, the gain of the second stage is approximately $(g_{m4} + g_{mb4} + g_{ds4})/(g_{m6} + g_{ds6} + g_{ds4})$. In this way, the gain of CF can be made on the order of 10^0.

The design of VC employs the structure shown in Fig. 7 (b). The tail current in Fig. 7(b)

is the same as the pull down current source I_0 in Fig. 3. The mechanism of VC is explained as follows. When V_{DIV} is relatively small, M6 turns off. At this time, VC is similar to a regular differential pair circuit. Due to the asymmetry design of M1 and M4, V_x will drop promptly when V_{DIV} reaches V_a, some level lower than V_{ref}. Concurrently, M6 is turned on and the output current I_{ovc} begins to flow out. Meanwhile, I_{ovc} increases while V_{DIV} increases. As V_{DIV} rises to V_{ref}, that the currents satisfy $I_{M2} = I_{M3} = \frac{1}{2} I_0$, $I_{M4} = \frac{1}{3} I_{M1}$, $I_{ovc} = I_{M6} = 2I_{M2} = 2I_{M3} = I_0$. Thus it can be seen that when $V_{DIV} = V_{ref}$, the outflow current I_{ovc} happens to fit the pull down current source I_0 in Fig. 3. Simultaneously, the pMOS transistor Mp in Fig. 3 is turned off; VC, including the current source I_0, constitutes the amplifier for constant voltage control. The amplifier for constant voltage control and its feedback network keep V_{DIV} equal to V_{ref}. Thus the constant voltage phase is achieved. In the constant voltage phase, V_G gradually rises, with the result that the charging current shrinks as well. Once the charging current is reduced to 1/10 of its maximum value, the charge termination control circuit sends the signal SHD to turn on the switch Ms, pulling up the gate voltage of M0, M1 to V_{DD} and terminating the charge cycle. In the design of V_C, the level of V_a is determined by the W/L ratio of M1 and M4. As this ratio is adjusted, the size of M6, as well as the tail current in VC, should be synchronously adjusted, so that when $V_{DIV} = V_{ref}$, the output current I_{ovc} of VC happens to fit the pull down current source I_0 in Fig. 3.

It can be seen from the analysis above that after a charge cycle is completed, the battery voltage is

$$V_{BAT} = \frac{R_1 + R_2}{R_2} V_{ref} \tag{2}$$

In order to achieve precise V_{BAT} after charging, the bandgap reference circuit that produces V_{ref} needs to be tuned to an accurate level.

3 Experimental results

The charger IC proposed was implemented in a CSMC 0.6μm CMOS mixed signal process. A photograph of the chip is shown in Fig. 8. The part surrounded by the solid line is the improved CC-CV control module corresponding to Fig. 3.

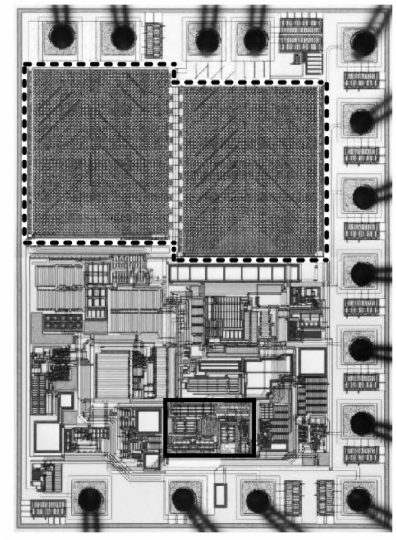

Fig. 8 Photograph of the charger IC

The part in the dashed frame is the implementation of the current mirror M0 and M1 in Fig. 2. M0 and M1 take half the area of the whole chip, for M1 must be large enough to provide a current of several hundred milliamperes. The layout of M0 and M1 is shown in Fig. 9. The layout design of M0 and M1 is simple and requires no via. Moreover, it is also the best way to save chip area.

The testing circuit is shown in Fig. 10. A 1kΩ resistor is selected as R_{MON}, while a Li-ion battery is employed to verify the function of the chip. The initial battery voltage before charging is 3V. The measured charging characteristics graph is shown in Fig. 11. The measured result proves that the proposed CC-CV control circuit is capable of realizing the improved charging approach illustrated in Fig. 1 (b). As seen in Fig. 11, the charging current begins to descend when the battery voltage V_{BAT} reaches 4.06V. V_{BAT} finally remains constant at

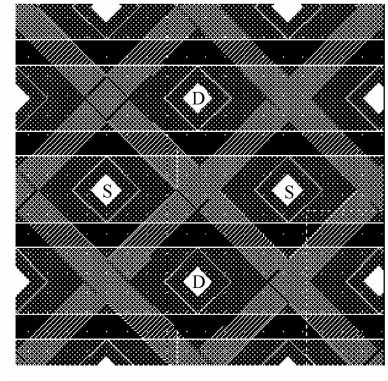

Fig. 9 Layout of M0 and M1

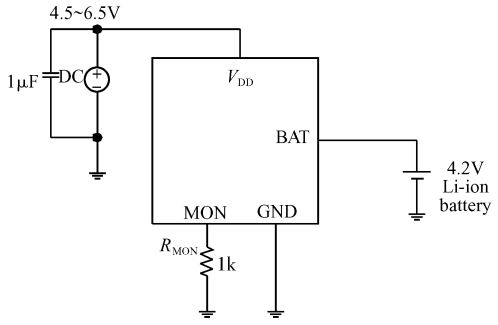

Fig. 10　Testing circuit

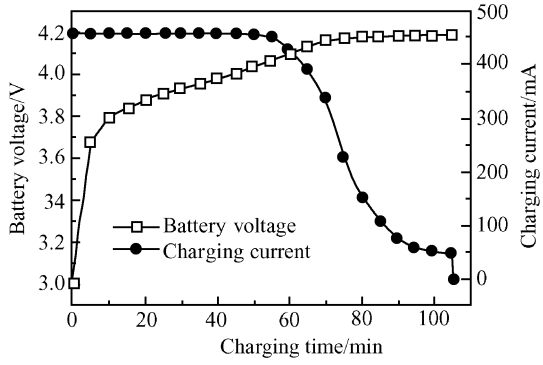

Fig. 11　Measured battery voltage and charging current as a function of charging time

4.1833V. At the constant current phase, V_{MON} is measured to be 1.143V. It can be predicted from Eq.(2) that the maximum charging current supplied to the battery is 457mA, which agrees with the measured result. This implies that the branch current in R_{MON} and the charging current I_{BAT} have an accurate proportion of 1∶400. As a result, in the application of this charger IC, the charging current can be monitored via the voltage at the port MON. In the constant voltage phase, the charge cycle terminates when the charging current is reduced to 45mA.

The battery temperature in the constant current phase is around 25℃. Moreover, during the transition phase and the constant voltage phase, the battery temperature is no more than 40℃.

4　Conclusion

An improved CC-CV charging approach that is more secure and reliable than the traditional method has been proposed and realized via the novel design of the core of the charger IC. The chip was implemented in a CSMC 0.6μm 2p2m CMOS mixed signal process. The experimental results verify the realization of the improved CC-CV charge mode. The voltage of the battery after charging is 4.1833V.

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恒流/恒压充电方式的锂电池充电器芯片

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摘要：提出了一种基于恒流-恒压(CC-CV)充电模式的锂电池充电器.在 CC-CV 充电模式下，充电器先给电池提供大的充电电流；在电池电压尚未到达饱和之前，充电电流便开始减小；电池电压达到饱和并保持恒定之后，充电电流进一步减小.这种充电方法，能够避免在电池电压的饱和值附近仍对电池进行大电流充电，从而导致过热现象.对这块充电器芯片核心电路的创新设计，保证了这种 CC-CV 充电模式的实现.本芯片采用 CSMC 公司 0.6μm 的 CMOS 工艺流片.测试结果验证了本文提出的 CC-CV 充电模式的实现.充电完成后，锂电池电压为 4.1833V.

关键词：锂电池充电器；恒流-恒压充电模式；CMOS 模拟电路

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