Storage Characteristics of Nano-Crystal Si Devices Using Different Measurements for MOS Capacitors*

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Abstract: The storage characteristics of nano-crystal Si (NC-Si) devices, especially for MOS capacitors, are studied by cross sectional transmission electron microscopy (TEM) and capacitance-voltage (*C-V*) measurement under different conditions, including programming and erasing at different temperatures and gate voltages, as well as using + / − bias-temperature (BT) measurements. Physical mechanisms such as carrier trapping, interface state filling, and temperature related deterioration are revealed. The experimental results demonstrate that the degradation of the program window and threshold voltage (V_T) shift at high temperature, large voltage sweep range, and bias applied to sweep voltage is strongly related to the type of majority carriers.

Key words: nano-crystal; storage; measurement
PACC: 7125; 7300
CLC number: TN4 **Document code**: A **Article ID**: 0253-4177(2007)08-1169-04

1 Introduction

Flash memory is the most widely used non-volatile memory because of its high density, low manufacturing cost, stable operation, etc. However, the scaling-down of flash memory cell sizes has become more difficult, because the tunneling oxide thickness cannot be scaled down with device size due to the difficulties of keeping the excellent charge retention and endurance characteristics. In order to solve this problem, new non-volatile memories such as nano-crystal non-volatile memory (NCNVM), a novel kind of flash memory in which the floating gate is fabricated by a Si dot-embedded oxide layer[1], have been studied extensively due to their high density and retention characteristics[2~4]. Carriers are programmed or erased by changing gate voltage using F-N or direct tunneling. Non-volatile characteristics are improved by a discrete storage mechanism. NC-Si memory has high storage density, low consumption, and fair retention characteristics. However, it is still necessary to improve NCNVM's storage characteristics. Experiments on MOS capacitors can reveal basic storage characteristics of NC-NVM and have been performed by many researchers, as well as charge trapping mechanism analyses[5,6]. However, few *C-V* tests that focus on interface characteristics and charge trapping analyses relative to the types of carriers, especially at high temperatures and biases of gate voltages, have been conducted. These kinds of analyses are presented in this paper.

2 Experiment

A control oxide, a layer of Si dots, and a tunneling oxide are the elements of NCNVM, and they compose a sandwich structure. The original structure, which became the sandwich structure after annealing, was fabricated by evaporation of SiO powder using electron beam evaporation. The resistance of the (100) p-type Si substrate is 15～20Ω · cm^{-1}, and the thicknesses of the tunneling oxide, silicon rich oxide, and control oxide are 4, 4, and 20nm, respectively. Annealing was performed to form NC-Si from the silicon-rich oxide layer in N_2 atmosphere at 900℃ for 30min and then 1100℃ for 30min. For electrical measurement, Al top electrodes were deposited by direct current sputtering using a shadow mask. The typical area of the top electrodes is 9.62×10^{-2} mm^2, while the largest electrode is about twice the area

* Project supported by the State Key Development Program for Basic Research of China (No. 2006CB302702)
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Received 26 January 2007, revised manuscript received 10 April 2007

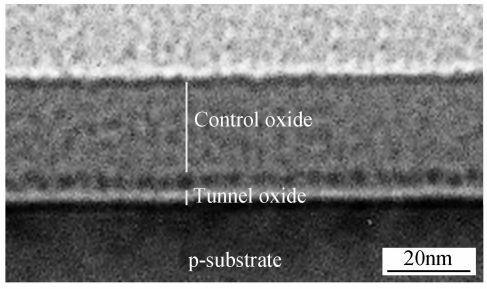

Fig. 1 TEM photo of the MOS capacitor

of the smallest electrode.

TEM was used to test the physical appearance of the NCNVM. *C-V* test was performed using an HP 4284 LCR meter under different conditions such as temperature and voltage to uncover storage characteristics.

3 Results and discussion

3.1 TEM measurement

Figure 1 shows a TEM photo of the MOS capacitor. The diameter of the silicon dots is 2～3nm, and the density of the silicon dots is calculated to be $7\times10^{12}\,\mathrm{cm}^{-2}$. The thicknesses of the control oxide and tunneling oxide are 20 and 3～4nm, respectively.

3.2 *C-V* test

V_T is one of the most fundamental elements of device technology. The V_T of a MOSFET can be represented as below.

$$V_T = V_{FB} + \frac{d_i}{\varepsilon_0\varepsilon_i}\sqrt{4\varepsilon_0\varepsilon_s qN_A V_F} + 2V_F(\text{pMOS})$$
$$V_T = V_{FB} - \frac{d_i}{\varepsilon_0\varepsilon_i}\sqrt{4\varepsilon_0\varepsilon_s qN_D V_F} - 2V_F(\text{nMOS}) \quad (1)$$

Here, V_{FB} represents the flat-band voltage, V_F is the Fermi potential, d_i is the thickness of the oxide layer, ε_0 is the permittivity of vacuum, ε_i and ε_s are the relative dielectric permittivities for oxide and silicon, q equals 1.602×10^{-19} C, and N_A and N_D are the concentrations for donor and acceptor impurities.

Moreover, V_{FB} can be measured through *C-V* testing. We choose a MOS capacitor to perform the *C-V* test and analyze the storage characteristic of the NC-Si devices. All of the *C-V* tests are performed under a 1MHz, 30mV signal.

Firstly, the *C-V* test is performed at room temperature (RT, 25℃) and different gate voltage sweep ranges: gate voltage sweep forward and backward between negative and positive 9, 11, and 15V. The results are shown in Fig. 2. In Fig. 2, np represents a sweep from negative to positive voltage, and pn represents a sweep from positive to negative voltage (np and pn in other figures mean the same). The value of ΔV_{FB} increases when the range of the gate voltage increases. Furthermore, the curves of the gate voltage sweeping from negative to positive shift more than the curves of gate voltage sweeping from positive to negative, and all the shifts are left-handed as well. Considering that the substrate of the MOS capacitor is p-type and the majority carriers are holes, we conclude that there are many more traps for holes than electrons. On the contrary, V_T of the nMOSFET displays a shift characteristic of majority carriers (electrons) trapping as well[7]. We then also conclude that there are traps in the NC sandwich structure which are capable of trapping carriers, resulting in a majority carrier trapping related threshold voltage shift and program window (ΔV_T) change.

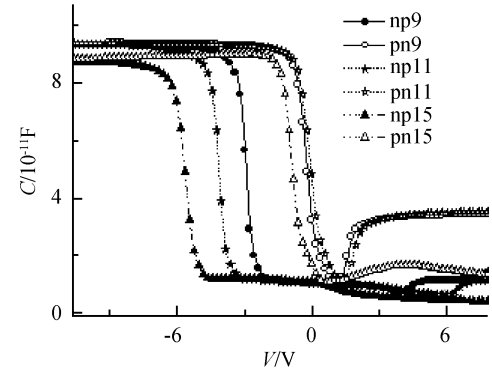

Fig. 2 *C-V* test at room temperature

Secondly, *C-V* tests in different sweep ranges are performed at different temperatures: RT (25℃), 35, 50, and 65℃. The results of 35, 50, and 65℃ are shown in Fig. 3.

In Fig. 3, 35np55 means a sweep from −5V to +5V at 35℃; the other labels are similarly defined. As the program and erase temperature increases, the slope of transition ranges between different curves vary, which displays interface state related aberrations[8]. These aberrations of hystereses contribute to a smaller ΔV_{FB} (program window) and voltage threshold shift. Furthermore, the differences between the initial and final

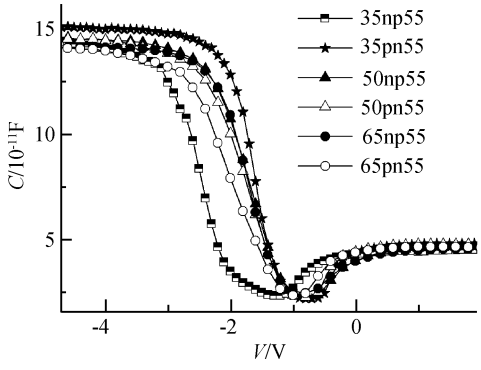

Fig. 3　*C-V* test at different temperatures

curves (after program/erase at higher temperatures: 35, 50, 65 and 80℃) are presented in Fig. 4. *C-V* tests are performed under the gate voltages between negative and positive 5V. After program/erase at higher temperatures, the hysteresis curves shift left, because many carriers, especially majority carries (holes) are trapped. Finally, the curve of the gate voltage sweeping forward (np55last) shifts abruptly toward the backward one (pn55last), which is a feature of the high density interface state[8] and indicates deterioration of the storage characteristic.

Lastly, +/− BT analysis is performed at 70℃ to test the moveable charge density (N_m). The results of +/− BT analysis of *C-V* test of different sweep ranges (between negative and positive 3, 5, and 7V) are shown in Fig. 5.

When the gate voltage is swept forward and backward between negative and positive 3V, ΔV_{FB} at room temperature ($\Delta V_{FB}|_{RT}$, marked delta$_{RT}$ in the figure above) is nearly 0; and the N_m of forward and backward +/− BT analysis is almost the same. The uniformity of N_m for the forward and backward sweeps results from the short sweep range, which is not able to the program or erase

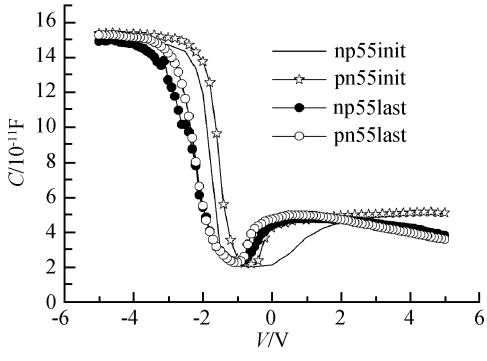

Fig. 4　*C-V* test before and after temperature changes

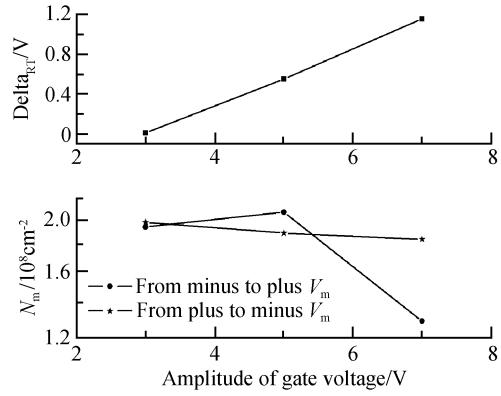

Fig. 5　+/− BT analysis in different gate voltage ranges

the carriers between the NC-Si layer and substrate through the tunneling oxide. When the gate voltage is swept forward and backward between negative and positive 5V, $\Delta V_{FB}|_{RT}$ is nearly 0.6V and the N_m of +/− BT analysis of the forward sweep is a little bit more than that of the backward sweep. The difference between N_m of the forward and backward sweeps is the result of the program and erase characteristic of the NC-Si. The N_m of forward sweep is higher because the substrate is p-type and the holes are majority carriers that contribute to the storage characteristic. When the gate voltage is swept forward and backward between negative and positive 7V, is nearly 1.2V and the N_m of +/− BT analysis of the forward sweep is much less than the backward sweep. The crest fall of N_m of the forward sweep is mainly because of the majority carriers' trap. The uniformity of N_m for the backward sweep is mainly because the trap mechanism towards minority carriers is much weaker than towards majority carriers. The increase of ΔV_{FB} is because of majority carriers trapped at NCs. ΔV_{FB} of the third sample is nearly twice that of the second sample and may be the result of strong trapping and weak erasing mechanisms during +/− BT analysis. The results of +/− BT analysis with different biases adding to 5V amplitude gate voltage during *C-V* tests are compared in Fig. 6.

$\Delta V_{FB}|_{RT}$ (marked delta$_{RT}$ in the figure above) of the 0-bias *C-V* sweep is much larger than −1V-bias and a little larger than +1V-bias. Comparing $\Delta V_{FB}|_{RT}$ with N_m and Fig. 5 with Fig. 6 as well, the explanation could be that there are traps towards holes and electrons, and the effect of traps

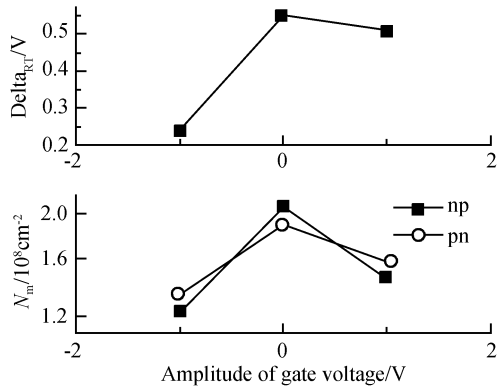

Fig. 6 +/− BT analysis with gate voltage bias during *C-V* test

on holes is more intensive, and the traps are more evident when the relative bias added to the *C-V* sweep voltage.

4 Summary

The storage characteristics of NC-Si devices are influenced by charge trapping characteristics and interface state-related effects. The deterioration of program window and V_T shift is quite noteworthy under high temperature, large voltage sweep range, and bias applied to sweep the voltage as well. It is quite possible to improve the storage character by adjusting the traps and interface states towards majority carriers, like energy band engineering and so on.

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基于不同测量手段的纳米晶器件的存储特性*

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摘要: 对纳米晶器件, 尤其是 MOS 电容进行了横截面 TEM 分析和不同条件下的电学特性(*C-V* 特性)测量, 包括 +/− BT 分析. 揭示了系统的纳米晶存储物理机制, 例如电荷俘获、界面态填充和温度特性. 研究结果表明, 高温、大电压摆幅和偏置情况下, 器件编程窗口的恶化和阈值电压的漂移与多数载流子的种类有关.

关键词: 纳米晶; 存储; 测量

PACC: 7125; 7300

中图分类号: TN4 **文献标识码:** A **文章编号:** 0253-4177(2007)08-1169-04

* 国家重点基础研究发展规划资助项目(批准号: 2006CB302702)

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2007-01-26 收到, 2007-04-10 定稿