Threshold Voltage Model of a Double-Gate MOSFET with Schottky Source and Drain*

Xu Bojuan, Du Gang, Xia Zhiliang, Zeng Lang, Han Ruqi, and Liu Xiaoyan†

(*Institute of Microelectronics, Peking University, Beijing* 100871, *China*)

Abstract: A quasi two-dimensional (2D) analytical model of a double-gate (DG) MOSFET with Schottky source/drain is developed based on the Poisson equation. The 2D potential distribution in the channel is calculated. An expression for threshold voltage for a short-channel DG MOSFET with Schottky S/D is also presented by defining the turn-on condition. The results of the model are verified by the numerical simulator DESSIS-ISE.

Key words: double-gate; Schottky barrier; threshold voltage
PACC: 7330; 4710
CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2007)08-1179-05

1 Introduction

As an alternative to conventional MOSFETs with doped S/D contacts, Schottky-barrier (SB) MOSFETs have attracted the attention of the device research community[1~3]. SB MOSFETs replace S/D impurity doping with silicide. There are numerous motivations for replacing pn junctions with Schottky contacts in the S/D regions, including low parasitic S/D resistance, low-temperature processing for S/D formation, and elimination of the parasitic bipolar effect[4]. Several simulation efforts have been undertaken to design and optimize SB MOSFETs[5~8]. Their main focus has been the current mechanism, including tunneling current and thermal current. However, little work has been done on the device model, especially on the compact model for SB MOSFETs[9].

In this paper, we develop a threshold model of SB DG MOSFETs based on the Poisson equation in quasi 2D analytically[9]. The turn-on conditions of an SB MOSFET are defined. The results of the model are verified by the numerical simulator DESSIS-ISE[10]. This model can be used as a tool for optimizing SB MOSFETs and a device model for IC design with SB MOSFETs.

2 Derivation of analytical model

Figure 1 shows a schematic diagram of a DG MOSFET with SB source and drain. The coordinate reference zero point is in the middle of the silicon film in the source side. $x = \pm T_{si}/2$ and $x = 0$ correspond to Si/SiO_2 interfaces and the channel center, respectively. The channel Boron doping density is $N_A = 10^{15}\ cm^{-3}$. φ_B is the S/D Schottky barrier height, L_g is the gate length, t_{ox} is the gate-oxide thickness, and T_{si} is the silicon film thickness.

2.1 Potential distribution

The potential distribution $\Psi(x, y)$ can be

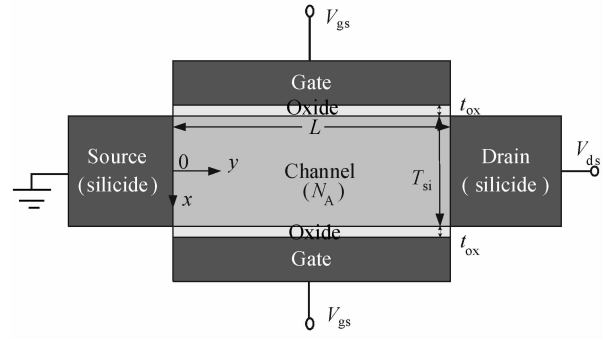

Fig. 1 Schematic of the cross section of a DG MOSFET with silicide source/drain

* Project supported by the State Key Development Program for Basic Research of China (No. 2006CB302705) and the National Natural Science Foundation of China (No. 60606013)
† Corresponding author. Email: xyliu@ime.pku.edu.cn
Received 30 January 2007, revised manuscript received 20 April 2007
©2007 Chinese Institute of Electronics

obtained by solving Poisson's equation in 2D to include the influence of the source/drain. Therefore, a lateral potential distribution along the channel is assumed while the perpendicular potential is under consideration. In order to solve Poisson's equation in 2D analytically, we assume a 2D potential distribution in the whole channel as

$$\Psi(x,y) = c_0(y) + c_1(y)\Psi(x) \tag{1}$$

where $c_0(y)$ is a function of lateral surface potential $\Psi_s(y)$, and $c_1(y)$ is the coupling coefficient which connects the lateral surface potential with the perpendicular potential $\Psi(x)$. The boundary conditions for $\Psi(x,y)$ are given as

$$\Psi(-T_{si}/2,y) = \Psi_{sf}(y) \tag{2a}$$

$$\Psi(T_{si}/2,y) = \Psi_{sb}(y) \tag{2b}$$

$$\left.\frac{\partial\Psi(x,y)}{\partial x}\right|_{x=-T_{si}/2} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \times \frac{\Psi(-T_{si}/2,y) - (V_{gs} - \Delta\Psi)}{t_{oxf}} \tag{2c}$$

$$\left.\frac{\partial\Psi(x,y)}{\partial x}\right|_{x=T_{si}/2} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \times \frac{(V_{gs} - \Delta\Psi) - \Psi(T_{si}/2,y)}{t_{oxb}} \tag{2d}$$

$$\Psi(x,0) = \varphi_B \tag{2e}$$

$$\Psi(x,L) = \varphi_B + V_{ds} \tag{2f}$$

where $\Psi_{sf}(y) = \Psi_{sb}(y) = \Psi_s(y)$ for a symmetric DG MOSFET, $t_{oxf} = t_{oxb} = t_{ox}$ for a DG MOSFET, and $t_{oxf} = t_{ox} \leqslant t_{oxb}$ for a UTB SOI MOSFET, V_{gs} is the gate voltage, V_{ds} is the drain voltage, φ_B is the Schottky barrier height, and $\Delta\Psi$ is the work function of both the top and bottom gate electrodes with respect to the intrinsic silicon. In other words, $\Delta\Psi = 0$ is for a mid-gap work function gate, $-E_g/2q$ for an n^+ poly gate, and $+E_g/2q$ for a p^+ poly gate.

The 1D Poisson's equation along the channel in the silicon film takes the following form with only a mobile charge (electrons) term[11],

$$\frac{d^2\Psi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} e^{q\Psi/kT} \tag{3}$$

where q is the electronic charge, n_i is intrinsic electron density in silicon, and ε_{si} is the permittivity of silicon. Here we consider an nMOS with $q\Psi/kT \gg 1$ so that the hole density is negligible.

The solution obtained by solving Poisson's equation (3) gives the corresponding potential distribution in the silicon film[11],

$$\Psi(x) = \frac{kT}{q}\ln\left[\frac{n_0}{n_i}\cos^{-2}\left[\left(\frac{q^2 n_0}{2\varepsilon_{si}kT}\right)^{1/2} x\right]\right] \tag{4}$$

where n_0 is the electron density in the silicon film center where $x = 0$.

Calculating Eqs. (1), (2), and (4), we get the solutions of $c_0(y)$ and $c_1(y)$. Substituting $c_0(y)$, $c_1(y)$ and Eq. (4) into Eq. (1), we obtain a 2D potential distribution.

$$\Psi(x,y) = \Psi_s(y) + \frac{\varepsilon_{ox}[\Psi_s(y) - (V_{gs} - \Delta\Psi)]}{2\varepsilon_{si}T_{si}\left(\frac{q^2 n_0}{2\varepsilon_{si}kT}\right)^{1/2}\tan\left[\left(\frac{q^2 n_0}{2\varepsilon_{si}kT}\right)^{1/2} \times \frac{T_{si}}{2}\right]} \times \ln\left[\cos^2\left[\left(\frac{q^2 n_0}{2\varepsilon_{si}kT}\right)^{1/2} x\right] / \cos^2\left[\left(\frac{q^2 n_0}{2\varepsilon_{si}kT}\right)^{1/2} \frac{T_{si}}{2}\right]\right] \tag{5}$$

Here $\Psi_s(y)$ can be derived by applying Gauss's law to a rectangular box of height T_{si} and length Δy in the channel depletion region as shown in the equation,

$$\frac{\varepsilon_{si}T_{si}}{\eta} \times \frac{\partial E_s(y)}{\partial y} - 2\frac{\varepsilon_{ox}}{t_{ox}}[V_{gs} - \Delta\Psi - \Psi_s(y)] = -Q_{ch} \tag{6}$$

where $E_s(y)$ is the front lateral surface electric field, and Q_{ch} is the channel carrier charge corresponding to T_{si}, V_{gs} and V_{ds}. The solution to Eq. (6) under the boundary conditions of Eqs. (2e) and (2f) is

$$\Psi_s(y) = \Psi_L + \frac{\varphi_B + V_{ds} - \Psi_L}{\sinh(L/\lambda)}\sinh(y/\lambda) + \frac{\varphi_B - \Psi_L}{\sinh(L/\lambda)}\sinh[(L-y)/\lambda] \tag{7}$$

where $\Psi_L = V_{gs} - \Delta\Psi - \frac{Q_{ch}t_{ox}}{2\varepsilon_{ox}}$ and $\lambda = \sqrt{\frac{\varepsilon_{si}T_{si}t_{ox}}{2\eta\varepsilon_{ox}}}$. Here we suppose effective gate voltage $V'_{gs} = V_{gs} - V_{FB}$.

The channel surface potential expressed by Eq. (7) can be thought as the long-channel surface potential modified by the electric field of the S/D. The effects of the variation of the lateral field in the depletion layer are incorporated through the fitting parameter η. In this paper, $\eta = 1.8$.

2.2 Threshold voltage model

The Schottky barrier at the source and drain changes the current control mechanism of an SB MOSFET compared to a conventional MOSFET. The Schottky barrier at the source is efficiently modulated by the gate bias, which controls the carrier transport into the channel. The threshold voltage V_{th} is the gate voltage at which the carrier injection into the channel is enough larger than the on current of SB DG MOSFET. There are two components of the carrier injection into the channel through the Schottky barrier, one of which is

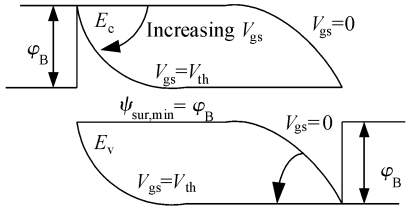

Fig. 2 Schematic diagram of the definition of threshold voltage for one gate of DG MOSFET with SB S/D

the thermal emission part for carriers with energy higher than SB, and the other is the tunneling part. With increasing gate voltage, the shape of SB in the source side is modulated by the gate voltage and becomes thinner corresponding to the increase of tunneling current. However, the threshold voltage of an SB MOSFET can not be simply defined as the value of the gate voltage when the surface potential reaches strong inversion condition because of the unique current control mechanism of an SB MOSFET. Thus it is difficult to obtain an analytical threshold voltage model for an SB MOSFET[12].

In this paper, V_{th} is defined as the value of V_{gs} at which the minimum of the surface potential $\Psi_{sur,min}$ is equal to the source Schottky barrier height φ_B as shown in Fig. 2.

The minimum surface potential in the channel $\Psi_{sur,min}$ and its location y_0 can be obtained analytically by solving

$$\left.\frac{\partial \Psi_s(y)}{\partial y}\right|_{y_0} = 0, \Psi_{sur,min} = \Psi_s(y_0) = \varphi_B \quad (8)$$

Substituting Eq. (7) into Eq. (8) results in the threshold voltage model for a short-channel SB DG MOSFET.

$$V_{th} = \Delta\Psi + \frac{Q_{ch} t_{ox}}{2\varepsilon_{ox}} + \varphi_B - \frac{\alpha}{1-4\alpha} V_{ds} \quad (9)$$

Here α is a parameter describing the effects of the drain voltage V_{ds} on the threshold voltage V_{th}, which is expressed as $\alpha = 1/2\cosh(L/2\lambda)$.

3 Results and discussion

To verify the analytical model, the 2D device simulator DESSIS-ISE[10] was used to simulate the device characteristics of an SB DG MOSFET, including the potential distribution and the threshold voltage. All the device parameters were fixed unless otherwise stated and are given in the figure captions.

Figure 3 shows the variation of the surface potential with the position in the channel for different effective gate voltages V'_{gs} obtained from the analytical model and DESSIS simulation at 0.2, 0.4, 0.6, and 0.8V, where the Schottky barriers of the source and drain are both 0.2eV. It can be seen from Fig. 3 that the surface potential of the drain is slightly greater than that of the source because of the drain voltage bias, 0.05V. With increasing effective gate voltage, the barrier of the source becomes thinner, and then the carriers tunnel into the channel more easily. Compared with the results of 2D device simulation, it is verified that the model is appropriate for an SB MOSFET even at lower drain voltage, such as 0.05V.

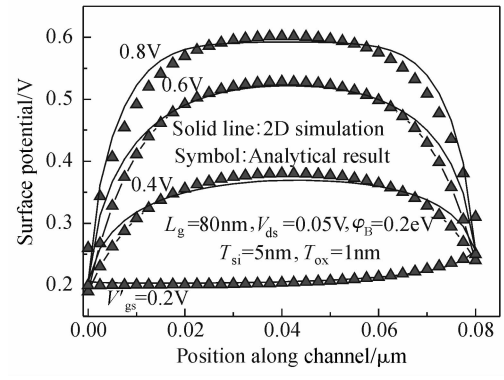

Fig. 3 Surface potential versus position along the channel for different gate voltages

Figure 4 shows the surface potential versus position in the channel for different drain voltages at 0.05 and 1.0V and with Schottky barrier heights of 0.2 and 0.5eV from the analytical model and DESSIS simulation results. It can be seen that the surface potential near the drain side increases dramatically due to the increase of the

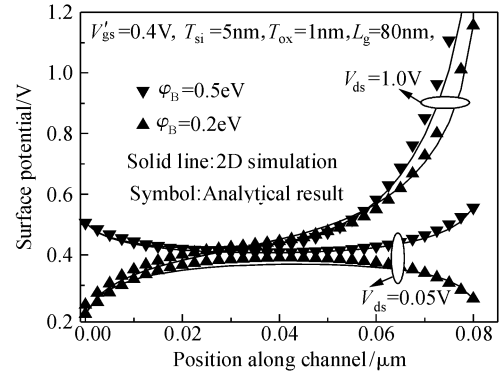

Fig. 4 Surface potential versus position in channel for different drain voltages and Schottky barriers

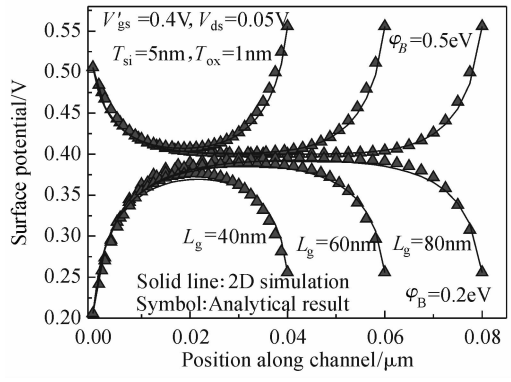

Fig. 5 Surface potential versus position in channel for different gate lengths and Schottky barrier height

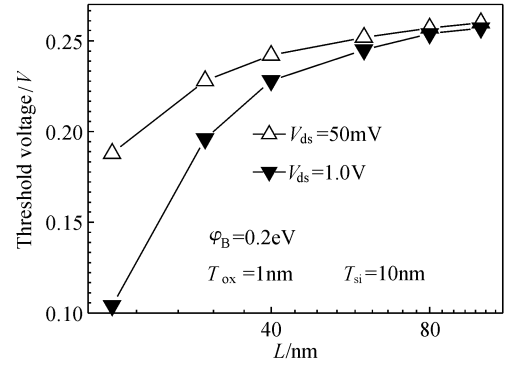

Fig. 7 Threshold voltage versus gate length L_g with different drain voltages

drain bias V_{ds} from 0.05 to 1.0V, and the potential distribution near the S/D regions are sensitive to the Schottky barrier height. The results from the analytical model are almost the same as the simulation results at different drain voltages and at different Schottky barrier heights.

It is shown in Fig. 5 that the surface potential distribution along the channel varies with the channel length at 40, 60, and 80nm when the Schottky barrier heights are 0.2 and 0.5eV, respectively. The DIBL effect can be found for a short channel SB MOSFET as shown in Fig. 5. Therefore, the potential model can describe the short channel effects of an SB MOSFET due to the solution of the Poisson equation in quasi 2D.

Figure 6 shows the threshold voltage versus gate length L_g with different Schottky barrier heights φ_B and silicon film thicknesses T_{si}, obtained from analytical results when T_{ox} = 1.0nm and V_{ds} = 1.0V. The relationship between Schottky barrier and threshold is linear, meaning that an increase in the value of the barrier corresponds to

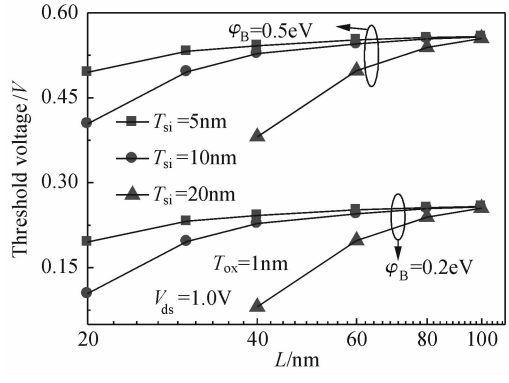

Fig. 6 Threshold voltage versus gate length L_g with different φ_B and T_{si}

an increase in the value of the threshold voltage. Figure 7 shows the threshold voltage versus gate length L_g with different drain voltages. The effect of the drain voltage of an SB MOSFET on the threshold voltage is almost equivalent to that of a conventional MOSFET, which means that the effect is more evident in the short channel device than in the long. The method defining the threshold voltage of an SB MOSFET is reasonable and worth applying in the modeling fields for SB MOSFETs.

4 Conclusion

An analytical potential model for SB DG MOSFETs based on the Poisson equation in quasi 2D is developed. Moreover, a threshold voltage model is also deduced by defining the turn-on conditions of an SB MOSFET based on the potential model. The results of the potential model are verified by numerical simulation using DESSIS-ISE. Therefore, this model can be used as a tool for SB MOSFET design. It gives helpful physical insight into novel devices on the nanoscale, and it also serves as a useful and convenient device model for IC design with SB MOSFETs.

References

[1] Lepselter M P, Sze S M. SB-IGFET: an insulated gate field-effect transistor using Schottky barrier contacts as source and drain. Proc IEEE, 1968, 56: 1400

[2] Kedzierski J, Xuan P, Anderson E H, et al. Complementary silicide source-drain thin-body MOSFETs for 20nm gate length regime. IEDM Tech Dig, 2000: 57

[3] Guo J, Lundstrom M S. A computational study of thin-body, double-gate, Schottky barrier MOSFETs. IEEE Trans Elec-

tron Devices,2002,49(11):1897
[4] Larson J M, Snyder J P. Overview and status of metal SD Schottky-barrier MOSFET technology. IEEE Trans Electron Devices,2006,53(5):1593
[5] Du G, Liu X, Liu M, et al. Characterizations of double-gate SBTT studying by a 2-D full-band Monte Carlo device simulator. Proc 4th Int Workshop Junction Technol,2004:325
[6] Ieong M K, Solomon P M, Laux S E, et al. Comparison of raised and Schottky source/drain MOSFETs using a novel tunneling contact model. IEDM Tech Dig,1998:733
[7] Connelly D, Faulkner C, Grupp D E. Optimizing Schottky S/D offset for 25-nm ual-gate CMOS performance. IEEE Electron Device Lett,2003,24(6):411
[8] Matsuzawa K, Uchida K, Nishiyama A. A unified simulation of Schottky and ohmic contacts. IEEE Trans Electron Devices,2000,47(1):103
[9] Xu Bojuan, Xia Zhiliang, Liu Xiaoyan, et al. An analytical potential model of double-gate MOSFETs with Schottky source/drain. ICSICT, Shanghai,2006:1296
[10] DESSIS, ISE TCAD Manuals, Integ Syst Engr AG Zurich, Switzerland
[11] He Jin, Xi Xuemei, Chan Mansun, et al. A non-charge-sheet based analytical model of undoped symmetric double-gate MOSFETs using SPP approach. Proceedings of 5th International Symposium on Quality Electronic Design,2004:45
[12] Knoch J, Zhang M, Mantl S, et al. On the performance of single-gated ultrathin-body SOI Schottky-barrier MOSFETs. IEEE Trans Electron Devices,2006,53(7):1669

双栅肖特基源漏 MOSFET 的阈值电压模型*

徐博卷 杜 刚 夏志良 曾 朗 韩汝琦 刘晓彦†

(北京大学微电子学研究院，北京 100871)

摘要：通过求解泊松方程得到了双栅肖特基势垒 MOSFET 的解析模型.这个解析模型包括整个沟道的准二维电势分布和适用于短沟双栅肖特基势垒 MOSFET 的阈值电压模型.数值模拟器 ISE DESSIS 验证了模型结果.

关键词：双栅；肖特基势垒；阈值电压
PACC：7330；4710
中图分类号：TN386 **文献标识码**：A **文章编号**：0253-4177(2007)08-1179-05

* 国家重点基础研究发展规划(批准号:2006CB302705)和国家自然科学基金(批准号:60606013)资助项目
† 通信作者.Email:xyliu@ime.pku.edu.cn
2007-01-30 收到,2007-04-20 定稿
©2007 中国电子学会