Mismatch Calibration Techniques in Successive Approximation Analog-to-Digital Converters

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Abstract: Comparator offset cancellation and capacitor self-calibration techniques used in a successive approximation analog-to-digital converter (SA-ADC) are described. The calibration circuit works in parallel with the SA-ADC by adding additional calibration clock cycles to pursue high accuracy and low power consumption, and the calibrated resolution can be up to 14bit. This circuit is used in a 10bit 3Msps successive approximation ADC. This chip is realized with an SMIC 0.18μm 1.8V process and occupies 0.25mm^2. It consumes 3.1mW when operating at 1.8MHz. The measured SINAD is 55.9068dB, SFDR is 64.5767dB, and THD is $-$74.8889dB when sampling a 320kHz sine wave.

Key words: analog-to-digital converter; successive approximation; self-calibration techniques
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1 Introduction

As device dimensions and operating voltage continue to be scaled down, analog circuits are being pushed to their operational limits. Performance degradation such as sampling linearity and signal-to-noise ratio (SNR) due to limited signal swing exists, so calibration methods are needed to improve the accuracy of analog circuits.

The accuracy of analog-to-digital (A/D) converters is often limited by the mismatch of both passive components and ideally identical transistors of the circuits. Comparator offset voltage and capacitor mismatch can cause harmonic distortion and thus greatly influence the accuracy of SA-ADCs. Input and output storage[1] can eliminate the offset voltage of comparators, but this requires additional capacitors on the signal path, thus reducing the bandwidth. Furthermore, errors due to channel charge injection cannot be overcome either[2]. For capacitor mismatch, laser trimming can guarantee the resolution, but it is an expensive and time-consuming procedure. Tan *et al*.[3] adopted a sub-capacitor array to calibrate the error of the capacitor array. However, this method is limited by the parasitic and offsets of the sub-capacitor array itself, while also increasing the capacitive load of the input signal. Leung *et al*.[4] merged small capacitors from the bigger capacitors in series. The calibration is based on adding or removing small capacitors to get a good match in the array. But it provides only a resolution of 1/8 of the unit capacitance value C and makes the design of the layout more difficult.

This paper presents self-calibration methods for SA-ADCs, with the calibration module, and both comparator offset voltage and capacitor mismatches can be effectively eliminated, thus improving the performances of SA-ADCs. The circuit runs in parallel with the proposed SA-ADC by adding additional calibration clock cycles. The block diagram of the proposed SA-ADC is shown in Fig. 1, in which the calibration module is indicated by the dashed line. A pseudo-differential input stage is adopted for both improving power supply rejection and rejecting common mode noise.

2 Comparator offset cancellation

To achieve higher speed, a regeneration comparator is used[5]. In order to maximize the speed, the number of pre-amps should be 6[6]. Considering the tradeoff among speed, power and area, 2 stage pre-amps are used in this design. In order to

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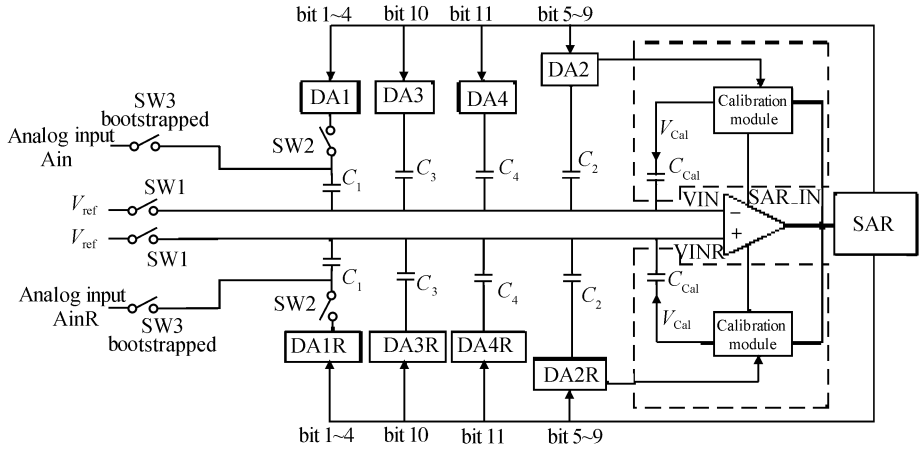

Fig. 1 Block diagram of proposed SA_ADC

compensate the disadvantages of the offset cancellation techniques mentioned above, negative feedback is introduced. By adjusting the load of the first stage pre-amp through negative feedback, the input offset voltage can be effectively reduced. Figure 2 is the circuit of the comparator.

During calibration periods, a reference voltage V_{ref} is applied to both inputs VIN and VINR. Without offset, the output of comparator should be 0 or 1 of all rate equality; however, if offset occurs, the output will be stable at 0 or 1. When CK3 is 1, the output signal charges capacitor C_1, and then CK3 becomes 0 and CK4 is 1. Then the charge stored on C_1 is redistributed between C_1 and NM16 , whose source and drain are connected to form a capacitor. For simplicity, the initial voltages on both capacitors are assumed to be 0. After charge redistribution, we have:

$$\begin{cases} Q_{C1} = Q'_{C1} + Q_{NM16} \\ \dfrac{Q'_{C1}}{C_1} = \dfrac{Q_{NM16}}{C_{NM16}} \end{cases} \tag{1}$$

where Q'_{C1} and Q_{NM16} are the charges stored on C_1 and NM16 after charge redistribution.

Because the value of the capacitor formed by NM16 is $(WL)_{NM16} C_{ox}$, the voltage variation of transistor NM16 is given by

$$\Delta V_{NM16} = \frac{Q_{C1}}{C_1 + (WL)_{NM16} C_{ox}} \tag{2}$$

By properly biasing the first stage pre-amp, transistor NM4 operates in its triode region. After calibration, the absolute resistance variation of NM4 can be written as

$$|\Delta R_{NM4}| = \left| \frac{1}{\mu_n C_{OX} \left(\frac{W}{L}\right)_{NM4} (V_{GSNM4} + \Delta V_{NM16} - V_{THNM4})} - \frac{1}{\mu_n C_{OX} \left(\frac{W}{L}\right)_{NM4} (V_{GSNM4} - V_{THNM4})} \right| \tag{3}$$

According to Eqs. (2) and (3), by decreasing C_1 or increasing WL of NM16, both ΔV_{NM16} and $|\Delta R_{NM4}|$ can be reduced, thus increasing the accuracy of the calibration, but at the expense of lower

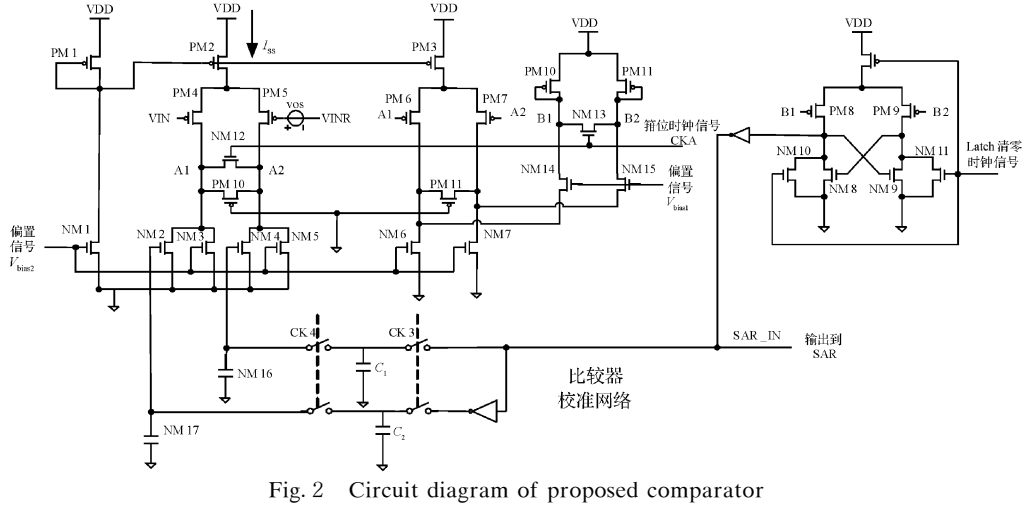

Fig. 2 Circuit diagram of proposed comparator

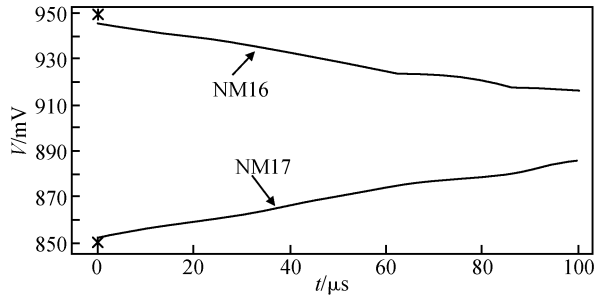

Fig. 3　Simulated waveform of offset calibration

calibration speed. A similar conclusion can be drawn for NM17 and NM2. The calibration method does not add any capacitors on the signal path, and is immune to process and temperature variation[7], thus improving the speed and accuracy greatly. By adding a 50mV offset voltage to the input devices, the mismatch can be calibrated within 100μs. Figure 3 shows the static result of the calibration as simulated by HSpice.

When the comparator works during normal conversion cycles, simulation results show that when the input common mode voltage is 0.5V with a 2mV voltage swing, the output voltage swing is 103mV after amplification, and thus the total gain is about 52. When operating at a clock frequency of 10MHz, the minimum signal detected by the latch is about 2.15mV, divided by the overall gain of pre-amps, and the comparator can get a resolution of 14bit (with a 1Vpp input differential signal), which is accurate enough for a 10bit application.

3　Capacitor self-calibration

A combination of a resistor network and capacitor array is used to perform the DACs in the SA-ADC to realize an economically feasible die size[8] as shown in Fig. 4.

In Fig. 4, DA1(R) and DA2(R) are controlled by bits 1～4 and bits 5～9 of the SA-ADC, respectively, while DA3(R) and DA4(R) are controlled by the lower bit 10 and bit 11.

The capacitors C_1 and C_2 have the greatest weights and are the main limiting factors of the resolution of the SA-ADC. Mismatch between them will cause large harmonic distortion and thus degrade the spurious-free dynamic range (SFDR) of the SA-ADC[9]. Bit 1 is the MSB weighted by $\frac{1}{2}V_{FS}$. The weight of each of the other bits is reduced successively by a factor of 2, except for bit 6 and bit 7, whose weights are both $\frac{1}{64}V_{FS}$. Bit 11 is the LSB, which equals $\frac{1}{1024}V_{FS}$, in which V_{FS} is the full-scale input voltage of the SA-ADC.

When there are any mismatch among the capacitors, the voltages of the nodes VIN and VINR will not be equal. In such a situation, the calibration module will calibrate the mismatch between C_1 and C_2 through the calibration capacitor $C_{cal(R)}$, and this adjustment will continue through several calibration cycles until the net change value at node VIN(R) comes to zero. A linear differential attenuator is proposed to compensate for the slight capacitor mismatches between the arbitrary output of DA1 and DA2.

As set forth above, the voltage weights of DA1(R)～DA4(R) are $\frac{1}{16}V_{FS}$, $\frac{1}{64}V_{FS}$, $\frac{1}{32}V_{FS}$ and $\frac{1}{64}V_{FS}$, respectively. The capacitors C_1, C_2, C_3, C_4, C_{cal} have values of $16C$, $16C$, C, C, and C, re-

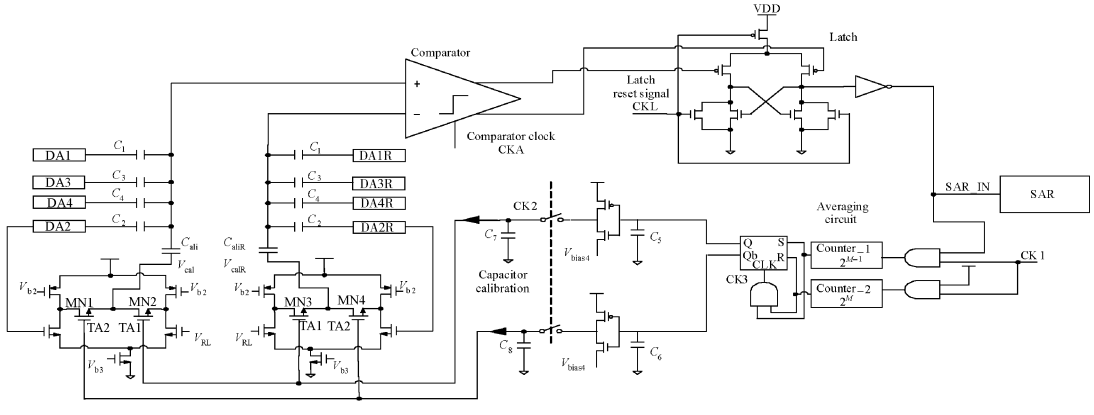

Fig. 4　Circuit diagram of DAC with capacitor calibration

spectively. We have

$$\begin{aligned}\mathrm{VIN}-\mathrm{VINR}=&\left[\sum_{1}^{4} D_i 2^{i-1}\frac{1}{16}V_{\mathrm{FS}}-(\mathrm{Ain}-\mathrm{AinR})\right]\times\\&\frac{C_1}{C_{\mathrm{sum}}}+\left(\sum_{1}^{5} D_{i+4}2^{i-1}\frac{1}{64}V_{\mathrm{FS}}\right)\times\frac{C_2}{C_{\mathrm{sum}}}+\\&\left(D_{10}\frac{1}{32}V_{\mathrm{FS}}\right)\times\frac{C_3}{C_{\mathrm{sum}}}+\left(D_{11}\frac{1}{64}V_{\mathrm{FS}}\right)\times\\&\frac{C_4}{C_{\mathrm{sum}}}+(V_{\mathrm{cal}}-V_{\mathrm{calr}})\times\frac{C_{\mathrm{cal}}}{C_{\mathrm{sum}}}\\=&\left[\left(\sum_{1}^{4} D_i 2^{i-1}\times\frac{1}{16}V_{\mathrm{FS}}+\sum_{1}^{5} D_{i+4}2^{i-1}\times\right.\right.\\&\frac{1}{256}V_{\mathrm{FS}}+D_{10}\times\frac{1}{512}V_{\mathrm{FS}}+D_{11}\times\frac{1}{1024}V_{\mathrm{FS}}\Big)-\\&\left.(\mathrm{Ain}-\mathrm{AinR})\right]\times\frac{16}{23}+(V_{\mathrm{cal}}-V_{\mathrm{calr}})\times\frac{1}{23}\end{aligned}\tag{4}$$

where D_i is the digital output of bit i; D_7, D_8, D_9 represent 2^2, 2^3, 2^4, respectively, and $C_{\mathrm{SUM}} = C_1 + C_2 + C_3 + C_4 + C_{\mathrm{cal}} = 23C$.

When the ADC works, the term $(V_{\mathrm{cal}} - V_{\mathrm{calr}}) \times \frac{1}{23}$ is used to calibrate the mismatch between C_1 and C_2.

The capacitors C_7 and C_8 will be charged or discharged according to the result of the voltage at the node so as to control the potential at TA1 and TA2. An averaging circuit is included. Counter_2 has a period of 2^M ($M = 4$ in this case) clocks. Counter_1, which counts only when the comparator output is high, has a period of the 2^{M-1} cycles. Both of the counters average the numbers of highs and lows, store the result in an SR Flip-Flop, and pass it on to C_5 and C_6. The NM1～NM4 controlled by TA1 and TA2 work in the deep triode region just like voltage controlled resistors, and thus the gain of the differential amplifier (A_{V}) will be low. The calibration signals V_{cal} and $V_{\mathrm{cal}}(R)$ are linear summations of the potentials at TA1 and TA2, depending on the resistance ratios among NM1～NM4:

$$V_{\mathrm{cal}} = \mathrm{DA2}\times A_{\mathrm{V}}\times\frac{R_{\mathrm{NM16}}}{R_{\mathrm{NM16}}+R_{\mathrm{NM17}}}\tag{5}$$

$$V_{\mathrm{cal}}(R) = \mathrm{DA2}(R)\times A_{\mathrm{V}}\times\frac{R_{\mathrm{NM18}}}{R_{\mathrm{NM18}}+R_{\mathrm{MN19}}}\tag{6}$$

Thus the mismatch between C_1 and C_2 can be calibrated by generating the controlled potential of the calibration capacitors C_{cal} and $C_{\mathrm{cal}}(R)$.

If there are no mismatch, the final voltages of TA1 and TA2 are about 1.3V. The voltage step between each calibration process is 7×10^{-5} V, which ensures a 14bit resolution. Therefore, the voltage adjustment each time is small, and the accurate adjustment of C_1 and C_2 takes a long time.

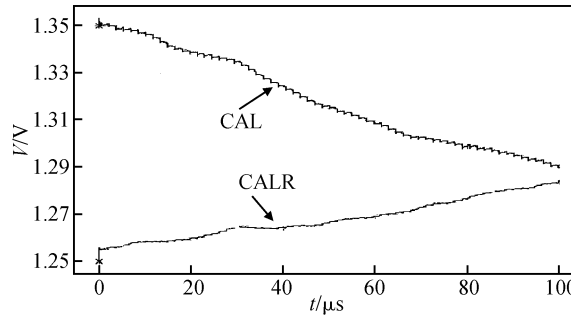

Fig. 5 Static simulated result of capacitor mismatch calibration

Figure 5 is the static simulated result of capacitor mismatches calibration with HSpice.

4 Measurement results

The SA-ADC has been fabricated in SMIC 0.18μm single-poly six-metal CMOS as a module of the SoC system Garfield4Plus designed by the national ASIC center, southeast university. The chip is packaged in PQFP-176 Lead. Figure 6 is the layout pattern, and Figure 7 is the test board of the proposed SA-ADC. When the chip is set to the "MacroTest" mode, the SA-ADC can be tested separately.

Figures 8～10 are the measured dynamic and static results of the proposed SA-ADC, respectively. The SA-ADC is driven by a sampling clock of 1.8MHz generated by PLL, which is also integrated on the chip. The input signal is generated from a Hewlett-Packard HP8648B function generator, with an amplitude of −1dBFS and a frequency of 320kHz. The output of SA-ADC is buffered by

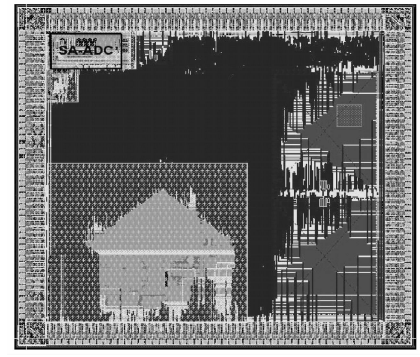

Fig. 6 Layout pattern of SoC including ADC

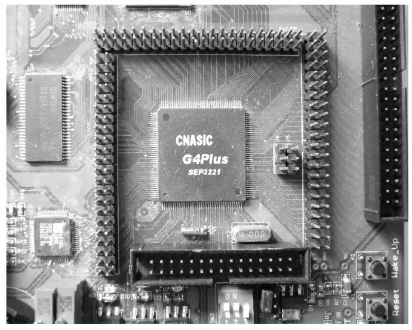

Fig. 7　Test board of proposed SA-ADC

SN74ALVCH16244, and then goes into an Agilent 16702B logic analyzer. The data captured by the logic analyzer is shown in Fig. 11. The measured differential nonlinearity (DNL) is +0.8/−0.9LSB, and integral nonlinearity (INL) is +1.4/−1.1LSB. The 2048-point fast Fourier transform (FFT) shows 55.9068dB signal-to-noise and distortion (SINAD), which corresponds to a 9.003 effective number of bits (ENOB), 64.5767dB SFDR, and the total harmonic distortion (THD) is −74.8889dB. All measurements are performed with a 1.8V supply at room temperature. Table 1 summarizes the performance of the SA-ADC.

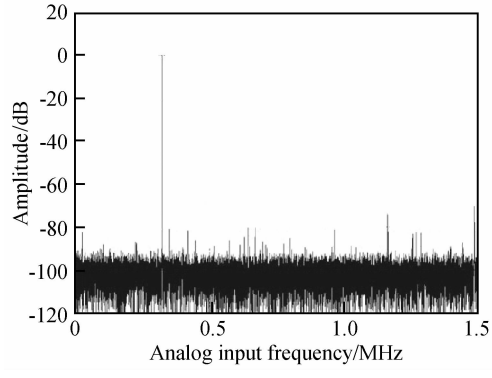

Fig. 8　Measured dynamic characteristics

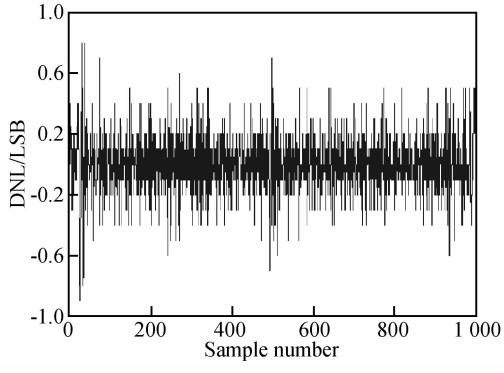

Fig. 9　Measured statistic characteristic: DNL

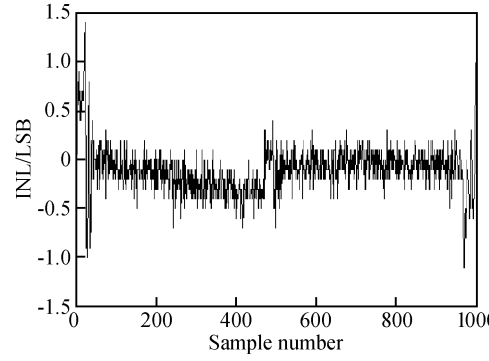

Fig. 10　Measured statistic characteristic: INL

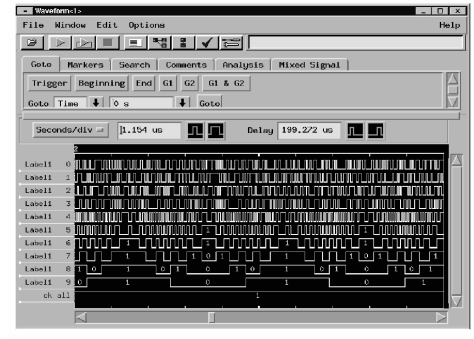

Fig. 11　Data captured by logic analyzer

As a commonly used figure of merit (FOM) for ADCs considering resolution, bandwidth and power[10,11], we use $\mathrm{FOM}=\dfrac{2^{\frac{\mathrm{SNR}-1.76}{6.02}}f_{\mathrm{samp}}}{P_{\mathrm{diss}}}$, compared with ADS7843 from TI and MC9328MX from FREESCALE. Their FOM are 284LSB-Hz/W and 560LSB-Hz/W for typical values, respectively, while the FOM of this design is 660 LSB-Hz/W for typical values, which shows an improvement of the SA-ADC performance.

Table 1　Measured results of the ADC

Parameter	Typical value
Supply voltage	1.8V
Resolution	10bit
Power consumption	3.1mW
Sample rate	3MHz
Input range(diff)	1Vpp
DNL(max)	0.8LSB
INL(max)	1.4LSB
SINAD	55.9068dB
THD	−74.8889dB
SFDR	64.5767dB
Area(ref)	0.25mm^2

5 Conclusion

Linear analog calibration techniques to reduce the comparator offset voltage and capacitor mismatch in an SA-ADC have been proposed in this paper. The calibration module can work in parallel with the SA-ADC conversion. It avoids the requirements of precise matching and trimming of components as normally expected with ADC signal conversion. The ADC is implemented in a signal-poly six-metal CMOS process. With the calibration module, measurement results show that the ADC can yield both good static and dynamic performance.

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逐次逼近型模数转换器中的失配校准技术

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摘要： 设计了一种用于逐次逼近型模数转换器中的比较器失调和电容失配自校准电路. 通过增加校准周期，该电容自校准结构即可与原电路并行工作，实现高精度与低功耗. 校准精度可达 14bit. 采用该电路设计了一个用于逐次逼近型结构的 10bit 3Msps 模数转换器单元，该芯片在 SMIC 0.18μm 1.8V 工艺上实现，总的芯片面积为 0.25mm^2. 芯片实测，在采样频率为 1.8MHz，输入 320kHz 正弦波时，信号噪声失真比为 55.9068dB，无杂散动态范围为 64.5767dB，总谐波失真为 -74.8889dB，功耗为 3.1mW.

关键词： 模数转换器；逐次逼近；自校准技术

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