A High Speed, 12-Channel Parallel, Monolithic Integrated CMOS OEIC Receiver*

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Abstract: The design and fabrication of a high speed, 12-channel monolithic integrated CMOS optoelectronic integrated circuit (OEIC) receiver are reported. Each channel of the receiver consists of a photodetector, a transimpedance amplifier, and a post-amplifier. The double photodiode structure speeds up the receiver but hinders responsivity. The adoption of active inductors in the TIA circuit extends the −3dB bandwidth to a higher level. The receiver has been realized in a CSMC 0.6μm standard CMOS process. The measured results show that a single channel of the receiver is able to work at bit rates of 0.8～1.4Gb/s. Altogether, the 12-channel OEIC receiver chip can be operated at 15Gb/s.

Key words: CMOS; optoelectronics; parallel receiver; high speed
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1 Introduction

The significant performance advantages of optoelectronics (OE) have motivated research into many applications[1]. The drive for greater bandwidth has conventionally concentrated on wavelength division multiplexing (WDM). However, with the trend towards multi-media and interactive communications, there is a major thrust towards building computing and switching systems that exceed the gigabit/sec (Gb/s) rate. To meet these requirements, these systems need multi-gigabit linking capacity, which parallel optical links can offer[2].

Silicon technologies[3] are generally known for their low-cost, large-scale integration benefits, but due to their poor performances as OE devices, OE devices and silicon were previously deemed to be incompatible. Ever since OE components moved into multi-channel, short-distance applications, however, silicon has been highly favored. Not only is silicon a mature technology to date, but its widespread availability and high reliability making it a cost-effective solution for parallel optical links. Several works about silicon-based OEIC receivers have been reported recently. Ghazi and Heide[4,5] demonstrated a high performance fiber receiver, but their photodetector was PIN-type and was not compatible with standard CMOS. Woodward and Krishnamoorthy[6,7] reported that DPD detectors can be fabricated in standard CMOS technologies and that their OEIC receiver can operate at 1Gbit/s in 0.35μm CMOS, but their receivers are all single-channel and cannot be used for high speed parallel optoelectronic communication.

In this paper, we demonstrate the design and fabrication of a high performance 12-channel, CMOS parallel monolithically integrated OEIC receiver that can be fabricated in standard CMOS without any modifications to the process. The design method for high speed and broad bandwidth will be discussed. The simulated and measured results of the 12-channel OEIC receiver will be also illustrated.

2 System structure

The system structure of the 12-channel OEIC

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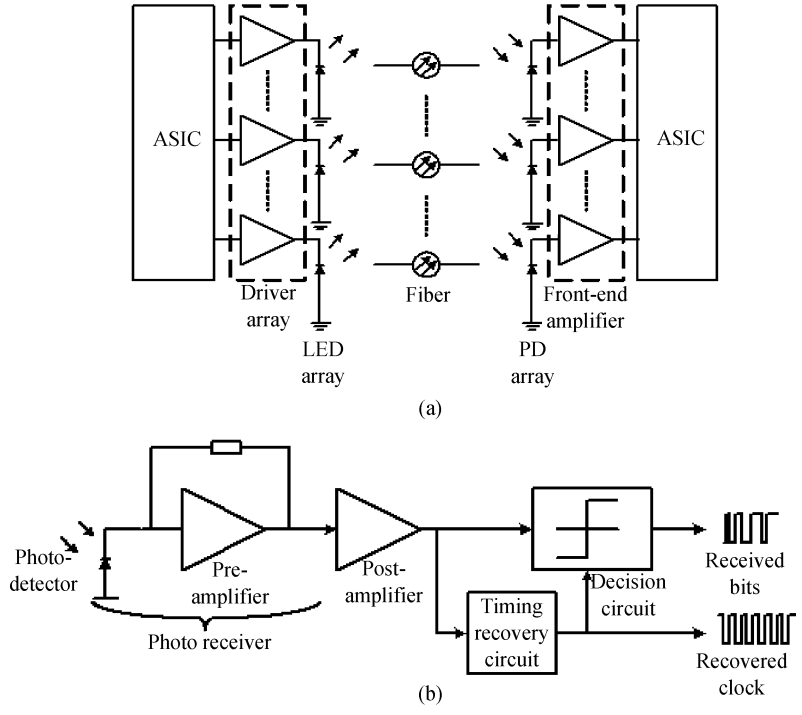

Fig.1 (a) System structure of 12-channel OEIC transceiver; (b) Single channel block diagram of the receiver

transceiver is shown in Fig.1(a). In a parallel optical link, bundles of fibers are used to interconnect the driver arrays to the receiver arrays directly, with no need for multiplexing (MUX) and demultiplexing (DEMUX) as the traditional WDM links should do.

Each single channel of the 12-channel CMOS OEIC receiver involves the blocks shown in Fig.1 (b). In general, light is impinged on the photodetector, and as it generates a photocurrent signal, the pre-amplifier converts the current to a voltage. Post-amplifiers can further amplify the signal to enhance the dynamic range. The timing recovery circuit extracts the clock and data from the incoming data stream.

3 Design of high speed photodetector

The CMOS integrated photodetector (PD) poses a new set of challenges. It is often the main bottleneck of the overall receiver because of either the RC time constant due to wire bonding or the slow transit photocarriers in the bulk substrate. The former issue is alleviated when integrating the PD on the same substrate; the latter issue can be solved by a DPD (double-PD) structure as discussed below, but this method requires a trade off between speed and responsivity.

Figure 2 shows a schematic cross section of the DPD detector structure[8]. The photodetector is implemented in a process identical to the formation of a p-type MOSFET. A p^+ region with an interdigitated lateral structure is designed as the anode of the photodetector, which is originally implanted to form the source and drain of the MOSFET. An n-well is tied to the detector bias (positive) and the guard ring is grounded. Thus, this structure forms two junctions: p-diffusion to n-well junction, and n-well to p-substrate junction. Inside the n-well, the interdigitated network of the p source-drain material is employed to broaden the depletion region, and forms the active terminal of the detector. Another junction formed

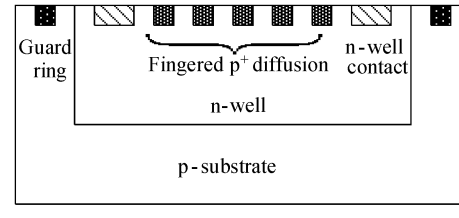

Fig.2 Cross section of the DPD detector structure

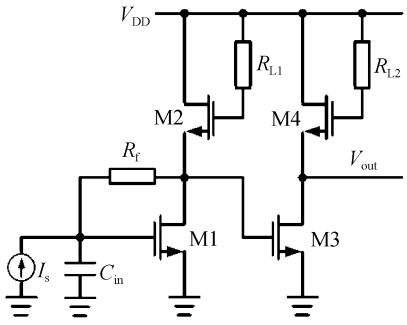

Fig. 3　Schematic of equivalent PD model and TIA circuit

by the n-well and p-substrate also plays an important role in this structure，called a screening diode. This diode prohibits the diffusive carriers generated in the bulk from contributing to the total generated current. This kind of screening scheme obviously trades responsivity for speed，because a large part of the photo generated carriers are discarded.

4　Design of high bandwidth TIA

A schematic of the TIA is shown in Fig. 3. In Fig. 3，I_s denotes the photo-generated current in units of μA，C_{in} is the input capacitance whose quantity is dominated by the p-n junction capacitance of the photodetector，and I_s and C_{in} together form the equivalent circuit model of the DPD. The first transimpedance stage consists of M1，M2 and R_{L1}，which transfer the input current from I_s into voltage，and the second stage involves M3，M4 and R_{L2}，which amplify the voltage to a higher level for the subsequent LA circuit. R_f is the feedback resistor.

For CMOS TIAs，the primary factor that constrains signal bandwidth[9] is the inherent parasitic capacitance introduced by the photodetector. In order to achieve a wide bandwidth optical receiver，special methods must be used. In this design，the technique called inductive shunt peaking is utilized. We use active inductors instead of conventional bulky spiral inductors for two reasons：(1) Spiral inductors consume much area and their performance is much worse than out-of-chip inductors；(2) The inductance values of active inductors are quite small，usually below tens of nano-henries. The active inductors[10] are made up of an nMOS and a resistor and are configured as

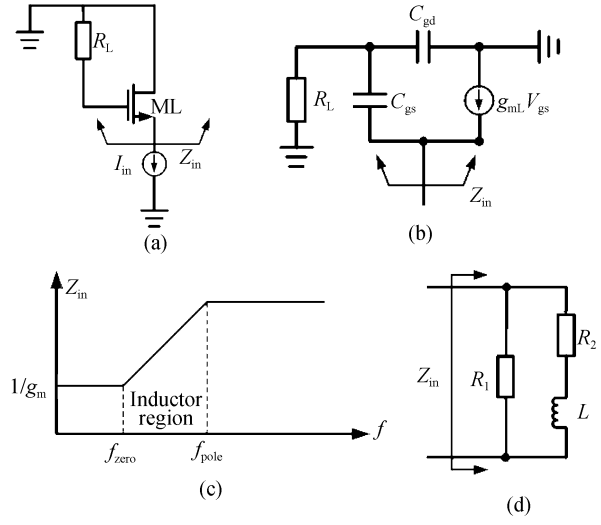

Fig. 4　Active inductor and the equivalent circuit

M2 + R_{L1}，M4 + R_{L2} in Fig. 3.

Figure 4 shows how the active inductor works. Figure 4 (b) is a small signal model of an active inductor. The input impedance Z_{in} can be approximated by

$$Z_{in} \approx \frac{1}{g_m} \times \frac{1 + sR_L C_{gs}}{1 + s\dfrac{1}{g_m} C_{gs}} \tag{1}$$

From Eq. (1) we can get f_{zero} and f_{pole} in Fig. 4(c). $f_{zero} = \dfrac{1}{R_L C_{gs}}$，$f_{pole} = \dfrac{g_m}{C_{gs}}$. For Z_{in} to behave as an inductor，$f_{zero} < f_{pole}$ should be satisfied as signified in Fig. 4(c)，or in another way，g_m should be greater than $1/R_s$. In the inductive region，Z_{in} can be modeled as an ideal inductor L in series with a passive resistor R_2 and with another resistor R_1 in parallel as shown in Fig. 4(d). The parameters in Fig. 4(d) can be calculated by the equations below：

$$R_1 \approx R_L，R_2 \approx \frac{1}{g_{mL} - 1/R_L}，L \approx \frac{R_L C_{gs}}{g_{mL} - 1/R_L} \tag{2}$$

The inductive region and the inductance can be adjusted by tuning the locations of the pole and zero. Figure 5 shows a comparison of 3dB bandwidth with and without active inductors. From it we can see，by the adoption of the active inductor，the −3dB bandwidth of one single channel of the 12-channel OEIC receiver can be extended from 800MHz to 1.25GHz.

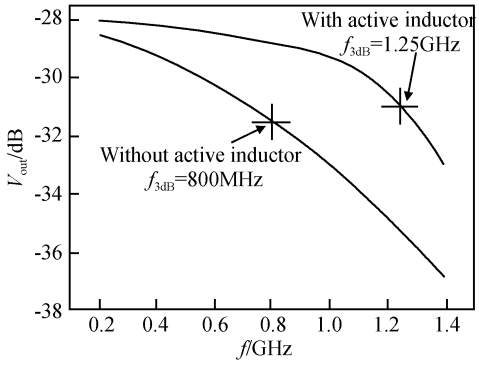

Fig. 5 Simulation results of OEIC receiver with and without active inductor

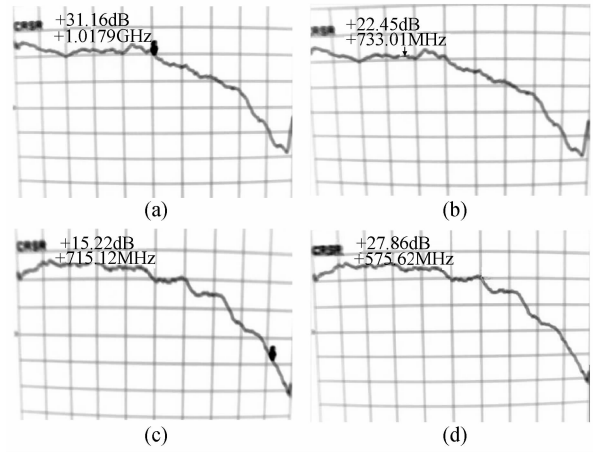

Fig. 7 Frequency response of the 1st, 2nd, 4th, and 6th channels as counted from left to right

5 Chip fabrication and measurement

This monolithically integrated 12-channel parallel CMOS OEIC receiver is implemented in CSMC (a foundry in Wuxi, China) 0.6μm standard CMOS technology. Figure 6 shows a chip photograph of the receiver. From the photograph, we can see that every channel has an independent power supply, as this is convenient for measuring every single channel separately. In practice, we connect all the power supplies together.

The chip was tested under -6dBm incident optical power at a wavelength of 850nm. The experimental system consists of a high speed optical transmitter model, NF1780 (New Focus) and a network analyzer, HP8757C. The frequency response of four typical channels of the 12-channel parallel CMOS OEIC receiver is shown in Fig. 7. Under ideal conditions, all 12 channels should have the same frequency response, but due to process deviations and interchannel crosstalk, there are visible differences from channel to channel. From Fig. 7 we can see that the channels on the edge of the chip have the best frequency response (about 1GHz) and the channels in the middle have the worst frequency response (only 575MHz). This is because of the fact that channels in the middle of chip suffered from more interchannel crosstalk than those on the edge. When the bit rate is 1.4 times the 3dB bandwidth, the single channel of the receiver can be operated at bit rates from 0.8 to 1.4Gb/s, and the average value is about 1.25Gb/s. Altogether the 12 channels can work at 15Gb/s.

6 Conclusions

In this paper, a 12-channel parallel CMOS OEIC receiver was introduced. The DPD structure can speed up the receiver but at the same time hinders responsivity. By the adoption of active inductors, the -3dB bandwidth of the receiver can be extended to a higher level. The chip was fabricated using a CSMC 0.6μm standard CMOS process. From the measured results we can see that single channel of the receiver is able to work at bit rates of 0.8 $\sim$ 1.4Gb/s. Altogether the 12-channel OEIC receiver chip can be operated at 15Gb/s. The simulated and measured results show that the achieved 12-channel CMOS OEIC receiver has the merits of high speed, low cost and monolithic integration, and can be used in ultra high speed parallel optoelectronic communication systems.

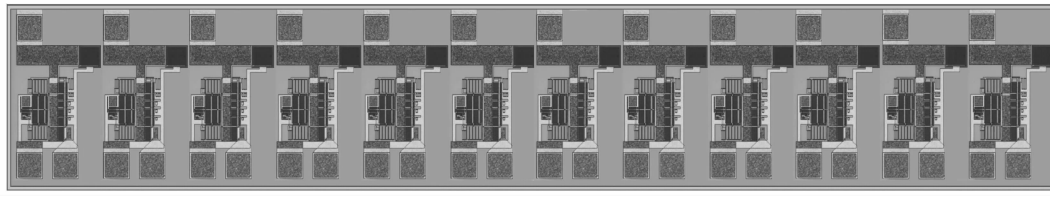

Fig. 6 Chip photo of the 12-channels parallel CMOS OEIC receiver

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高速 12 路并行 CMOS 单片光电集成接收机设计与实现*

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摘要：设计并实现了一个高速 12 路并行 CMOS 单片光电集成接收机.其每一路都包括一个光探测器、一个跨阻放大器以及后续放大电路.双光电二极管(DPD)结构可以提高接收机速度,但同时降低了响应度.在跨阻放大器电路中采用有源电感来展宽 -3dB 带宽.通过无锡上华(CSMC)0.6μm CMOS 工艺流片并对芯片进行了测试.测试结果显示该接收机单路传输比特率可达 0.8～1.4Gb/s,总的 12 路可传输 15Gb/s 数据.

关键词：CMOS；光电集成；并行接收机；高速

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