A Three-Stage Operational Amplifier for a Wide Range of Capacitive Loads

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Abstract: This paper presents a three-stage CMOS operational amplifier (opamp) that combines accuracy with stability for a wide range of capacitive loads. A so-called quenching capacitor is added to a multipath nested Miller compensation (MNMC) topology to obtain stability for a wide range of capacitive loads. Theoretical analysis and mathematical formulas are provided to prove the improvement in stability. A prototype of this frequency compensation scheme is implemented in a 0.7μm CMOS process. Measurements show that the amplifier can drive capacitive loads ranging from 100pF to 100μF with a gain of 90dB and a minimum phase margin of 26°. The amplifier has a unity-gain bandwidth of 1MHz for a 100pF capacitive load. It employs a quenching capacitance of 18pF.

Key words: operational amplifier; frequency compensation; phase margin; capacitive loads
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1 Introduction

The motivation for developing an operational amplifier that is stable for a wide range of capacitive loads is the increasing demand for such amplifiers in power management and audio applications, e.g., in low-dropout regulators (LDO), or in amplifiers that must drive predominantly capacitive loads such as piezoelectric or ceramic loudspeakers. However, undetermined capacitive loading conditions and stability requirements limit the DC loop gain. The problem of driving variable capacitive loads has led to the evolution of numerous frequency compensation techniques[1~6]. Unfortunately, they are not suitable for a wide range of capacitive loads. A two-stage Miller compensated (MC) amplifier is stable for a wide range of capacitive loads only when the gain of the input stage is less than 20dB[7].

In this paper, we propose a three-stage operational amplifier with quenched multipath nested Miller compensation (QMNMC), which is stable for a wide range of capacitive loads and the gain of the input stage is an order of magnitude larger than that of the two-stage MC amplifier. We also give the transfer function, stability criteria, and a mathematical analysis of the proposed three-stage QMNMC amplifier. Moreover, we present the design considerations, circuit implementation and the measurements of the proposed three-stage amplifier.

2 Two-stage Miller compensation amplifier

As shown in Fig. 1, a two-stage Miller compensated amplifier can be made unconditionally stable for a wide range of capacitive loads as long as the gain of the input stage is limited[7]. In this topology, there are two left half plane (LHP) poles and one right half plane (RHP) zero. The RHP zero is negligible under the assumption that g_{m2} is much smaller than g_{m1}. When $C_L \ll R_1 g_{m1} \times C_{M1}$, the nondominant pole shifts to lower frequencies with the increase of C_L, while the dominant pole is fixed. Therefore, the two poles move closer to each other and the phase margin is reduced to a certain minimum value. When $C_L \gg R_1 g_{m1} C_{M1}$, the frequency of the dominant pole decreases with the further increase of C_L, while the nondominant pole becomes fixed. Therefore, the distance between these two poles increases and the phase margin is improved. This trend is evident in

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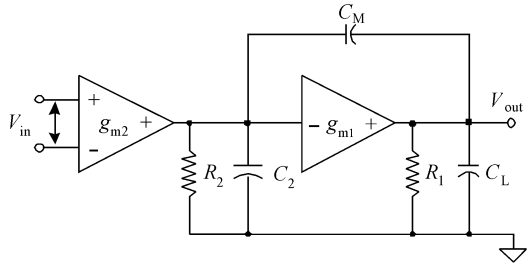

Fig. 1 Two-stage amplifier with Miller compensation

the simulated plot of phase margin (PM) versus load capacitance shown in Fig. 2.

3 Proposed three-stage quenched multipath nested Miller compensation

In an MNMC amplifier (Fig. 3), a high frequency (HF) path g_{m3HF} directly drives the output stage by bypassing an intermediate stage g_{m2}[8]. If the gain of the intermediate stage is limited, the two-stage path can take over from the three-stage path at high frequencies[9]. Therefore, the MNMC structure combines the high gain of the three-stage nested Miller compensation (NMC) at low frequencies and the good stability of the two-stage Miller compensation (MC) at high frequencies. Unfortunately, the amplifier is not stable for all capacitive loads even if the gain of the intermediate stage is reduced. A quenched MNMC (QMNMC) structure is illustrated in Fig. 3. It uses a parallel quenching capacitor C_Q at the output of the input stage of the LF path that lowers the frequency at which the two-stage HF path takes over the three-stage LF path.

In order to investigate the stability of the QMNMC amplifier, the open loop small-signal transfer function of the Fig. 3 topology is calculat-

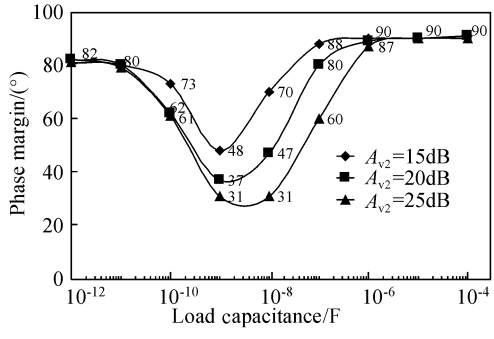

Fig. 2 Simulation of PM versus C_L for different input-stage gains

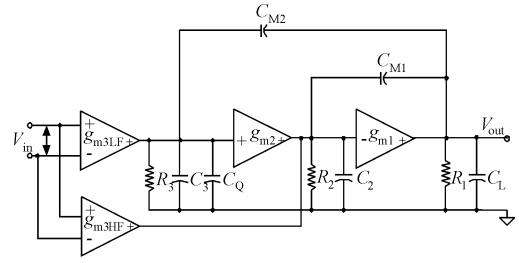

Fig. 3 Block diagram of a three-stage QMNMC amplifier

ed with the following assumptions:

(1) The gain bandwidth product (GBW) of the HF path is equal to the LF path. The LF path smoothly hands over to the HF path without showing pole zero doublets.

(2) The parasitic capacitances C_2, C_3 are much smaller than the Miller capacitances C_{M1}, C_{M2}, and load capacitance C_L.

The transfer function is given by Eq. (3), where $A_{v(QMNMC)}(0) = A_{dc} = g_{m3}R_3g_{m2}R_2g_{m1}R_1$, is the DC gain of the amplifier.

$$A_{v(QMNMC)}(s) = -A_{dc}\frac{N(s)}{D(s)} \approx -A_{dc}\Big[1+\frac{1}{g_{m2}R_3}+\Big(\frac{C_Q+C_M}{g_{m2}}-\frac{C_M}{g_{m1}}-\frac{C_M}{g_{m1}g_{m2}R_3}-\frac{C_M}{g_{m1}g_{m2}R_2}\Big)s-\frac{C_M(C_Q+2C_M)}{g_{m1}g_{m2}}s^2\Big]\Big/\{1+s[R_1C_L+R_1g_{m1}C_M(R_2+R_3R_2g_{m2})]+s^2[(R_3R_2R_1g_{m1}C_M+R_3R_1C_L)(C_M+C_Q)+R_1R_2C_LC_M]+s^3R_1R_2R_3C_LC_M(C_M+C_Q)\} \quad (1)$$

From the transfer function, the amplifier has two zeros and three poles. The denominator $D(s)$ is a third-order polynomial, which generates three LHP poles. The locations of the three poles for different load capacitances are as given in Table 1.

According to the formulas in Table 1, if $C_L \ll R_1g_{m1}C_{M1}$, increasing C_L causes the second nondominant pole p_3 to shift lower in frequency towards the first nondominant pole p_2. The Miller compensation (C_{M1}) fails to split apart p_2 and p_3, while the dominant pole is fixed. Therefore, the phase margin is deteriorated in this situation and reaches a local minimum PM_{min1}. When $R_2g_{m2} \times R_1g_{m1}C_{M2} \gg C_L \gg R_1g_{m1}C_{M1}$, increasing C_L further causes the nondominant pole p_2 to move lower in frequency towards the dominant pole p_1. The Miller compensation (C_{M2}) fails to split apart p_1 and p_2, while the second nondominant pole p_3 is

Table 1　Location of three poles

	$C_L \ll R_1 g_{m1} C_{M1}$	$R_1 R_2 g_{m1} g_{m2} C_{M2} \gg C_L \gg R_1 g_{m1} C_{M1}$	$C_L \gg R_1 R_2 g_{m1} g_{m2} C_{M2}$
p_1	$\frac{1}{R_3 R_2 g_{m2} R_1 g_{m1} C_M}$	$\frac{1}{R_3 R_2 g_{m2} R_1 g_{m1} C_M}$	$\frac{1}{R_1 C_L}$
p_2	$\frac{g_{m2}}{C_Q + C_M}$	$\frac{g_{m1} g_{m2} R_2 R_3 C_M}{C_L[R_2 C_M + R_3(C_M + C_Q)]}$	$\frac{1}{R_2 C_M + R_3(C_M + C_Q)}$
p_3	$\frac{g_{m1}(C_M + C_Q)}{C_L(C_M + C_Q) + C_M C_Q}$	$\frac{R_2 C_M + R_3(C_M + C_Q)}{R_2 R_3 C_M(C_M + C_Q)}$	$\frac{R_2 C_M + R_3(C_M + C_Q)}{R_2 R_3 C_M(C_M + C_Q)}$

fixed. Therefore, the phase margin deteriorates again and reaches another local minimum PM_{min2}. When $C_L \gg R_2 g_{m2} R_1 g_{m1} C_{M2}$, increasing C_L causes the frequency of the dominant pole p_1 to decrease while the nondominant poles p_2 and p_3 remain fixed. The phase margin is improved further because the distance between p_1 and p_2 increases. This is proven by the concave curves indicated in Fig. 4, which are more obvious with larger quenching capacitance. However, if the quenching capacitance is too large, it does not benefit the worse case phase margin very much. Therefore, a quenching capacitance that is twice the Miller capacitance is chosen because of the flat phase margin curve for a wide range of capacitive loads. It appears that as long as the nondominant pole p_3 is located at a higher frequency than the unity gain frequency, PM_{min1} causes no problems while PM_{min2} is the minimum phase margin for the whole range of capacitive loads. Since the numerator $N(s)$ is a second order polynomial, two zeros are created. The numerator $N(s)$ can be factorized as follows:

$$N(s) = n(s - z_1)(s - z_2) = n[s^2 - (z_1 + z_2)s + z_1 z_2] \quad (2)$$

where $z_1 + z_2 = -\omega_{LHP} + \omega_{RHP} \approx \frac{C_Q + C_M}{C_Q + 2C_M} \times \frac{g_{m1}}{C_M}$,

$z_1 z_2 = -\omega_{LHP}\omega_{RHP} \approx -\frac{g_{m1} g_{m2}}{C_M(C_Q + 2C_M)}$.

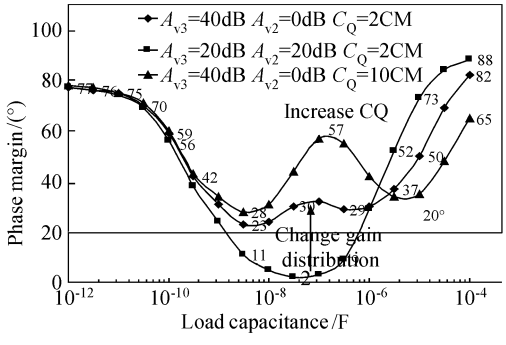

Fig. 4　Simulation of PM versus C_L for different gain distributions and C_Q

Because the signs of the s and s^2 terms are opposite, the RHP zero is located at a higher frequency than the LHP zero ($\omega_{RHP} > \omega_{LHP}$), and so the LHP zero is dominant. The LHP zero increases the phase margin. According to Eq. (2), the contribution to the phase margin of the two zeros is given by

$$PM_{zeros} = \tan^{-1}\left\{\tan\left[\tan^{-1}\left(-\frac{GBW}{\omega_{RHP}}\right) + \tan^{-1}\left(\frac{GBW}{\omega_{LHP}}\right)\right]\right\} \approx \tan^{-1}\left\{GBW \times \frac{C_Q + C_M}{C_Q + 2C_M} \times \frac{g_{m1}}{C_M} \Big/ \left[GBW^2 + \frac{g_{m1} g_{m2}}{C_M(C_Q + 2C_M)}\right]\right\} \quad (3)$$

The phase margin contributed by the two zeros is limited to $\tan^{-1}\left(GBW \times \frac{g_{m1}}{2C_M} \Big/ \left(GBW^2 + \frac{g_{m1} g_{m2}}{2C_M^2}\right)\right)$ without the quenching capacitor C_Q. Equation (3) shows that the phase margin PM_{zeros} improves monotonically as the value of the quenching capacitance C_Q is increased.

4　Circuit design and measurement results

To confirm the theoretical analysis above, a prototype of the three-stage QMNMC amplifier is implemented in a 0.7μm CMOS process. The circuit schematic is shown in Fig. 6. The transistors M301, M302 and M303, M304 form two identical input transconductance stages $g_{m3HF} = g_{m3LF} = g_{m3}$, while M311 ~ M318 and M211 ~ M218 form the folded cascode branches of the LF and HF paths, respectively. The intermediate stage of the LF path and the input stage of the HF path share the same load branch M211 ~ M218. A simple class-A output stage M101 is biased at a relatively large current of 100μA to achieve good large-signal performance and to avoid limiting the overall slew rate. Together with the transconductances g_{m3} and g_{m2}, resistors R_3 and R_2 are used to define the

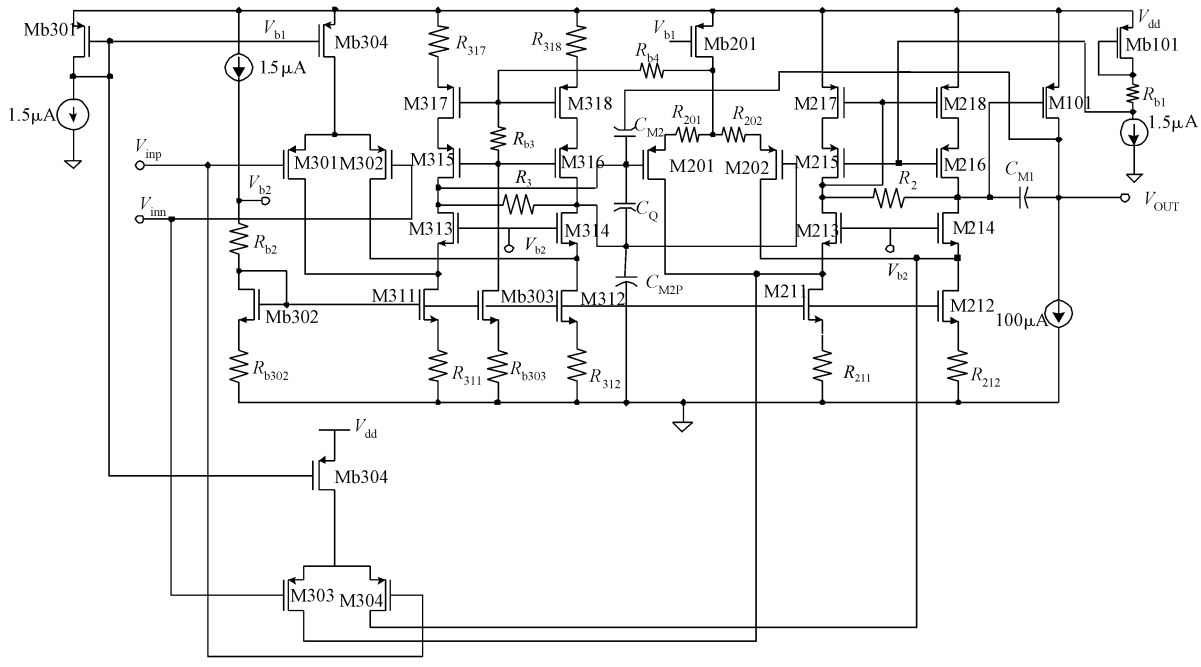

Fig. 5 Schematic of the proposed QMNMC amplifier

gain of the input and intermediate stage. Because of the differential configuration of the LF path input stage, capacitor C_{M2P} and C_{M2} together with C_{M1} form a nested Miller compensation network. The quenching capacitor C_Q is located between the differential output nodes to reduce the HF gain of the intermediate stage of the LF path. It is split into two equal parts that are laid out in opposite directions in order to eliminate the parasitic capacitance between n-well and substrate.

The prototype of the amplifier is implemented in a CMOS 0.7μm process. The chip area, including the pad ring, is 1335μm×1276μm. The microphotography of the chip is shown in Fig. 6. The voltage gain as a function of the frequency (bode plot) can be measured with a network analyzer (HP4395A) with active probes (C_{in}<3pF). However, the network analyzer has a limited output voltage (7V). The input offset voltage amplified by the large open loop gain may blow up the network analyzer. Therefore, the input signal V_S is damped by a resistor divider to $10/(10+12000)\approx -61.59$dB as shown in Fig. 7. The DC gain of the

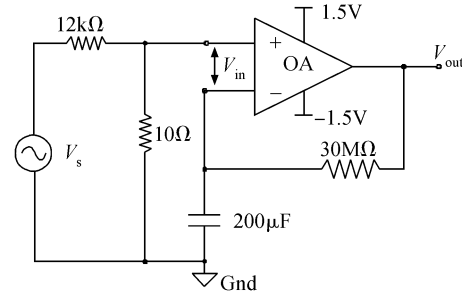

Fig. 7 Measurement setup for frequency response

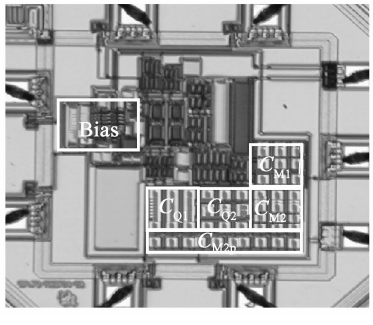

Fig. 6 Microphotograph of the prototype chip

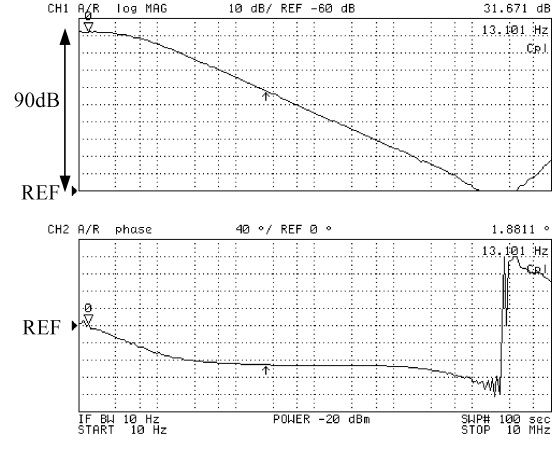

Fig. 8 Measurement result of the open loop gain

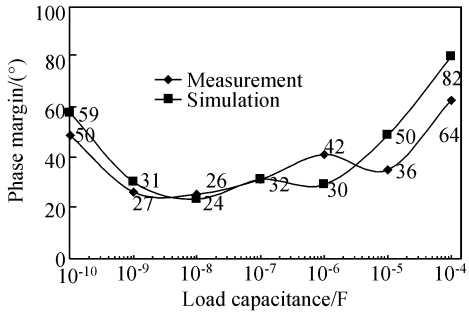

Fig. 9　Phase margin of measurement results versus simulation results

operational amplifier is the read out value from the network analyzer in Fig. 8 added by this damping value. It is more than 90dB. The measurement results of the phase margin are compared with simulation results in Fig. 9.

5　Conclusions

A three-stage amplifier with (QMNMC) is suitable for driving a wide range of undetermined capacitive loads. An 18pF quenching capacitor is used to compensate the amplifier to meet this stability requirement. The QMNMC three-stage amplifier described in this paper can provide up to a 20dB greater gain at the input stage than a MC two-stage amplifier under a wide range of capacitive load conditions. The measurement results show that the amplifier has a minimum phase margin of 26° for the capacitive loads ranging from 100pF to 100μF.

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适合宽范围电容负载的三级运放

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摘要： 结合精确度和稳定性的要求提出了一种适合宽范围电容负载的 CMOS 运放. 在多径嵌套式密勒补偿结构中加入一个抑制电容得到适合各种电容负载的稳定性. 为了证实稳定性的提高对该结构进行了理论分析并计算得出数学表达式. 基于这种新的频率补偿结构，利用 CMOS 0.7μm 工艺模型设计了样品芯片. 测试结果表明：该运放可以驱动从 100pF 到 100μF 负载电容，直流增益为 90dB，最小相位裕度为 26°；该运放在 100pF 负载情况下单位增益带宽为 1MHz，使用抑制电容仅为 18pF.

关键词： 放大器；频率补偿；相位裕度；电容负载
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