A Low-Voltage, Low-Power CMOS High Dynamic Range dB-Linear VGA for Super Heterodyne Receivers

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Abstract: This paper presents a low-voltage low-power variable gain amplifier, which is applied in the automatic gain control loop of a super heterodyne receiver. Six stages are cascaded to provide an 81dB digitally controlled gain range in a 3dB step. The gain step error is less than 0.5dB. It operates at an intermediate frequency of 300kHz, and the power consumption is 1.35mW from a 1.8V supply. The prototype chip is implemented in a TSMC's 0.18μm 1P6M CMOS process and occupies approximately 0.24mm^2. It is very suitable for portable wireless communication systems. The measurement results agree well with the system requirements.

Key words: variable gain amplifier; low voltage; low power; super heterodyne receiver; CMOS RF integrated circuits

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1 Introduction

Super heterodyne receivers are very suitable for wireless data transmission over short distances, like those in the industrial, scientific and medical (ISM) band, because of their good sensitivity and selectivity, and they are especially suitable for battery-operated systems. However, more attention should be paid to the power losses in the circuit design. Variable gain amplifiers (VGA) are widely used in various applications such as high performance industrial systems and wireless communications. They are typically employed in a feedback loop to realize an automatic gain control (AGC) loop that is a key element in any portable communication system, including a super heterodyne receiver. VGAs help to maximize the dynamic range of the overall system[1~3]. It is clear that a digitally controlled VGA can simplify the interface circuitry between the analog and digital parts of the receiver.

Over the years, many techniques have been proposed for VGAs. Among them, there are two kinds of circuit implementations for VGA functions. One is the closed-loop system. By using a negative feedback method, it can obtain precise gain setting and higher signal linearity[3,4]. However, operational stability becomes a big problem, which complicates circuit design. Moreover, since stability is always an important concern in this type of amplifier, the bandwidth is smaller. The other kind of circuit used for VGA functions is the open-loop structure, which achieves gain control by varying the transconductance and load value of an amplifier stage or by a series of switchable gain stages[5,6]. The bandwidth of this kind of structure is wide.

With the increasing demands for lower power dissipation and the downsizing to wireless communication systems, it is necessary to investigate VGA structures for low-voltage, low-power wireless architectures. Meanwhile, the design of a VGA with high linearity and wide bandwidth is also a big challenge. In general, the design of a VGA needs to meet requirements in gain, bandwidth and linearity under power consumption and die area constraints.

In this paper, a simple structure, low-voltage, low-power VGA with high selectivity and high sensitivity used in super heterodyne receiver is proposed. It has such features as low power dissipation, wideband, high dynamic range and good linearity for its cascade structure and constant current bias scheme. It operates in a 1.8V supply that offers a programmable gain from -9 to 72dB

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ranges in a 3dB step. The gain step error is less than 0.5dB. It is fabricated with TSMC's 0.18μm 1P6M CMOS technology. It occupies only 0.24mm^2 and the typical power dissipation is less than 1.35mW. The small standby power consumption and chip area make it an ideal choice for portable applications.

2 VGA design

2.1 Basic structure of the VGA

The specifications of the VGA were derived from the requirements of the AGC in the super heterodyne receiver. The specification for the linearity of the VGA is high to maintain good overall system linearity. Moreover，a VGA with an exponential gain control characteristic is desired in applications where wide gain control range is required. The maximum and the minimum gains of the VGA are 72 and −9dB，respectively when the frequency of the signal is 300kHz.

The proposed VGA consists of six amplifier stages cascaded to satisfy the specifications. The first，the third，and the fifth stages are amplifiers. The second and the fourth stages are attenuators. Finally，in the sixth stage，a buffer is used to eliminate the DC offset and provide exact differential signals to the analog-to-digital converter (ADC) following the receiver. The gain of the VGA can be varied from −9 to 72dB in a 3dB step with different stage gain combinations. A pseudo-differential amplifier is employed to achieve good linearity and low power consumption. The input impedance of the amplifier is high enough to dispense with extra driving buffers. The proposed VGA has such features as low voltage，low power，a high dynamic range，and good linearity for its cascade structure and constant current bias scheme.

2.2 Amplifier in VGA

As mentioned above，the first，the third，and the fifth stages are amplifiers. A differential circuit topology is preferred to a crosstalk perspective when the VGA is combined with an ADC. In a low power design，the power consumption is a primary design consideration. The power consumption of the fully differential degeneration amplifier (FDDA)[7] is low for its simplicity in structure. In addition，it can also provide good linearity and high precision gain steps under a low supply voltage. Thus，the gain block based on a fully differential degeneration amplifier is used. The basic structure of FDDA is shown in Fig. 1. The VGA gain can be programmed by changing the ratio of the passive elements. The gain of the amplifier is：

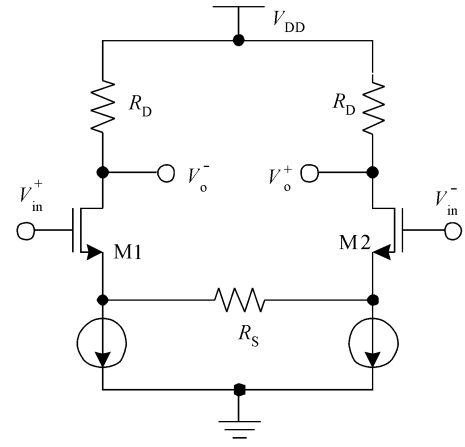


Fig. 1　Basic structure of the full differential degeneration amplifier

$$\text{Gain} = R_D g_{mdiff} = \frac{R_D}{\frac{1}{2}R_S + \frac{1}{g_{m1}}} \tag{1}$$

where g_{mdiff} is the equivalent transconductance of the circuit，g_{m1} is the transconductance of the input transistor M1，R_D is the load of the input transistor，and R_S is the degeneration resistance.

Two switches are used to change the values of R_D and R_S respectively. Thus，four different gains are achieved according to Eq. (1). However，in order to get high precision，it is desired that the gain is only a function of the ratio of resistance values. Therefore，g_{m1} should be large enough to minimize the contribution of g_{m1} to the amplifier gain. In addition，a large g_{m1} is good for maintaining the precision of the steps. But a large I_{dc} may bring a large amount of high power dissipation because g_{m1} is in direct proportion to $\sqrt{I_{dc}}$. By numerous simulations and careful design，an optimized value of I_{dc} was obtained as a trade off between power consumption and step precision.

Even though the gain of the amplifier is relatively small，it is enough to satisfy the designed super heterodyne receiver system. Moreover，due to

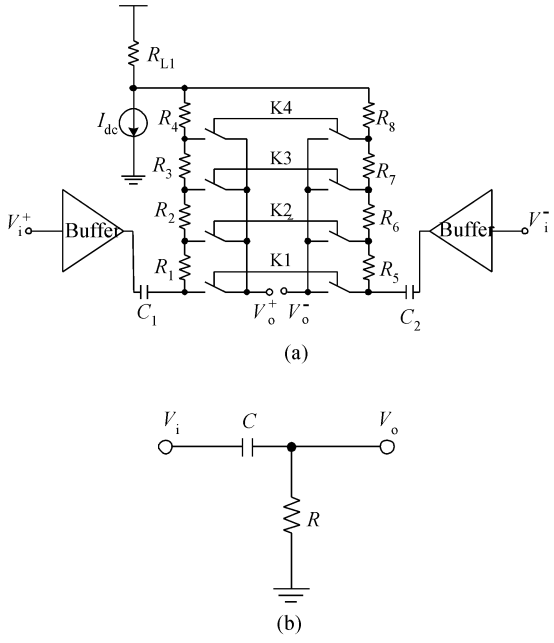


Fig. 2 (a) Structure of the attenuator in VGA; (b) Equivalent RC network in the attenuator

low amplifier gain, the output signals do not affect the DC operation point of the output terminal. Thus, it does not need the common mode feedback (CMFB) circuit in the amplifier stages. The simple architecture lowers the power consumption as well as the chip area.

2.3 Attenuator in VGA

In order to obtain a wide dynamic range and enhance the linearity of the VGA, two attenuators are used. They can be controlled externally to adjust the gain of the VGA. The structure of proposed attenuator is shown in Fig. 2 (a), which is composed of a buffer cell and a resistor ladder that attenuate the input signals. The buffer is utilized to drive block condensers C_1 and C_2. Resistor R_L and the independent current source I_{dc} are employed to provide the DC bias. The attenuator gain is digitally controlled using resistors R_1 to R_8 through the control switches K1 to K4.

The attenuator is located between two gain amplifiers and ensures the linearity of the VGA. In the attenuator, signals are coupled by the capacitor C. The DC voltages of the output signals are decided by the pull up resistance R_{L1} and the bias current I_{dc}. Therefore, the output DC voltages of the signals are exactly the same, which means that the output signals of the attenuator are exact differentials. Therefore, the differential signals can be easily applied to the following amplifiers.

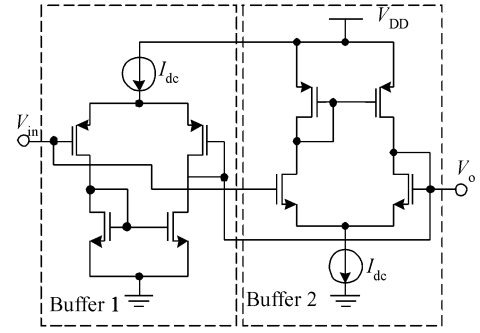


Fig. 3 Structure of the isolation buffer

The values of the resistors and the equivalent resistors of the switches are designed so that a dB-linear gain and a 3dB step are obtained in a fine gain setting. The gain of the attenuator is decided by the ratio of resistances, which can be controlled precisely in the CMOS process so the gains of the attenuator are very accurate and not sensitive to the outside environment.

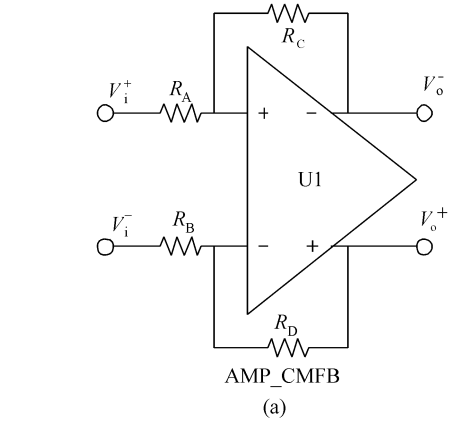
The high-pass −3dB corner of the VGA is determined by the pole point of the differential cascade amplifier. Normally, the cutoff frequency of the amplifier is high, so it is easy to meet the specifications of a high-pass −3dB point. The RC network in the attenuator, which is illustrated in Fig. 2 (b), is a high pass network. It determines the low-pass −3dB corner of the VGA.

V_o is denoted as follows:

$$V_o = V_i \frac{R}{R + \frac{1}{j\omega C}} = V_i \frac{j\omega RC}{j\omega RC + 1} \qquad (2)$$

The low-pass −3dB corner is $\omega_c = \frac{1}{RC}$. The values of the resistors and the capacitor are very important in meeting the bandwidth requirement. They are appropriately selected to ensure $\omega_c < \omega_{-3dB}$ (ω_{-3dB} is the low-pass −3dB corner). There are four different gains when one of the four switches is turned on.

Between every amplifier and attenuator proposed above, an isolation buffer is designed to improve the amplifier's driving capability. Two different unity-gain buffers are connected in parallel, as shown in Fig. 3. In buffer 2 the input signal is sent to the gate of nMOS, while in buffer 1, the input signal is sent to the gate of pMOS. When the DC voltage of the input signal is high, buffer 2



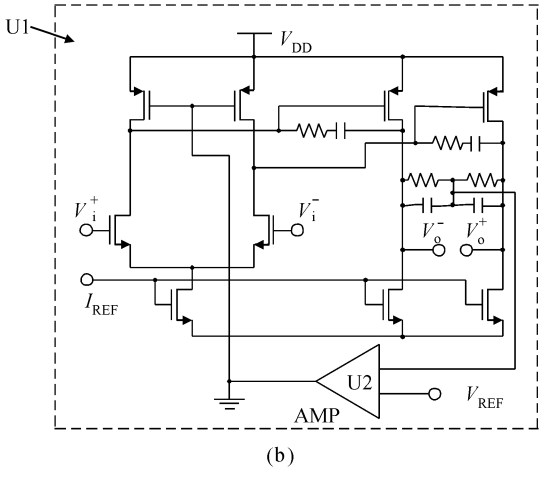


Fig. 4　(a) Output stage of the VGA; (b) Amplifier with CMFB circuit

works. Buffer 1 works under a low input DC voltage. This structure enhances the dynamic range of input signal common voltage.

2.4　Output stage

The output stage is shown in Fig. 4 (a). It consists of an amplifier U1 and several resistors. A buffer should be used to eliminate the DC offset of the differential node because the DC voltage of the input signals at V_i^+ and V_i^- in Fig. 4 (a) may not be identical due to the process variation. This variation affects the accuracy of the following ADC. In our design, U1 is designed as a CMFB structure to guarantee that the DC voltages of the differential output signals are equal.

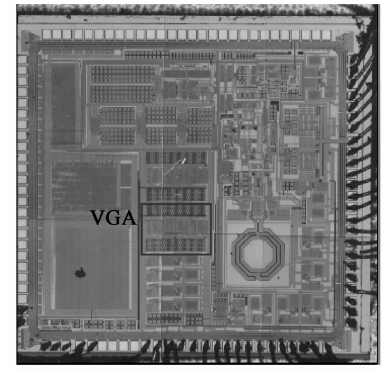


Fig. 5　Microphotograph of VGA in SOC

The structure of the amplifier U1 is shown in Fig. 4 (b) where a simple one-stage amplifier U2 is used to make the output DC voltage of the main amplifier and the reference V_{REF} identical. This structure ensures the variation of the DC voltage output is very small in order to satisfy the system requirement.

3　Implementation and measurement results

The proposed VGA was fabricated in a TSMC's 0.18μm CMOS process, and occupied 0.24mm^2 chip area. It operates at an IF of 300kHz in 81dB gain range with a 3dB step. The chip microphotograph, shown in Fig. 5, is a SOC that consists of a super heterodyne receiver, a transmitter, and a phase locked loop (PLL). The proposed VGA is one part of the super heterodyne receiver.

The specifications and measurement results are shown in Table 1.

Table 1　Specifications versus measurements

Parameter	Specification	Measured results	Unit
Supply current, I_{AVDD}, in power on	1000	750	μA
Supply current, I_{AVDD}, in power down	10	2	nA
Minimum VGA gain@300kHz	−9	−8.63	dB
Maximum VGA gain@300kHz	72	71.63	dB
1dB output compression point, 42dB gain setting	−15	−12.00	dBV
1dB input compression point, 42dB gain setting	−57	−55.62	dBV
High-pass −1dB corner, maximum gain setting	800	2400	kHz
High-pass −3dB corner, maximum gain setting	1300	4000	kHz
Low-pass −1dB corner, maximum gain setting	200	100	kHz
Low-pass −3dB corner, maximum gain setting	120	60	kHz

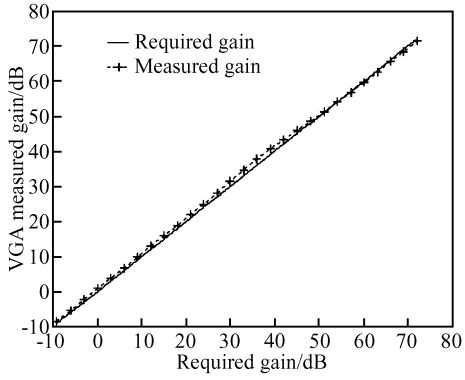


Fig. 6 Measurement results of VGA's gains

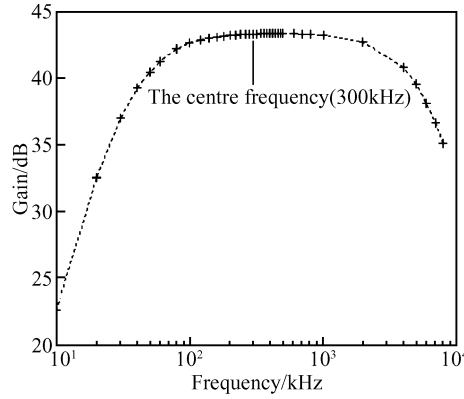


Fig. 8 Bandwidth curve of VGA

A large dynamic range with a precise gain step is obtained. Figure 6 shows that the test gains (from −9 to 72dB) meet the required index. The gains increase monotonously from the minimum gain to the maximum gain in a step of 3dB. The measurement results of the step errors are shown in Fig. 7. The maximum step error is less than 0.5dB. The gain errors come primarily from the finite transconductance of the input resistors. The total current consumption of the VGA is 0.75mA when the VGA works on a 1.8V power supply. Therefore, the total power consumption is only 1.35mW, which is far smaller than the predicted value. A good trade-off between the power consumption and the gain accuracy is achieved. From Fig. 8, we can see that the 3dB bandwidth of the VGA is approximately 4MHz over the entire gain range.

The 1dB compression point was measured to have a 42dB gain in the receiver, including low noise amplifier (LNA), mixer and filter. The results are shown in Fig. 9. The 1dB input compression point is −55.62dBV at a gain of 42dB, while the 1dB output compression point is −12dBV at a gain of 42dB. The test results show that the sensitivity of the receiver is −110dBm, meeting the specification. The test results also show that the VGA expands the dynamic range of the overall system.

We will now compare the proposed VGA with other recent designs that focus on low voltage operation. In Ref. [8], a VGA that exhibits a turning range of 84dB at the cost of higher power consumption of 5.4mW and the larger die area of 0.383mm^2 was reported. In Ref. [9], a VGA was reported to have a gain tuning range from −10 to 20dB and a power consumption of 1.35mW with a die area of 0.3mm^2. BiCMOS VGA with wide dynamic range was introduced in Ref. [10]. This circuit achieves a high operating frequency and wide dynamic range. But, it consumes a higher amount of power dissipation and is not compatible with standard CMOS technology. The measured results show that the structure of this work is suitable for the low power, high dynamic range applications for wireless systems.

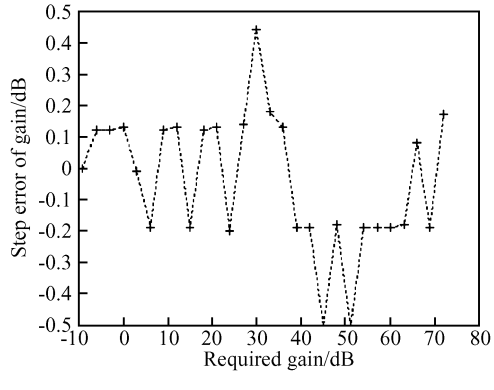


Fig. 7 Measurement results of gain step errors

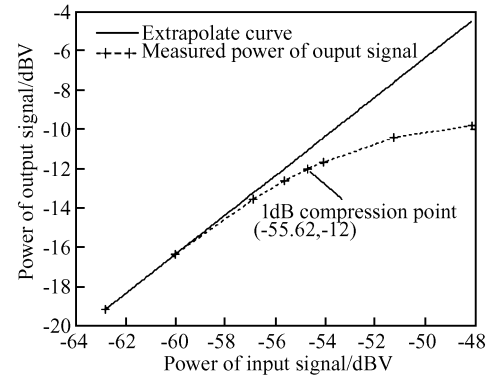


Fig. 9 1dB compression point of VGA

4 Conclusions

A fully differential VGA was designed for the super heterodyne receiver. The proposed VGA was characterized by a high dynamic range of gain，low-power consumption，small chip size，and controllable dynamic gain range. It was fabricated in 0.18μm CMOS technology and showed an 81dB range in a 3dB step with linearity error of less than 0.5dB. The range of gain variation can be controlled from −9 to 72dB. It operates at an IF frequency of 300kHz with less than 1.35mW from a 1.8V supply and occupies 0.24mm^2 of chip area. The bandwidth is approximately 4MHz. This new VGA can operate under low voltage and achieves low power consumption，which are widely useful in low-bit-rate ISM band wireless communications and short distance data exchange. Despite the poor rejection of strong spurious signals，this kind of receiver offers an excellent trade-off among simplicity，low power and overall performance of the receiver. The measurement results demonstrate the advantages of the proposed design in terms of gain step，gain error，dynamic range and linearity.

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用于超外差接收机的低压、低功耗高动态范围 CMOS 线性可变增益放大器

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摘要：针对超外差接收机的自动增益控制网络，设计了一种结构简单的低压、低功耗全差分可变增益放大器. 它由 6 级子电路级联而成，提供范围为 81dB 的数字控制增益，每一档为 3dB，增益误差小于 0.5dB. 该电路工作于中频 300kHz 下，工作电压为 1.8V，功耗仅为 1.35mW. 采用 TSMC 0.18μm 1P6M CMOS 工艺制造，芯片面积约为 0.24mm^2，低功耗及小芯片面积使其极适用于便携式通信系统的应用. 测试结果达到设计要求.

关键词：可变增益放大器；低压；低功耗；超外差接收机；CMOS 射频集成电路

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