

# Ti/4H-SiC Schottky Barrier Diodes with Field Plate and B<sup>+</sup> Implantation Edge Termination Technology\*

Chen Gang<sup>†</sup>, Li Zheyang, Bai Song, and Ren Chunjiang

(National Key Laboratory of Monolithic Integrated Circuits and Modules,  
Nanjing Electronic Devices Institute, Nanjing 210016, China)

**Abstract:** This paper describes the fabrication and electrical characteristics of Ti/4H-SiC Schottky barrier diodes (SBDs). The ideality factor  $n = 1.08$  and effective Schottky barrier height  $\phi = 1.05\text{eV}$  of the SBDs were measured with the method of forward current density-voltage ( $J$ - $V$ ). A low reverse leakage current below  $5.96 \times 10^{-3}\text{ A/cm}^2$  at a bias voltage of  $-1.1\text{ kV}$  was obtained. By using B<sup>+</sup> implantation, an amorphous layer as the edge termination was formed. We used the PECVD SiO<sub>2</sub> as the field plate dielectric. The SBDs have an on-state current density of  $430\text{ A/cm}^2$  at a forward voltage drop of about  $4\text{ V}$ . The specific on-resistance  $R_{\text{on}}$  was found to be  $6.77\text{ m}\Omega \cdot \text{cm}^2$ .

**Key words:** 4H-SiC; Schottky barrier; ideal factor; barrier height; implantation

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## 1 Introduction

Silicon carbide (SiC) has received remarkable attention during the last decade as a promising device material for high temperature, high frequency, and high power device applications due to its high thermal conductivity and high critical field for breakdown. It exhibits higher thermal conductivity (3~13 times), critical electric field (4~20 times), and saturated carrier velocity (2~2.5 times) than conventional semiconductor materials such as silicon and gallium arsenide<sup>[1~3]</sup>. As an example, Si SBDs with blocking voltage above 100V are not used due to their excessive reverse leakage currents and limited forward conduction current-handling capability. SiC technology has made tremendous strides in the last several years. In power conversion applications, the opportunity to use high voltage Schottky rectifiers, whose breakdown voltages are higher than 300V with low series resistance, can be investigated<sup>[4]</sup>.

Many authors have investigated the properties of SiC Schottky rectifiers, first on 3C-SiC, then on 6H-SiC, and more recently on 4H-SiC.

Wang *et al.*<sup>[5]</sup> fabricated a Ti/6H-SiC SBD with  $V_B = 800\text{ V}$ . Sun *et al.*<sup>[6]</sup> fabricated a Ti/4H-SiC SBD with a  $32\mu\text{m}$ -thick epilayer and  $(2\sim5) \times 10^{15}\text{ cm}^{-3}$  carrier density with a blocking voltage of over 1kV. By using high-quality epilayers at a low donor concentration of  $5.8 \times 10^{15}\text{ cm}^{-3}$  and a relatively small thickness of  $9.6\mu\text{m}$ , a high-blocking voltage of over 1.1kV was obtained successfully by Kimoto *et al.*<sup>[7]</sup>. In 2003, Cree broadened its SiC Schottky rectifier product family to include 1.2kV devices.

In this paper, we report a high-voltage ( $> 1.1\text{ kV}$ ) Ti/4H-SiC SBD fabricated on  $12\mu\text{m}$ -thick 4H-SiC epilayer with B<sup>+</sup> implantation edge termination and field plate technology.

## 2 Experiment

The SiC SBDs were fabricated at the National Key Laboratory of Monolithic Integrated Circuits and Modules, using 4H-SiC wafers purchased from CREE and epitaxial layers provided by CETC55. The active layer doping level and thickness were  $N_d = 3.5 \times 10^{15}\text{ cm}^{-3}$  and  $d = 12\mu\text{m}$ , respectively.

The SiC wafer underwent a typical cleaning

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<sup>†</sup> Corresponding author. Email: steelchg@163.com

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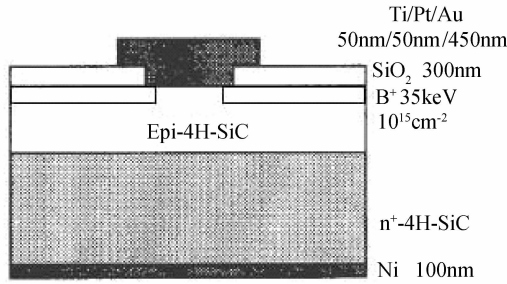


Fig.1 Schematic cross-sectional view of the Ti/4H-SiC SBD

procedure. After cleaning the sample, the processes began with the formation of the mark. Then we formed the edge termination by using the  $B^+$  implantation with an energy of 35keV and a dose of  $1 \times 10^{15} \text{ cm}^{-2}$ . As the field plate, the 300nm  $\text{SiO}_2$  was deposited by PECVD. Then the large area Nickel back-side ohmic contact was evaporated and annealed in  $\text{N}_2$  atmosphere at  $1000^\circ\text{C}$  for 10min. The  $\text{SiO}_2$  layer was removed using 1/10  $\text{HF}/\text{H}_2\text{O}$  etchant. Circular Ti Schottky contacts with diameters of  $310\mu\text{m}$  were evaporated. A schematic of the completed device is shown in Fig.1.

Forward  $I$ - $V$  measurements were performed in the range of  $10^{-12} \sim 1\text{A}$  using a Keithley SCS-4200. Reverse  $I$ - $V$  measurements were performed in the voltage range of  $0 \sim 2000\text{V}$  using a Tektronix 370A semiconductor parameter analyzer.

### 3 Results and discussion

Several Ti/4H-SiC SBDs were investigated in the direct voltage range of  $0 \sim 1\text{V}$ . Most of the SBDs show good agreement with the thermionic current model. The  $I$ - $V$  relationship under thermionic emission theory is given by<sup>[8]</sup>

$$J = J_s [\exp(qV/nkT) - 1] \quad (1)$$

and

$$J_s = A^{**} T^2 \exp(-q\phi/kT) \quad (2)$$

Here,  $J$  is the current density,  $n$  is the ideality factor,  $\phi$  is the Schottky barrier height, and  $A^{**}$  is the effective area-Richardson's constant.  $R_{on}$  is the series resistance. If the applied voltage  $V$  is much larger than  $kT/q$ , then the exponential term in the above equation dominates, and  $J$  can be approximated as

$$J = J_s \exp(qV/nkT) \quad (3)$$

Then we can obtain the  $n$  and  $\phi$  from the equa-

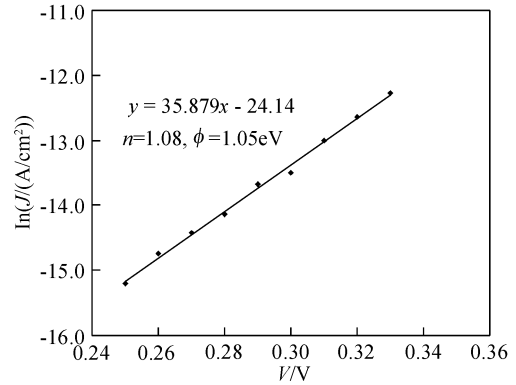


Fig.2 Ti/4H-SiC SBD forward  $\ln J$ - $V$  curve

tions:

$$\frac{1}{n} = \frac{kT}{q} \times \frac{d(\ln J)}{dV} \quad (4)$$

$$\phi = \frac{\ln A^{**} T^2 - \ln J_s}{q/kT} \quad (5)$$

$J_s$  can be measured by extrapolating the linear region of the  $\ln J$  versus  $V$  plot to  $V=0$ .

The  $\ln J$ - $V$  characteristics of the Ti/4H-SiC SBDs at room temperature are shown in Fig.2.

The ideality factor obtained from the slope of the forward  $\ln J$ - $V$  plot for the Ti/4H-SiC SBD was 1.08, and the Schottky barrier height calculated using the theoretically predicted value of the Richardson constant ( $150\text{A}/(\text{cm}^2 \cdot \text{K}^2)$ )<sup>[9]</sup>, was found to be 1.05eV.

The measured forward current-voltage ( $I$ - $V$ ) characteristics of a typical SBD at a room temperature are shown in Fig.3.

We can obtain the series or specific on-resistance  $R_{on}$  to be  $6.77\text{m}\Omega \cdot \text{cm}^2$ . As we can see from Fig.3, the deviation from linearity at a high forward current is due to the series resistance associated with the ohmic contact and body resistance. The lower the value of  $R_{on}$  is, the more effective are the ohmic contact and body resistance.

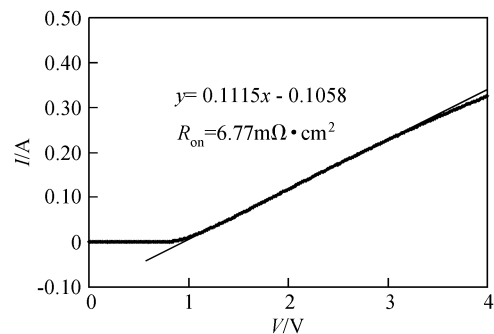


Fig.3 Forward Ti/4H-SiC SBD  $I$ - $V$  curve

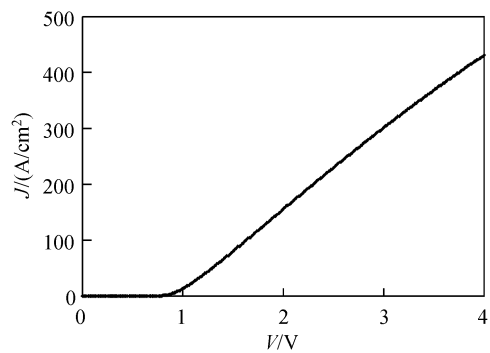


Fig.4    Forward Ti/4H-SiC SBD *J-V* curve

Figure 4 shows the forward *J-V* characteristics of the Ti/4H-SiC SBD. We can find that the SBDs have a current density of 430A/cm<sup>2</sup> at a forward voltage drop of 4V.

The room temperature forward and reverse *I-V* characteristics of the Ti/4H-SiC SBD obtained on a 12μm-thick n-type 4H-SiC epilayer grown by CETC55 are plotted in Fig.5.

From Fig.5, the Ti/4H-SiC SBD rectification ratio of forward to reverse (defined at ±1V) is over 10<sup>11</sup> at a room temperature.

The blocking voltage is more than 1.1kV. A low reverse leakage current below 5.96 × 10<sup>-3</sup> A/cm<sup>2</sup> at the bias voltage of -1.1kV has been obtained. A lower leakage current and higher blocking voltage could be realized by high-quality CVD-grown SiC layers and the optimized edge termination structure.

4    Conclusions

In summary, we have fabricated high performance Ti/4H-SiC SBDs on 12μm epilayer SiC

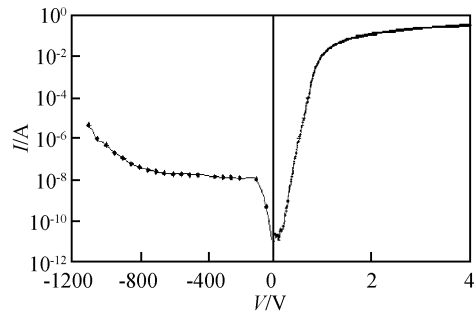


Fig.5    Forward and reverse Ti/4H-SiC SBD *I-V* curves

wafer. The breakdown voltage is measured to be higher than 1.1kV. At room temperature, the ideality factor and barrier height are 1.08 and 1.05eV, respectively. The series resistance *R*<sub>on</sub> is 6.77mΩ · cm<sup>2</sup>. A low reverse leakage current below 10<sup>-3</sup> A/cm<sup>2</sup> is obtained at the bias voltage of -1.1kV.

The 4.5kV SiC Schottky diodes were fabricated at CNM using a process technology developed in the framework of the ESCAPEE project<sup>[10]</sup>. In the next step, we may increase the SiC epilayer thickness and PECVD SiO<sub>2</sub> thickness. Then through changes in SiC SBD process technology we will further improve the performance of the SiC SBDs.

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## 采用场板和 $B^+$ 离子注入边缘终端技术的 Ti/4H-SiC 肖特基势垒二极管\*

陈 刚<sup>†</sup> 李哲洋 柏 松 任春江

(南京电子器件研究所单片集成电路与模块国家级重点实验室, 南京 210016)

**摘要:** 采用自主外延的 4H-SiC 外延片, 利用 PECVD 生长的  $\text{SiO}_2$  做场板介质,  $B^+$  离子注入边缘终端技术, 制造了 Ti/4H-SiC 肖特基势垒二极管. 测试结果表明, Ti/4H-SiC 肖特基势垒二极管的理想因子  $n = 1.08$ , 势垒高度  $\varphi_b = 1.05\text{eV}$ , 串联电阻为  $6.77\text{m}\Omega \cdot \text{cm}^2$ , 正向电压为 4V 时, 电流密度达到  $430\text{A}/\text{cm}^2$ . 反向击穿电压大于 1.1kV, 室温下, 反向电压为 1.1kV 时, 反向漏电流为  $5.96 \times 10^{-3}\text{A}/\text{cm}^2$ .

**关键词:** 碳化硅; 肖特基势垒二极管; 理想因子; 势垒高度; 离子注入

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<sup>†</sup> 通信作者, Email: steelchg@163.com

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