A High Precision CMOS Opamp Suitable for ISFET Readout*

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Abstract: This paper presents a high precision CMOS opamp suitable for ISFET readout. The opamp is tailored to provide a constant bias condition for ISFET as part of the readout circuits and, hence, is compatible for single chip integration with the sensor. A continuous time auto-zero stabilization technique is studied and employed, with the aim of suppressing the low frequency noises, including the offset voltage, $1/f$ noise, and temperature drift. The design is based on a 0.35μm CMOS process. With a 3.3V power supply, it maintains a DC open loop gain of more than 100dB and an offset voltage of around 11μV, while the overall power dissipation is only 1.48mW. With this opamp, a pH microsensor is constructed, of which the functionality is verified by experimental tests.

Key words: high precision; auto-zero; operational amplifier; ISFET microsensor
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1 Introduction

Ion sensitive FET (ISFET) was originally invented by Bergveld in 1970[1]. Although initially developed for hydrogen ion detection, the ISFET has also been used for sensing other varieties of ions and more recently molecules in biomedical, agricultural, environmental, food-industrial and general analytical applications[2,3]. Currently, the compatibility with standard microelectronic fabrication processes and the possibility of developing intelligent ISFET-based micro-systems are being studied intensively[4].

The need for high precision detection becomes increasingly critical for various advanced and emerging biochemical applications[5,6]. A majority of the reported ISFET sensor systems adopt the differential structure to reject common mode interference as a way to increase precision[7,8]. However, for most of the biosensors, whose signals are slow and weak, effective reduction of the low frequency noise, such as the offset voltage, $1/f$ noise, and temperature drift, is the only way to increase the system resolution. In other precision sensing applications, chopper and auto-zero techniques are primarily used to meet such objectives [9,10]. Yet, so far, few ISFET sensors make use of them.

This paper presents a novel ISFET opamp with the capability of providing a constant bias condition for ISFET to realize the single chip integration of the sensor with the readout circuits. It also features the implementation of a continuous auto-zero stabilization architecture, giving rise to a more power efficient solution to low frequency noise cancellation due to its simplicity compared with the chopper architecture.

2 ISFET operation principles

Figure 1 shows the cross section of the microsensor structure fabricated with a CMOS compatible ISFET process. The transistor-sensing area over the bonding pad (the top metal layer) opening is interconnected by a metal line on the chip to the gate of the n-channel MOSFET. The poly-silicon gate and other metal layer are interconnected by many vias. This structure is similar to the 'sensitive layer/poly-silicon/gate oxide' structure.

The operation of this microsensor is based on the surface adsorption of charges from the solution under test in the solid-electrolyte interface[11], which is also part of the gate of the ISFET. As a result of this process, the threshold voltage of the ISFET is modula-

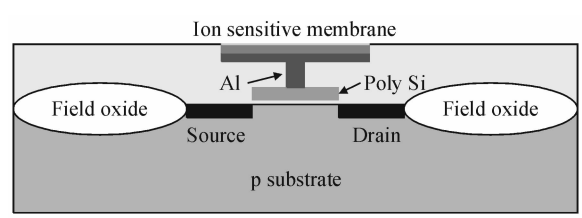

Fig. 1 Cross-section of ISFET structure

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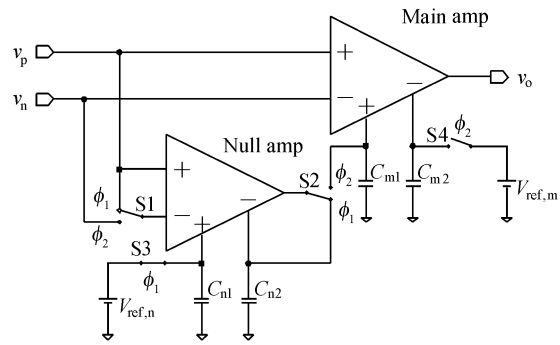

Fig. 2　Nest structure of a continuous time auto-zero opamp

ted. This combines the operational principles of low output impedance MOSFET and ion-sensitive electrodes (ISE). ISFET has a very fast response, high sensitivity, batch-processing capability, micro-sized features, and robust performance.

ISFET follows a current-voltage transfer function similar to that of the basic MOSFET. When biased in the saturation region, it can be written as

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - \frac{V_{DS}}{2} - f(c_{ion})\right) V_{DS}(1 + \lambda V_{DS}) \tag{1}$$

where $f(c_{ion})$ takes the place of V_{th} in the original transfer function, representing the modulation function of the threshold voltage related to the ion concentration. Then, if the bias conditions of the drain current I_{DS} and the drain-source voltage V_{DS} of the ISFET are held constant, the change of the ion concentration is reflected as the change of V_{GS}, which can be easily processed by the following readout circuits.

3　Continuous time auto-zero technique

Unlike the traditional discrete time auto-zero architecture where only one internal amplifier implements the sampling and the zeroing in alternate periods, our design of the continuous time auto-zero architecture comprises two internal amplifiers, the main amplifier and the null amplifier, which, together with switches and capacitors, constitute a nest structure, as shown in Fig. 2.

Each of these two internal amplifiers has two sets of differential inputs: a primary input $v_{i,p}$, and an auxiliary input $v_{i,a}$ as shown in Fig. 3. At each input exists an offset voltage due to the processing mismatch of the input transistors. Here we use $v_{os,p}$ and $v_{os,a}$ to denote the offsets of the primary and auxiliary inputs, respectively.

The small signal transfer function of such a dual-input amplifier can be modeled as

$$v_o = A_p(v_{i,p} + v_{os,p}) + A_a(v_{i,a} + v_{os,a}) \tag{2}$$

where A_p and A_a, respectively, represent the gains of

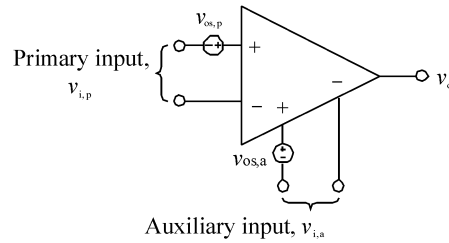

Fig. 3　Opamp with two sets of differential input pairs

the primary input signal and the auxiliary input signal, while v_o denotes the output.

The incoming signal is continuously amplified through the primary input of the main amplifier. The correction signal is generated and stored on the capacitor C_{n2} during the sampling phase Φ_1, when the primary input of the null amplifier is shorted, and the output is fed back to the auxiliary input to form a voltage follower. During the zeroing phase Φ_2, the correction signal is fed to the auxiliary input of the main amplifier for compensation, and at the same time stored on the capacitor C_{m1} in order to retain the compensation during the following phase Φ_1 and deliver a continuous valid output.

After a limited number of the alternate phases, the impact of the inherent offset is reduced, which is maintained at a level that can be calculated as

$$\begin{aligned} v_{os} &= \frac{v_{os,m,p}\dfrac{A_{m,p}}{A_{m,a}} + v_{os,m,a} + \dfrac{v_{os,n,p}A_{n,p} + v_{os,n,a}A_{n,a}}{1 + A_{n,a}}}{\dfrac{1}{A_{m,a}} + \dfrac{A_{m,p}}{A_{m,a}} + A_{n,p}} \\ &\approx \frac{v_{os,m,p}\alpha_m + v_{os,m,a} + v_{os,n,p}\alpha_n + v_{os,n,a}}{A_{n,p}} \end{aligned} \tag{3}$$

where the subscription m and n, respectively, relate the parameters to the main amplifier and the null amplifier, and

$$\alpha_m = \frac{A_{m,p}}{A_{m,a}}, \quad \alpha_n = \frac{A_{n,p}}{A_{n,a}} \tag{4}$$

Actually, due to the effect of charge injection, sampling noise, and leakage current, when switches change their conditions, they produce perturbations on the capacitors they connect with. The impact can be effectively reduced in the two following ways.

First, taking into account the perturbation voltages presented at all the hold capacitors, Equation (3) can be rewritten as

$$v_{os} \approx \frac{v_{os,m,p}\alpha_m + v_{os,m,a} + v_{os,n,p}\alpha_n + v_{os,n,a}}{A_{n,p}} + \frac{v_{c,m}}{\alpha_m} + \frac{v_{c,n}}{\alpha_n} \tag{5}$$

where $v_{c,m}$ and $v_{c,n}$ are the differential interference voltages, respectively, due to perturbations on C_{m1}/C_{m2} and C_{n1}/C_{n2}. Hence, the interference can be reduced by increasing α_m and α_n.

Second, we add two switches, through which the

reference voltages $V_{ref,m}$ and $V_{ref,n}$ are introduced. As shown in Fig. 2, if the switches S3 and S4 are perfectly matched with S2, when they synchronously change conditions, they produce the same perturbations on capacitors C_{m1}/C_{m2} and C_{n1}/C_{n2}. Therefore, the perturbations only constitute the common mode signals, of which the impact could be adequately rejected.

The DC potentials of $V_{ref,n}$ and $V_{ref,m}$ should be set approximately to the open-loop output DC potential of the null amplifier in order to restrain the dithering when switching between the sampling and the cancelling phases. Simulation shows that such dithering not only degrades the integrity of the output signals, but also deteriorates the offset cancelling efficiency.

In addition to the offset, the continuous auto-zero technique also removes the $1/f$ noise and the temperature drift of the amplifier. This makes sense because all three can be considered as low-frequency noise. Thus, all the noise below the auto-zeroing frequency should be effectively removed[12].

4 Continuous time auto-zero opamp and the ISFET readout circuits design

4.1 Internal amplifiers design

A folded-cascode structure is chosen because it can be easily modified to provide an auxiliary differential input. Figure 4(a) demonstrates the schematic. When the differential voltage of the auxiliary input pair v_{a-} and v_{a+} is unbalanced, M3 and M4 occupy different amounts of tail current I_{b1}. Therefore a differential current signal Δi_a is produced. Δi_a is mirrored by M1, M2, M5, and M6, and then added to the differential current signal Δi, which is produced by the differential voltage of the primary input pair in the same way. In the last stage, the sum of those current signals is amplified and transformed into the output voltage. Hence, a dual differential inputs amplifier is formed, and its transfer function is identical with Eq. (2).

To maintain comparatively low power consumption, bias conditions of all the transistors in the designed amplifier are carefully set. The over-driven voltages and bias currents are set to be as low as possible, for the sake of low power and high gain and without diminishing too much of the GBW or the load driving capability.

Furthermore, to provide the constant bias conditions required for ISFET readout, a unique structure consisting of M15, M16, and a controllable voltage source is added to the amplifier, as shown in Fig. 4

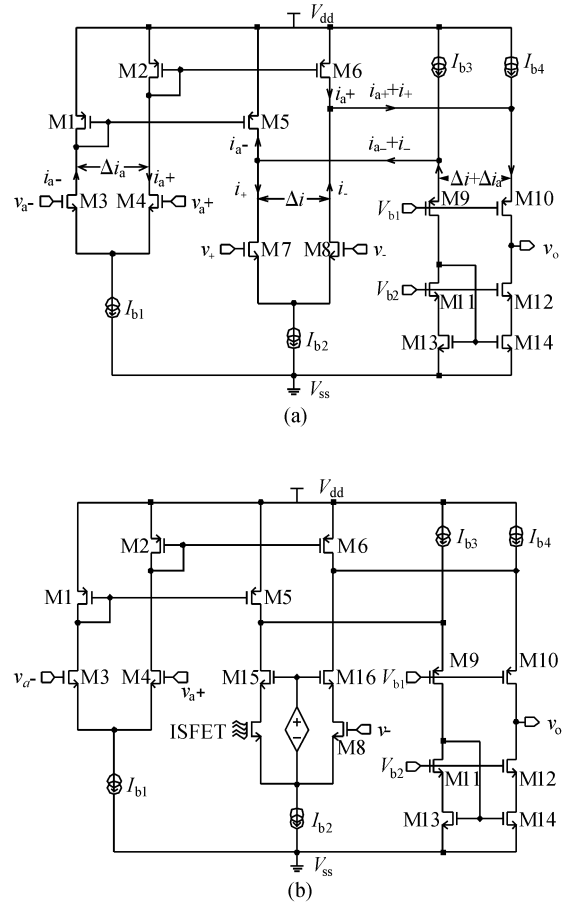

Fig. 4 Cascode structure of the main amplifier (a) and the modified version for ISFET application (b)

(b). When configured as a closed loop, I_{DS} of the ISFET is always half of I_{b2}. Meantime, V_{DS} of the ISFET is equal to the voltage source minus the threshold voltage of M15, which is almost a constant. Therefore, the gate voltage on the ISFET should be proportional to the ion concentration for a given solution.

The null amplifier also consists of a folded-cascode structure identical to the main amplifier, but with the output stage slightly adjusted to provide a different gain.

4.2 Other internal cells design

Complementary switches are applied. Each consists of a matched pair of dummy switches, which are driven in two complementary clocks as shown in Fig. 5. When perfectly matched, the channel carriers with opposite polarities in the pMOS and nMOS transistors neutralize, and the impact of charge injection is sufficiently reduced. Also, the opposite clocks can suppress the impact of clock feed through, as they always have charges opposite to the inherent gate-source or gate-drain capacitors of the complementary transistors, ensuring the clock does not interfere with the potential of the common capacitor plate significantly.

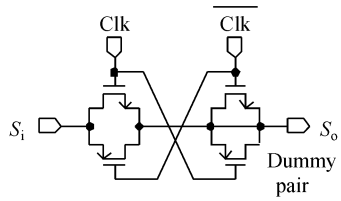

Fig. 5　Switch design with a dummy pair

A bandgap circuit previously designed in our lab is used in our auto-zero opamp to generate bias currents and bias voltages. The bandgap maintains a temperature coefficient of 35.63ppm/℃ within the temperature range of 0～120℃[13]. Together with the auto-zero technique, such a bandgap further enhances the precision of the opamp.

Each internal amplifier has its offset actively zeroed during one half of a clock cycle, while during the remaining half period the differential offset correction signals are stored on the hold capacitors. To maintain a low effective dropout, substantially small voltage degradation is mandatory over a sufficient period of time (5ms in this design). Thus, 10nF capacitors are chosen and placed externally.

An output buffer is designed and added to the final stage of the auto-zero opamp for the purpose of driving the resistive load.

4.3　ISFET readout circuits design

Our continuous time auto-zero opamp may be used to construct an ISFET readout for low power and high precision micro biosensor systems[14,15]. As depicted in Fig. 6, with two resisters (R_1 and R_2), we can configure the auto-zero opamp as a closed loop. Meanwhile, we extend the common gate of the ISFETs and connect it to the ion sensitive membrane. Based on the principle demonstrated in Ref. [16], high precision ISFET readout circuits can thus be implemented.

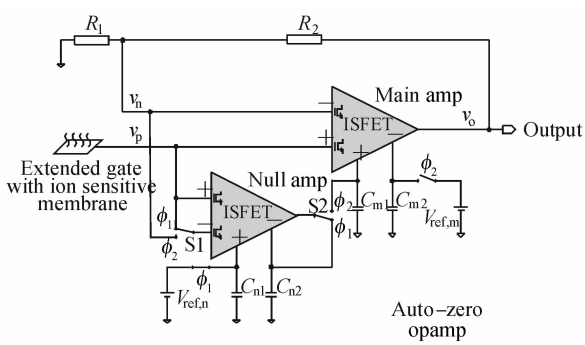

Fig. 6　An ISFET readout constructed with the auto-zero opamp

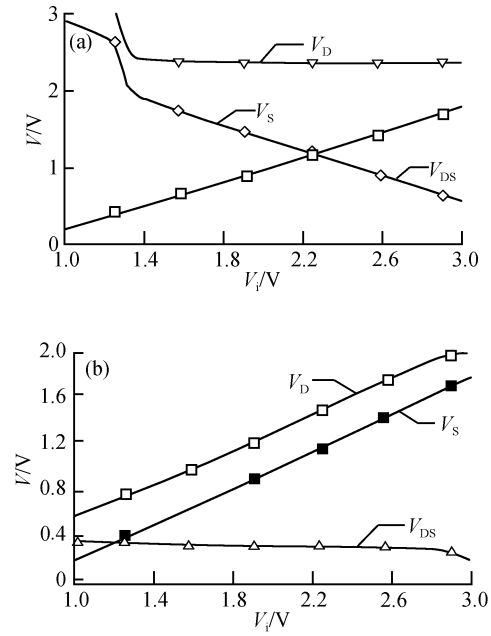

Fig. 7　V_{DS} varies with the input voltage without (a), and with (b) constant bias control

5　Circuit simulation and chip test

5.1　Simulation of constant bias voltage

The Cadence design tool was used to implement the circuit schematics. The simulations are performed with the SpectreS simulator, using 0.35μm technology models. The ISFET opamp is configured as a voltage follower. As shown in Fig. 7, the DC scan simulation validates the efficiency of the constant bias control. When the ISFET is biased in the saturation region and the input voltage varies from 1.0 to 2.7V, a nearly constant drain-source voltage of about 330mV is observed.

5.2　AC simulation of internal amplifiers

The AC response of the main amplifier and the null amplifier is simulated. For each, there are two sets of curves respectively for the primary input pair and the auxiliary input pair. The DC open loop gains are summarized in Table 1.

From the schematic in Fig. 2, within the auto-zero opamp, we have a cascading signal path made up of the null amplifier with its output connected to the auxiliary input of the main amplifier. Therefore, an accumulated gain of above 100dB is obtained, which is validated by simulation.

Table 1　DC open loop gains of each opamp

	Main amplifier	Null amplifier
Primary input	81.4dB	79.6dB
Auxiliary input	65.6dB	71.2dB

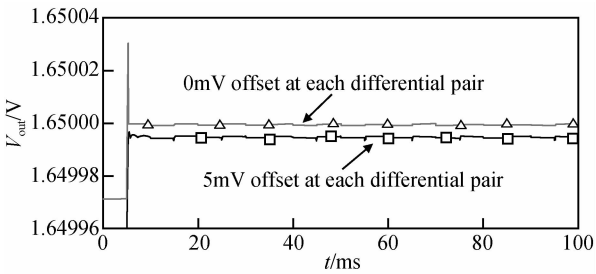

Fig. 8 Offset canceling simulation of auto-zero opamp

5.3 Simulation of low frequency noise canceling

We configure the auto-zero opamp as a voltage follower. First, by deliberately setting all the offset voltages in Fig. 3 to 0mV and feeding a constant 1.65V at the input, a transient response for the ideal opamp is obtained, as depicted in Fig. 8. For comparison, a response of the opamp with added offset is simulated. All the offset voltages are set as 5mV.

The difference of the two curves is nearly 4.5μV, i.e., the exact equivalent input offset of the whole auto-zero opamp. This result agrees with Eq. (3), and indicates that even though the process variation may bring about a mismatch on the order of magnitude of 1mV at all the differential pairs, the auto-zero opamp introduced in this paper can suppress the effect such that the overall offset of the opamp is only on the order of magnitude of 1μV.

From the equivalent input noise spectrum shown in Fig. 9, we see that the low frequency component of the $1/f$ noise is markedly eliminated, which greatly helps to achieve a high sensing resolution. The spike located at 100Hz is due to the 100Hz auto-zeroing frequency.

A simulation of the temperature drift is shown in Fig. 10. Throughout the temperature range -20℃ to 80℃, the offset maintains an extraordinarily low level and the average drift rate is about 150mV/℃.

5.4 Test of the prototype chip

The auto-zero opamp is fabricated in a standard 0.35μm, 4-metal and 2-poly layer CMOS process

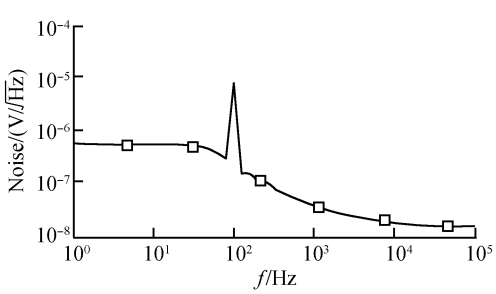

Fig. 9 Equivalent input noise spectrum

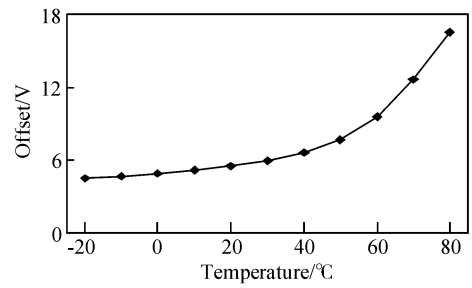

Fig. 10 Offset drift with the temperature

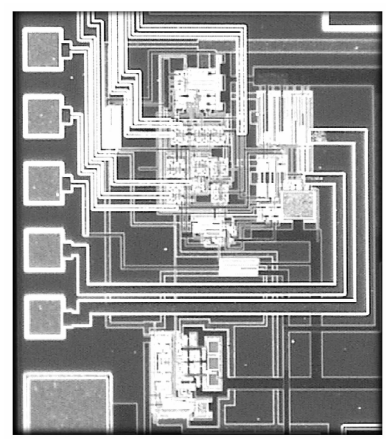

Fig. 11 Auto-zero opamp die microphotograph

(chartered semiconductor). The die size is approximately 800μm by 660μm. The overall power consumption is as low as 1.48mW. The die microphotograph is showed in Fig. 11.

Figure 12 shows the follower characteristic of the auto-zero opamp. A high linearity transfer function with the unity slope is obtained when the input voltage varies from 0.6 to 3.1V.

The input offset voltage can be measured using the test circuit from Fig. 13. Because the equivalent input offset voltage in our case is very small, it needs to be amplified using a resistor divider in the negative-feedback path. Therefore,

$$v_{os} = \frac{R(V_{out} - V_{in})}{R_f + R} = \frac{1}{1001}(V_{out} - V_{in}) \quad (6)$$

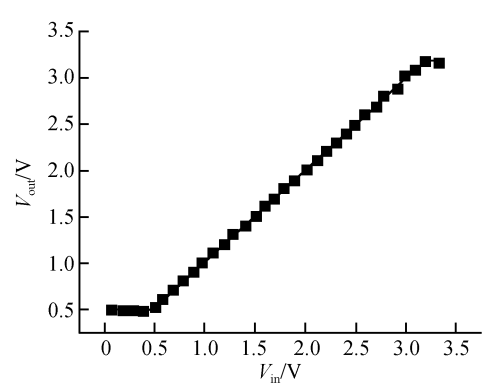

Fig. 12 Linear dynamic range measurement of the chip

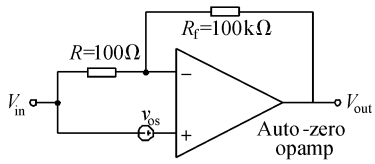

Fig. 13　Typical input offset voltage test circuit

Table 2　Offset voltages of three test chips

	Chip 1	Chip 2	Chip 3
Offset	10.8μV	11.3μV	12.0μV

The results are shown in Table 2 and the measured variations are primarily caused by uncertainty in the chip fabrication. The mean offset voltage is 11.4μV at room temperature.

5.5　Performance of the integrated sensor

We have developed a prototype high precision pH microsensor system, consisting of the proposed ISFET readout circuit, an extended-gate type ISFET sensor, and a micro reference electrode needed to provide a constant voltage potential in the solution for accurate measurement. Preliminary tests have been carried out in order to verify the basic functions of the readout circuit. The pH microsensor is tested in electrolyte samples with the pH values of 1.68, 6.88, and 12.64 at room temperature. The corresponding outputs are measured, which leads to a system sensitivity of around 51mV/pH. More comprehensive tests are currently ongoing.

6　Conclusion

A high precision CMOS opamp suitable for ISFET readout is demonstrated. The constant bias design enables the single chip integration of the ISFET sensor and the readout circuits. The adopted continuous time auto-zero technique significantly reduces the offset voltage to around 11μV, and also reduces the $1/f$ noise and temperature drift. The opamp is characterized with a DC open loop gain of more than 100dB and the overall power dissipation is only 1.48mW. This opamp has shown merits as part of a high precision ISFET-based micro pH sensor, of which the functionality has been well proven.

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一种适用于 ISFET 读出的高精度 CMOS 运放设计*

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摘要：介绍了一种适用于 ISFET 读出的高精度 CMOS 运放设计.该运放可为 ISFET 提供恒定电流、电压偏置，从而便于构建读出电路并于微传感器单片集成.通过运用连续时间自调零技术，大大降低了运放的失调电压、$1/f$ 噪声和温漂等低频噪声.该设计基于 0.35μm CMOS 工艺，电源电压 3.3V，运放的开环增益超过 100dB，输入等效失调电压低至 11μV，总功耗仅为 1.48mW.应用该运放实现的 pH 微传感器已通过实验验证.

关键词：高精度；自调零；运算放大器；ISFET 微传感器
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