第28卷 第10期
2007年10月

半 导 体 学 报
CHINESE JOURNAL OF SEMICONDUCTORS

Vol.28 No.10
Oct.,2007

Fabrication and Characterization of Strained Si Material Using SiGe Virtual Substrate for High Mobility Devices*

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Abstract: The fabrication and characterization of strained-Si material grown on a relaxed $Si_{0.79}Ge_{0.21}$/graded $Si_{1-x}Ge_x$/Si virtual substrate, using reduced pressure chemical vapor deposition, are presented. The Ge concentration of the constant composition SiGe layer and the grading rate of the graded SiGe layer are estimated with double-crystal X-ray diffraction and further confirmed by SIMS measurements. The surface root mean square roughness of the strained Si cap layer is 2.36nm, and the strain is about 0.83% as determined by atomic force microscopy and Raman spectra, respectively. The threading dislocation density is on the order of $4\times10^4 cm^{-2}$. Furthermore, it is found that the stress in the strained Si cap layer is maintained even after the high thermal budget process. nMOSFET devices are fabricated and measured in strained-Si and unstrained bulk-Si channels. Compared to the co-processed bulk-Si MOSFETs at room temperature, a significant low vertical field mobility enhancement of about 85% is observed in the strained-Si devices.

Key words: strained Si; RPCVD; SiGe virtual substrate; mobility enhancement
EEACC: 2520C; 2560S
CLC number: TN304.1 **Document code**: A **Article ID**: 0253-4177(2007)10-1518-05

1 Introduction

Scaling CMOS under the 65nm node faces both fundamental limits and technological challenges. One possible way to improve device performance is to enhance carrier mobility using material and process innovations (so-called "mobility engineering"). Strained Si grown on strain relaxed SiGe buffer layers is recognized as a promising way to achieve a global biaxial tensile strained channel. It provides enhanced electron and hole mobilities compared with bulk Si[1,2]. In order to obtain high quality strained-Si material, it is necessary to fabricate device-quality buffer layers with a very smooth surface and a low threading dislocation density. A number of growth techniques have been developed with demonstrated capability to produce device-quality SiGe films. The reduced pressure chemical vapor deposition (RP-CVD) technique is commercially available for large scale production of strained-Si MOSFET technology.

In this paper, the strain state as well as the surface morphology and threading dislocation density of a strained Si cap layer formed on a relaxed $Si_{0.79}Ge_{0.21}$ buffer layer were studied. This buffer layer has a compositionally graded buffer layer that serves as a template. Additionally, the characteristics of the SiGe virtual substrate were also investigated. In order to study the electrical quality of the RP-CVD grown strained-Si films and SiGe virtual substrates, n-MOSFET devices using a 10nm thick strained-Si/relaxed $Si_{0.79}Ge_{0.21}$ virtual substrate and bulk-Si (unstrained) channels were processed and measured.

2 Experiment

The samples were grown on 125mm Si(001) nominal p-type substrates (resistance in the 2～7 Ω·cm range) using an Applied Materials Epi-Centura 200 RP-CVD system. The sources of Si and Ge were pure dichlorosilane (SiH_2Cl_2) and germane (GeH_4) diluted at 15% in H_2, respectively. To further decrease the surface roughness and threading dislocation density, the growth rate and temperature were optimized in the epitaxy process.

* Project supported by the National Natural Science Foundation of China (Nos.60476017, 60636010)
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Received 8 May 2007, revised manuscript received 11 June 2007
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10nm strained Si
0.8μm uniform $Si_{1-x}Ge_x$ $x=0.21$
3μm graded $Si_{1-x}Ge_x$ $x=0\sim0.21$
Si substrate

Fig. 1 Structure of the strained Si material using a SiGe virtual substrate

The growth pressure was fixed to 13.3kPa; the growth temperature was set to 900 and 750℃ for the growth of the SiGe and the strained Si cap layer, respectively. Figure 1 shows the structure of strained Si material. Prior to the growth of a 10nm thick strained Si cap layer, a virtual substrate consisting of an approximately 3μm thick linearly graded $Si_{1-x}Ge_x$ (with a nominal final Ge mole fraction of 0.21) layer and of an approximately 0.8μm thick constant composition $Si_{0.79}Ge_{0.21}$ buffer layer was grown.

3 Material properties and characterization

3.1 X-ray diffraction determination of the composition

In order to determine the composition of the SiGe virtual substrate with a non-destructive method, conventional ω-2θ scans were performed using a Siemens D8 Discover high resolution double crystal X-ray diffractometer. The (004) ω-2θ scans are plotted in Fig. 2. Under the assumption that the SiGe virtual substrate is fully relaxed, Bragg's law is given by

$$2d_{(004)}\sin\theta=\lambda \quad (1)$$

where λ is the X-ray wavelength and is equal to 0.15406nm in this work, θ is the diffraction angle, and $d_{(004)}$ is the space between crystal planes along the ⟨004⟩ axes.

As for the symmetric (004) reflection, the lattice constant of the diamond alloy structure a_{lat} is given by

$$a_{lat}=4d_{(004)} \quad (2)$$

The nonlinear dependence of the SiGe unstrained lattice constant on the Ge mole fraction x can be calculated[3] by

$$a(Si_{1-x}Ge_x)=5.431+0.200326x+0.02327x^2(\text{Å}) \quad (3)$$

For Si (004), the Bragg's diffraction angle θ_0 is equal to 34.5646°. From the X-ray measurement (Fig. 2), the diffraction angle for the constant composition layer is estimated to be 34.2370°. Thus, combining Eqs. (1), (2), and (3), the Ge content can be estimated to be around 22%. The grading rate of the graded SiGe layer is then around 7.33% Ge/μm, which is consistent with the set-up values in the epitaxy process. The accurate determinations of the Ge composition and the strain relaxation degree require the measurement of both in-plane and perpendicular lattice parameters; details can be found in previous works[4].

In order to confirm the Ge mole fraction, secondary ion mass spectrometry (SIMS) measurements were carried out on a Cameca SIMS 4500. The measurement results of the Ge concentration depth profile inside the virtual substrate are plotted in Fig. 3. It shows a start at 2%, a grading rate around 7.4% Ge/μm of the graded SiGe layer, and a constant composition $Si_{0.79}Ge_{0.21}$ layer thickness of 0.778μm. These values further confirm the results obtained by the measurement of DC-XRD.

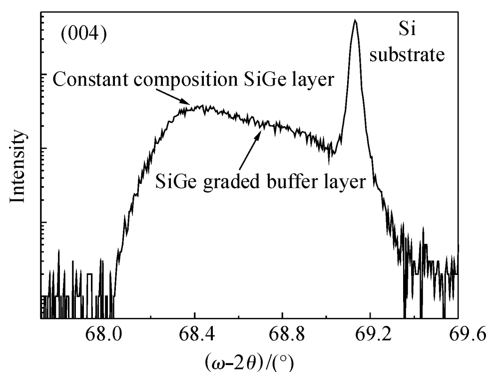

Fig. 2 X-ray double-crystal diffraction ω-2θ scan curve of the SiGe virtual substrate The corresponding SIMS profile is plotted in Fig. 3.

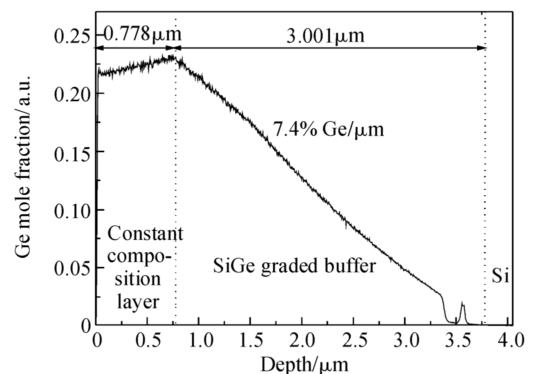

Fig. 3 SIMS depth profile of the Ge mole fraction inside the SiGe virtual substrate layer

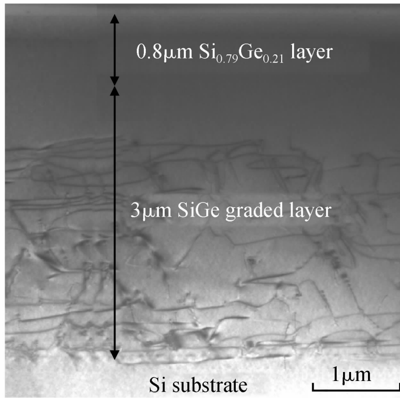

Fig. 4 Cross-sectional TEM image of the SiGe virtual substrate (electron beam along the ⟨110⟩ axes)

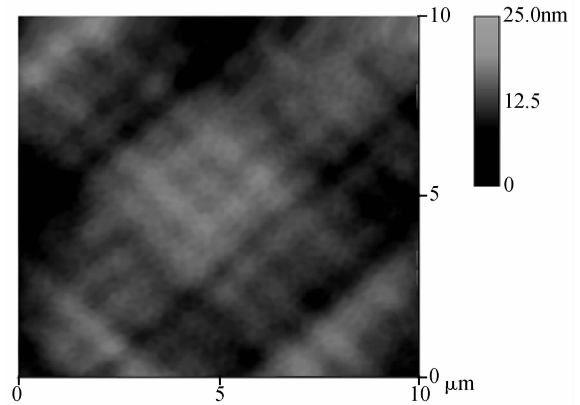

Fig. 5 Tapping-mode atomic force microscopy imaging ($10\mu m \times 10\mu m$) of the surface of a 10nm strained-Si/relaxed $Si_{0.79}Ge_{0.21}$ virtual substrate

3.2 Dislocation and surface morphologies

The dislocation morphology was analyzed using a JEOL 200CX cross-sectional transmission electron microscope (TEM) operating at 200kV. Figure 4 shows a cross-sectional TEM image of the SiGe virtual substrate. The benefit of using a linearly Ge graded layer is that misfit dislocations spread rapidly towards the edge driven by the residual stress in the films and are thus confined inside the graded layer. It greatly reduces the density of threading dislocations propagating into the strained Si layer[5,6]. A Schimmel etching solution was used to further depict the dislocations threading penetrating through the constant composition SiGe layer. Counting etch pits with an optical microscope, the statistically obtained threading dislocation density is $4\times10^4 cm^{-2}$. This result is consistent with the minimum threading dislocation density for relaxed graded SiGe buffer layer with a mismatch of less than 2%, which is in the range of 10^5 to $10^6 cm^{-2}$ (as estimated by Fitzgerald *et al*.[7]).

Figure 5 shows an AFM image of the surface morphology of a 10nm strained-Si on $Si_{0.79}Ge_{0.21}$ virtual substrate. The root mean square (RMS) surface roughness is measured to be 2.36nm ($10\mu m\times10\mu m$). A cross-hatch pattern along the orthogonal ⟨110⟩ axes is clearly observed.

Figures 6 (a) and (b) display Raman measurements for the 10nm strained $Si/Si_{0.79}Ge_{0.21}$ virtual substrate sample (see Fig. 5) and a reference Si bulk (unstrained) sample for excitation wavelengths of 514 and 325nm, respectively. In Fig. 6 (a), three distinct lines with strain and composition-dependent energies are found, which are ascribed to[8] Si-Si vibrations ($506.17cm^{-1}$) and localized Si-Si vibrations perturbed by neighboring Ge-Ge ($431.93cm^{-1}$) and Si-Ge ($404.97cm^{-1}$). The frequency shifts of the Si-Si and Si-Ge lines allow the simultaneous calculation of the composition and residual strain in the SiGe layer using empirical relations for the composition- and strain-induced frequency shift[9~11]:

$$x_{Ge} = (37\omega_{Si\text{-}Ge} - 24\omega_{Si\text{-}Si} - 2324.10)/2157.4 \quad (4)$$

$$\varepsilon = (68\omega_{Si\text{-}Ge} + 14.2\omega_{Si\text{-}Si} - 34626.52)/2157.4 \quad (5)$$

Solving Eqs. (4) and (5) simultaneously for the data of Fig. 6(a) gives a value of 23.7% for the Ge content and of 0.046 for the residual strain.

Furthermore, various thermal budgets introduced in the MOSFET device fabrication process have an important effect on the strain state in the strained Si cap layer. For example, the activation of the implanted impurity affects the source/drain ohmic contact, and the temperature influences the growth of high quality gate dioxide. In this work, we carefully consider the thermal budget of the growth of high quality gate dioxide. The results are reported in Figs. 6 (b) and 6 (a) (triangles) for excitation wavelengths of 325 and 514nm, respectively. There is almost no shift in the Raman spectra lines of the strained Si cap layer and SiGe virtual substrate before and after oxidation.

Considering that the theoretical value of the strain-shift coefficient of the Si longitudinal optical mode is $830cm^{-1}$[12], the observed shift in Fig. 6(b) corresponds to a strain in the Si cap layer of 0.83%. The strain in a 10nm strained Si cap

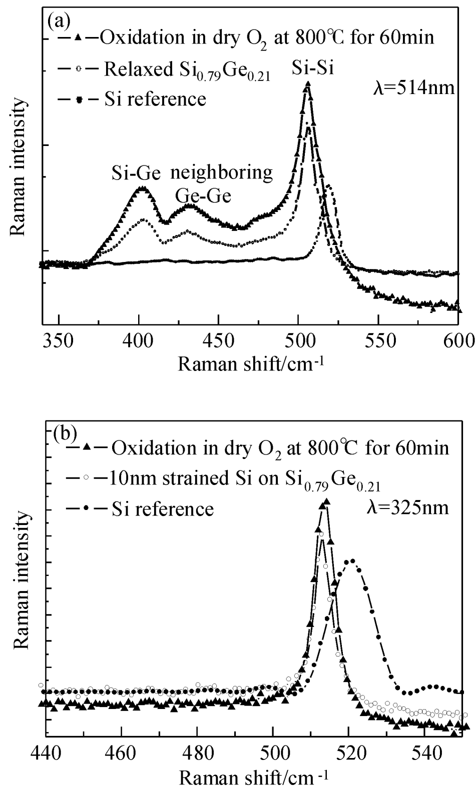

Fig.6 (a) Raman spectra of a 10nm strained-Si/relaxed $Si_{0.79}Ge_{0.21}$ virtual substrate for 514nm excitation wavelength; (b) Raman spectra of 10nm strained-Si before/after oxidation for 325nm excitation wavelength

layer formed on fully relaxed $Si_{0.79}Ge_{0.21}$ virtual substrate is about 0.82%. All these results confirm that the stress in the strained Si cap layer remains almost the same even after the thermal budget of the device process; this guarantees the improved device performance.

4 Device fabrication and mobility enhancement

To study the electronic quality of strained-Si films, we have fabricated and measured n-MOSFET devices with a 10nm thick strained-Si/relaxed $Si_{0.79}Ge_{0.21}$ virtual substrate and bulk-Si (unstrained) channels with a Boron *in-situ* light doping during the epitaxy process. Gate oxides were thermally grown to a thickness of 8.5nm at 800℃. The highest temperature step was the source/drain rapid thermal annealing for 15s at 950℃. The total thermal budgets were carefully controlled to minimize strain relaxation, Ge outdiffusion, and strained-Si consumption during the

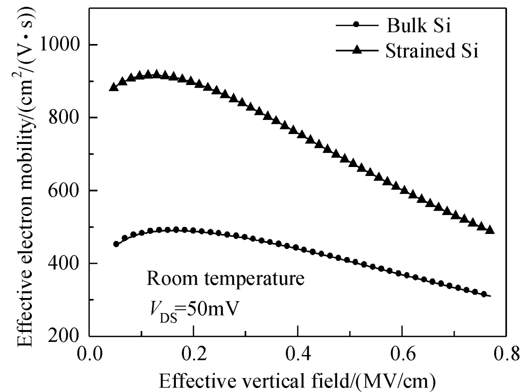

Fig. 7 Experimental effective electron mobility versus effective vertical field for strained-Si and bulk Si devices at room temperature

process.

In Fig. 7, the effective electron mobilities for both strained Si and bulk-Si measured in long channel devices are shown as a function of the effective vertical field. The electron mobility of the strained-Si device is enhanced by ~85% at low field and by ~60% at high field compared to the bulk-Si device. This result is consistent with that obtained by Rim *et al*.[13]. Although there is significant degradation in mobility as the effective vertical field increases for both strained-Si and bulk-Si control devices, the mobility enhancement factor is considered invariable in the whole effective vertical field, as predicted theoretically for the phonon-limited mobility in strained-Si MOS inversion layers[14]. The strained Si cap layer is thick enough and results in low interface state densities. Coulomb scattering is not the dominant scattering mechanism, and phonon and surface roughness scattering for the strained-Si and control bulk-Si materials make the electron mobility decrease at the same rate with an increasing effective vertical field[15].

5 Conclusion

We have studied the fabrication and characterization of strained-Si material using SiGe virtual substrate fabricated by RPCVD. The linear grading rate in the graded $Si_{1-x}Ge_x$ layer and the Ge mole fraction of the constant composition SiGe film were estimated by DC-XRD, and further confirmed by SIMS. The RMS of the strained silicon surface roughness is 2.36nm, as determined

by AFM measurements; the threading dislocation density is around $4\times10^4 cm^{-2}$. The strain in the strained Si cap layer is about 0.83% and is unchanged even with the high thermal budget. nMOSFET devices were fabricated and measured on a 10nm thick strained-Si/relaxed $Si_{0.79}Ge_{0.21}$ virtual substrate and bulk-Si (unstrained) channels. The low field effective electron mobility of the strained-Si device is enhanced by 85% at room temperature, compared to bulk devices.

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采用SiGe虚拟衬底高迁移率应变硅材料的制备和表征*

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摘要: 研究了生长在弛豫$Si_{0.79}Ge_{0.21}$/梯度$Si_{1-x}Ge_x$/Si虚拟衬底上的应变硅材料的制备和表征,这一结构是由减压外延气相沉积系统制作的.根据双晶X射线衍射计算出固定组分SiGe层的Ge浓度和梯度组分SiGe层的梯度,并由二次离子质谱仪测量验证.由原子力显微术和喇曼光谱测试结果得到应变硅帽层的表面粗糙度均方根和应变度分别为2.36nm和0.83%;穿透位错密度约为$4\times10^4 cm^{-2}$.此外,发现即使经受了高热开销过程,应变硅层的应变仍保持不变.分别在应变硅和无应变的体硅沟道上制作了nMOSFET器件,并对它们进行了测量.相对于同一流程的体硅MOSFET,室温下观测到应变硅器件中电子的低场迁移率显著增强,约为85%.

关键词: 应变硅; RPCVD; SiGe虚拟衬底; 迁移率增强

EEACC: 2520C; 2560S

中图分类号: TN304.1 **文献标识码:** A **文章编号:** 0253-4177(2007)10-1518-05

* 国家自然科学基金资助项目(批准号:60476017,60636010)

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2007-05-08收到,2007-06-11定稿

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