Fast-Lock Low-Jitter PLL with a Simple Phase-Frequency Detector*

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Abstract: A fast-locking, low-jitter, phase-locked loop (PLL) with a simple phase-frequency detector is proposed. The phase-frequency detector is composed of only two XOR gates. It simultaneously achieves low jitter and short locking time. The voltage-controlled oscillator within the PLL consists of four-stage ring oscillators which are coupled to each other and oscillate with the same frequency and a phase shift of 45°. The PLL is fabricated in 0.18μm CMOS technology. The measured phase noise of the PLL output at 500kHz offset from the 5GHz center frequency is −102.6dBc/Hz. The circuit exhibits a capture range of 280MHz and a low RMS jitter of 2.06ps. The power dissipation excluding the output buffers is only 21.6mW at a 1.8V supply.

Key words: phase locked loop; phase-frequency detector; voltage-controlled oscillator; jitter; locking time
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1 Introduction

High speed phase locked loops (PLL) are expected to be desirable components in many systems such as optical data links, high-speed memory interfaces, and RF and wireless transceivers. In optical communication systems, the synchronous clock should be extracted from NRZ data streams by virtue of the clock and data recovery circuit. The PLL-type of clock and data recovery circuits have been developed and widely implemented in optical transmission systems, because of their low cost, compactness, suitability to integration, and ease of treatment.

This paper presents a simple topology of PLL used in the optical transmission systems. It is required to generate low-noise or low-jitter clock signals and, at the same time, achieve fast locking. A phase-frequency detector (PFD) is one of the critical building blocks of a PLL. Previous PLLs were composed of a complex state machine and VCO[1~3]. A simple PFD composed of only two XOR logic gates has been used[4], but it has an asymmetric structure in the XOR that introduces a systematic phase skew between its two inputs. A PLL with a simple PFD composed of two symmetry XOR logic gates is proposed in this paper. The PLL can acquire fast-lock and low-jitter performance simultaneously. The PLL incorporates a four-stage interpolating ring oscillator to achieve a wide tuning range.

2 Architecture

In a generic PLL circuit, as shown in Fig. 1, the phase detector compares the phase of the reference clock or input data signal to the phase of the clock generated by the voltage-controlled oscillator (VCO), producing an error that is proportional to the phase difference between its two inputs. The error is then applied to a charge pump and a low-pass filter so as to generate the oscillator control voltage.

A critical problem in the architecture of Fig. 1 relates to the inherently unequal propagation delays for the two inputs of the phase detec-tor[5]. Most phase detectors are asymmetric with respect to the reference clock input and VCO inputs, thereby introducing a systematic phase skew between two inputs in phase-lock condition. Since it is difficult to replicate this skew, the generic PLL architecture suffers from a systematic phase margin, unless the raw speed of the technology is much higher than the reference frequency. Our approach to solving the skew adopts a symmetric circuit with respect to the reference clock and VCO inputs.

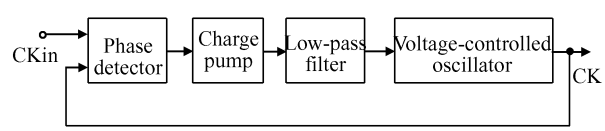

Fig. 1 Generic PLL architecture

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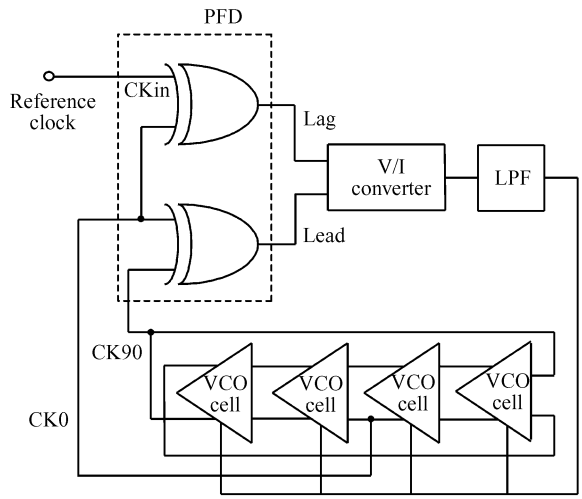


Fig. 2　Proposed PLL architectrue

In this work, a linear phase frequency detector composed of two symmetric XORs is described. The PFD has no phase skew between its outputs so as to alleviate the problems mentioned above. Owing to its simplicity, this technique achieves both high speed and low power dissipation, while minimizing the ripple on the oscillator control voltage.

The proposed PLL architecture is shown in Fig. 2. The PFD produces the Lead and Lag signal to the V/I converter and filter. The VCO, composed of four differential stages, generates two quadrature output clocks.

The Lead signal is produced between the two clocks CK0 and CK90, and the Lag signal is generated between CK0 and CKin. Figure 3 shows the detection signal waveform of the PFD. If CKin is phase-aligned with CK90, as in the lock state, the Lead signal and the Lag signal transitions occur at the same time. Therefore, the control voltage of the VCO remains at the same level.

If CKin is faster than CK90, then the 'high' state of the Lag signal is shorter than that of the Lead signal. Thus, the surplus part of the Lead signal decreases the charge in the loop filter. The decreased output of the filter makes the clock period shorter to track CKin.

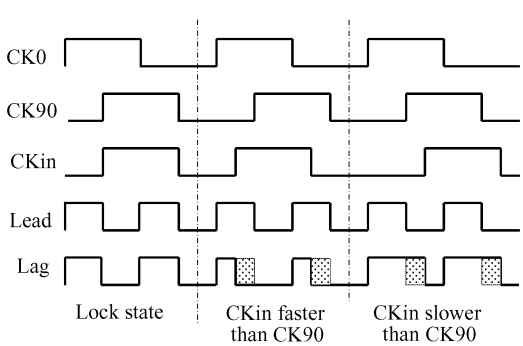
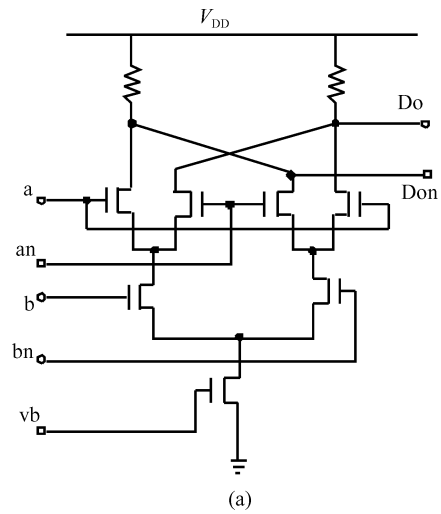


Fig. 3　Phase-frequency detection algorithm



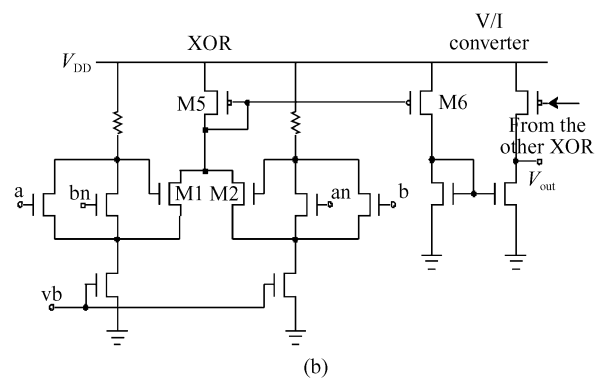


Fig. 4　(a) Conventional stacked XOR gate; (b) Symmetric XOR gate and V/I converter

If CKin is slower than CK90, then the 'high' state of the Lag signal is longer than that of the Lead signal. Thus, the surplus part of the Lag signal increases the charge in the loop filter. The increased output of the filter makes the clock period longer to keep pace with CKin.

When there is a frequency difference between the input signal and the VCO clock, the same algorithm can be applied. In the locked condition, the average charge caused by the 'high' state of Lag signal and Lead signal is the same. Thus, the control voltage of the VCO remains in the same level.

3　Building blocks

3.1　Symmetric XOR gate and V/I converter

The XOR gates in Fig. 2 must be symmetric with respect to their two differential inputs. Otherwise, differences in propagation delays will result in systematic phase skew. The conventional stacked XOR gate is shown in Fig. 4 (a). The symmetric XOR gate along with the V/I converter in our work is imple-

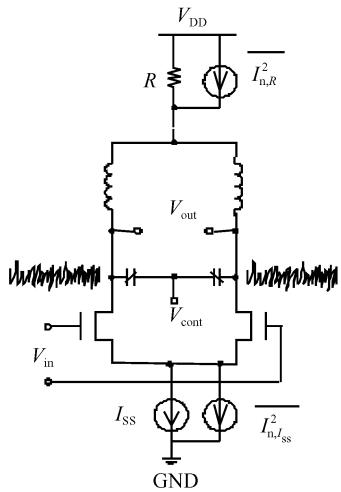


Fig. 5 Output common-mode noise

mented as shown in Fig. 4 (b). The circuit avoids stacking stages while providing perfect symmetry between the two inputs[6]. The operation of the XOR circuit is as follows. If the two logical inputs of a and b are identical, one of the input transistors on the left and one of the input transistors on the right turn on, thus turning M5 off. If the two inputs are not equal, one of the tail currents flows through M5.

Transistors M1 and M2 form local positive feedback loops and need no additional reference voltage. The current mirror composed of M5 and M6 copies the output current of the XOR gate, providing nearly rail-to-rail swings for the oscillator control line to increase the capture range of the PLL. All of the transistors in the V/I converter have small overdriving voltages to acquire nearly rail-to-rail swings. Since the converter drives the single-ended control terminals of the varactors in the VCO, it is designed to provide a single-ended output. Unlike charge pumps, V/I converters need not switch after every phase comparison and are, therefore, free from the dead-zone problem.

3.2 VCO

Typical quadrature clock generation method is to cross couple the even stages' VCO core cell. The purpose of coupling the VCO cell is to create a $\pi/4$ phase difference between I (in-phase signal node) and Q (quadrature-phase signal node). The common cell of VCO is shown in Fig. 5. The synchronous oscillation frequency can be tuned by using the varactor. To achieve a wide tuning range with a low supply voltage, the tank incorporates MOS varactors rather than pn junctions. But the noise currents produced by I_{SS} and R modulate the output common-mode voltage and, hence, the capacitance of the two varactors. The phase noise of the VCO is greatly increased by this effect[7]. The output common-mode noise $V_{n,CM}$ can

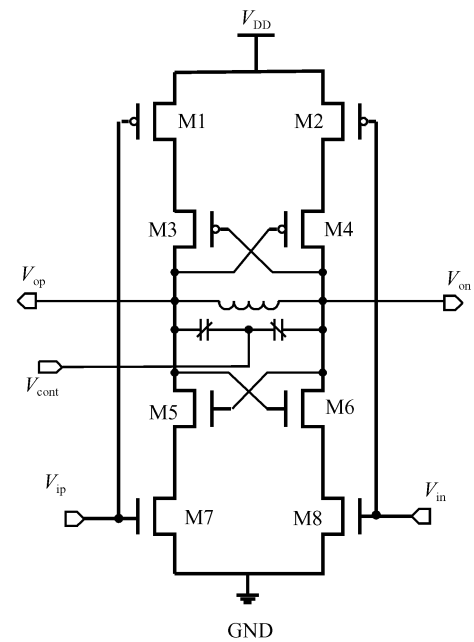


Fig. 6 Quadrature VCO cell

simply be placed in series with V_{cont} to predict the resulting phase noise. Specifically,

$$\overline{V^2_{n,CM}} = (\overline{I^2_{n,I_{SS}}} + \overline{I^2_{n,R}})R^2 \quad (1)$$

The simulated results indicate that the flicker noise of the tail current sources and their diode-connected mirror device contribute 90% of the phase noise[8].

The proposed quadrature VCO cell is shown in Fig. 6. Omitting the general current source below transistor M7 and M8 has the advantages of eliminating an important phase-noise source. Furthermore, it can maximize the signal swing[9]. This VCO topology can acquire highly accurate *I-Q* signals, while using low power and producing low phase noise.

The main disadvantage caused by omitting the current source is the increased sensitivity to the power supply. This effect can be reduced by the cascode coupling of nMOST and pMOST. For the realization of the negative resistance, the combination of nMOS and pMOS transistors was chosen in order to reuse the DC current.

4 PLL locking time

The PLL is a non-linear circuit and its design and optimization involve many trade-offs. Usually, the PLL bandwidth or cutoff frequency must be not too large in order to satisfy the noise and stability requirements. However, by choosing a narrow bandwidth, it becomes difficult to satisfy the speed requirement. An important parameter relevant to speed

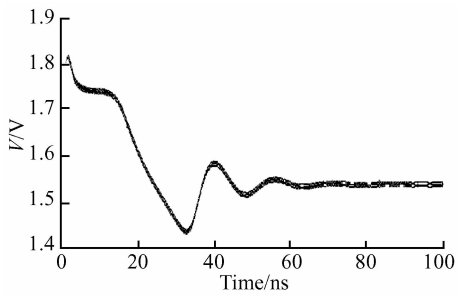


Fig. 7　VCO control voltage of the PLL when the input frequency changes from 5.2 to 5.0GHz

is locking time, which determines the amount of data lost from the out-of-locked state to the locked state.

For a conventional second-order system with $\zeta < 1$, the step response is expressed as[10]:

$$y(t) = \left[1 + \frac{1}{\sqrt{1-\zeta^2}}\exp(-\zeta\omega_n t) \times \sin(\omega_n\sqrt{1-\zeta^2}\,t - \Psi)\right]u(t) \quad (2)$$

where $\Psi = \sin^{-1}\sqrt{1-\zeta^2}$. Thus, for a frequency step at the PLL input, Equation (2) can be used to calculate the time required for the output frequency to settle within a given error band around its final value. The approximate acquisition time is

$$T \approx \frac{\pi^2}{16} \times \frac{\Delta\omega^2}{\zeta\omega_n^3} \quad (3)$$

where $\Delta\omega$ is the initial frequency step. The acquisition time T is inversed to ω_n. This relationship exacerbates the tradeoff between the jitter and the acquisition time.

The proposed PLL was simulated using the Cadence's simulator Spectre and the transistor models of the 0.18μm CMOS process provided by Taiwan Semiconductor Manufacture Corporation (TSMC). Simulation results confirm the locking time improvement of the PLL topology, as shown in Fig. 7. This figure depicts the variation of the VCO control voltage of the PLL when the reference frequency CKin changes abruptly from 5.2 to 5GHz. The PLL acquisition time for this frequency sweep is less than 60ns, which is very attractive compared to the locking time of a conventional PLL and other improved structures[11~13].

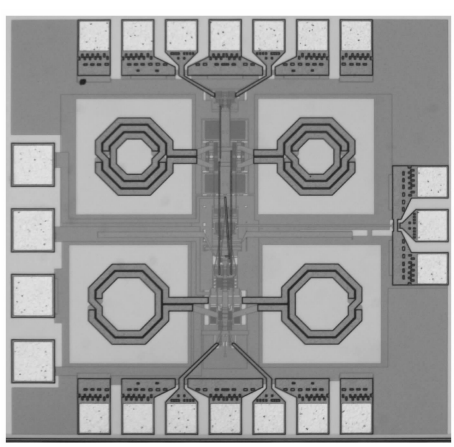


Fig. 8　PLL photomicrograph

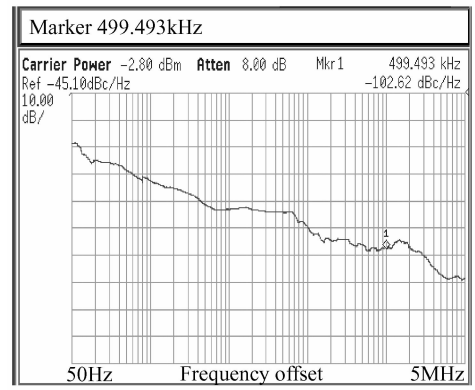


Fig. 9　Phase noise of the locked output at a 5GHz oscillation frequency

5　Experimental results

A photomicrograph of the 1mm × 0.95mm IC is shown in Fig. 8. The pad configuration was dictated by RF on-wafer probes. In order to increase the isolation between the oscillator and the data path circuits, their power supplies are kept separate. The frequency of the oscillator can also be tuned by its separated power supply to compensate the variation of technology and temperature. A plot of the PLL output spectrum in the locked state is shown in Fig. 9. The phase noise is −102.6dBc/Hz@500kHz. Figure 10 shows that the RMS jitter of the PLL output is only 2.06ps. The phase noise and locking performance is superior or comparable to that of other improved designs[14,16]. The IC consumes 21.6mW from a 1.8V supply (not including 50Ω test output buffers). The performance of this work and the other previously published PLL is summarized in Table 1.

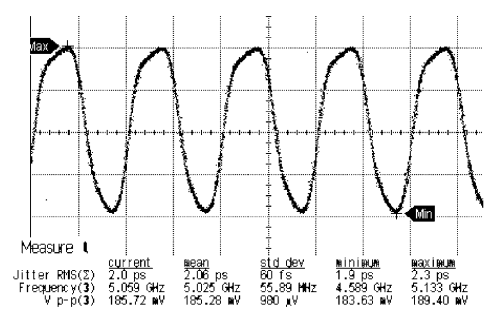


Fig. 10　Locked jitter performance of PLL

Table 1 PLL performance summary

	This work	Ref.[14]
Technology	TSMC 0.18μm CMOS 1P6M	TSMC 0.18μm CMOS 1P6M
Supply voltage/V	1.8	1.8
VCO free running phase noise /(dBc/Hz)@5MHz	-104.1	-
PLL output phase noise /(dBc/Hz)@1MHz	-102.6	-102
Locked jitter (RMS)/ps	2.06	-
Locking time/ns	60	3000
Power consumption/mW	83.3	70
Power excluding buffers/mW	21.6	>34
Die size/(mm×mm)	1×0.95	1.4×0.964

6 Conclusion

A simple PLL structure characterized by the two symmetric XOR gates phase-frequency detectors has been proposed and realized. The PLL can achieve fast-locking and low-jitter performance. The PLL has a phase noise of -102.6dBc/Hz@500kHz. Using the two-XOR gates as phase-frequency detectors, the PLL can catch the phase and frequency variations. Its capture range of 280MHz is sufficient to account for process, voltage, and temperature variations.

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一个简单鉴频鉴相器结构实现的快速锁定低抖动锁相环*

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摘要： 用简单的鉴频鉴相器结构实现了一个快锁定低抖动的锁相环.鉴频鉴相器仅仅由两个异或门组成,它可以同时获得低抖动和快锁定的性能.锁相环中的电压控制振荡器由四级环形振荡器来实现,每级单元电路工作在相同的频率,并提供45°的相移.芯片用0.18μm CMOS工艺来实现.PLL输出的中心频率为5GHz,在偏离中心频率500kHz处,测量的相位噪声为-102.6dBc/Hz.锁相环的捕获范围为280MHz,RMS抖动为2.06ps.电源电压为1.8V时,功耗仅为21.6mW(不包括输出缓冲).

关键词： 锁相环；鉴频鉴相器；电压控制振荡器；抖动；锁定时间

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