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# $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs with $f_{max}$ of 183GHz*

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**Abstract**: By epitaxial layer structure design and key fabrication process optimization, a lattice-matched InP-based $In_{0.53}Ga_{0.47}As$-$In_{0.52}Al_{0.48}As$ HEMT with an ultra high maximum oscillation frequency ($f_{max}$) of 183GHz was fabricated. The $f_{max}$ is the highest value for HEMTs in China. Also, the devices are reported, including the device structure, the fabrication process, and the DC and RF performances.

**Key words**: maximum oscillation frequency/power-gain cutoff frequency; high electron mobility transistor; InGaAs/InAlAs; InP

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## 1 Introduction

InP-based InGaAs/InAlAs high electron mobility transistors (HEMTs) are considered to be one of the most promising devices for the next generation of millimeter wave and optical communications because of their superior high frequency and low noise performances[1~3]. These performances are attributed to high electron mobility, high saturation velocity, and high sheet carrier density obtained in this material system[4,5].

In our previous work, we fabricated lattice-matched InP-based HEMTs with a 120GHz current gain cutoff frequency ($f_t$)[6]. However, maximum oscillation frequency/power-gain cutoff frequency ($f_{max}$) of those devices was relatively low (only 40GHz). Thus, the application of these devices to power millimeter-wave systems is limited. Recently, we optimized a series of key processes and fabricated lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs with an ultra high $f_{max}$ of 183GHz. This $f_{max}$ is the highest ever reported for HEMTs in China. In this paper, the devices are reported, including the device structure, the fabrication process, and the DC and RF performances.

## 2 Fabrication process

The HEMT epitaxial structure used in this work consists of an $In_{0.52}Al_{0.48}As$ buffer layer (300nm), a lattice-matched $In_{0.53}Ga_{0.47}As$ channel layer (15nm), an $In_{0.52}Al_{0.48}As$ spacer (3nm), a Si-δ-doped sheet ($5 \times 10^{12} cm^{-2}$), an $In_{0.52}Al_{0.48}As$ barrier layer (8nm), an InP etch-stopper layer (4nm), and a Si-doped $In_{0.53}Ga_{0.47}As$ cap layer ($1 \times 10^{19} cm^{-3}$, 30nm), which were grown on a semi-insulating(100) InP substrate by molecular beam epitaxy (MBE). Electron mobility of the two-dimensional electron gas (2DEG) is $9300cm^2/(V \cdot s)$ and the sheet carrier density is $3.32 \times 10^{12} cm^{-2}$ at room temperature, which was obtained by Hall measurements. The epitaxial layers were designed by our group and grown by MBE technology in Singapore.

Source and drain ohmic contacts were formed using alloyed Ni/Ge/Au/Ge/Ni/Au and the spac-

Table 1　Lattice-matched HEMT epitaxial layer structure

| InAlAs/InGaAs HEMT | | | |
|---|---|---|---|
| Layer | Thickness/nm | Dopant | Concentration |
| $In_{0.53}Ga_{0.47}As$ | 30 | Si | $1 \times 10^{19} cm^{-3}$ |
| InP | 4 | | |
| $In_{0.52}Al_{0.48}As$ | 8 | | |
| Si-δ-doped layer | | Si | $5 \times 10^{12} cm^{-2}$ |
| $In_{0.52}Al_{0.48}As$ | 3 | | |
| $In_{0.53}Ga_{0.47}As$ | 15 | | |
| $In_{0.52}Al_{0.48}As$ buffer | 300 | | |
| SI InP substrate (100) | | | |

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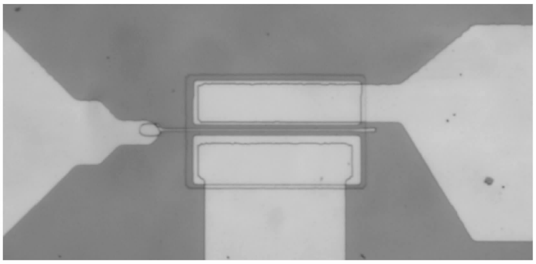

Fig.1　Partial photograph of an InP HEMT

ing between source and drain electrode pads was 2μm. Note that for a long time a low temperature alloy method[7] was used to prevent degradation of the epitaxial structure and achieve low contact resistance simultaneously. The contact resistance measured by the transmission line model (TLM) method was typically 0.1Ω·mm. Mesa structures were formed by photolithography and wet chemical etching using $H_3PO_4/H_2O_2/H_2O$ solution. Then Ti/Au connecting wire metal was evaporated by an electronic beam evaporation system.

The gate formation process was similar to that used in our previous work[6], except for the thickness of electron beam (EB) resist. A trilayer EB resist (PMMA/PMGI/PMMA) was first spun onto the substrate. A single alignment, EB exposure and a series of development steps were then carried out to form a recess above the InGaAs cap layer. The gate recess in the Si-doped $n^+$-InGaAs cap layer was formed by wet chemical etching using an aqueous mixture of citric acid ($C_6H_8O_7$) and hydrogen peroxide ($H_2O_2$), whose etching selectivity of InGaAs over InP is about 160[8]. The gate was finally formed after the evaporation of the Ti/Pt/Au layers with a total thickness of 300nm. Figure 1 is the photograph of the device we obtained, with a gate length of 0.2μm and a gate width of 1×50μm.

## 3　Device performance

Figure 2 shows the typical current-voltage (*I-V*) characteristics of the HEMTs at room temperature. The gate-source voltage $V_{gs}$ is increased from −2.0 to 0V in 0.4V steps and the device shows good pinchoff behavior. The maximum current density at $V_{gs}=0V$ is 280mA/mm. The current density was less than expected, possibly because of degradation in the material and devices due to the lengthy fabrication period. Figure 3 shows the transfer characteristics and transconductance characteristics of the HEMTs. The threshold voltage is −0.6V. When the drain-source voltage ($V_{ds}$) is 2.0V, the maximum transconductance ($g_m$) is 550mS/mm with a gate-source voltage ($V_{gs}$) of −0.35V. Off-state gate-drain breakdown voltage defined at a gate-drain current of 1.0mA/mm is −2.0V. The on-state drain-to-source breakdown voltage, i.e. $V_{gs}=0V$, is 2.5V.

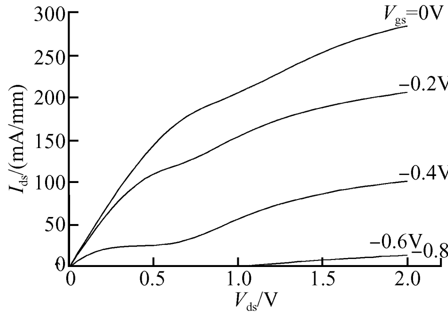


Fig.2　Current-voltage (*I-V*) characteristics of the InP HEMT

*S*-parameters, shown in Fig.4, were measured in a frequency range from 0.045 to 45GHz using an Agilent 8510XF vector network analyzer. Figure 5 shows the frequency dependence of the current gain ($|h_{21}|^2$) and the maximum available power gain/stable power gain (MAG/MSG) of the HEMTs with a drain-source voltage ($V_{ds}$) of 2V and a gate-source voltage ($V_{gs}$) of −0.3V. Note that the parasitic capacitance due to the probing pads was carefully measured and de-embedded. Finally, we obtained an $f_T$ of 93GHz and an $f_{max}$ of 183GHz by extrapolating $|h_{21}|^2$ and MAG/MSG with a −20dB/decade slope.

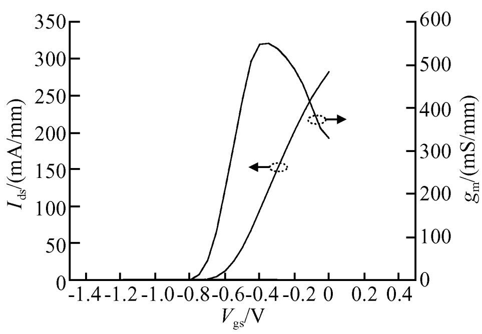


Fig.3　Transfer and transconductance characteristics of the InP HEMT

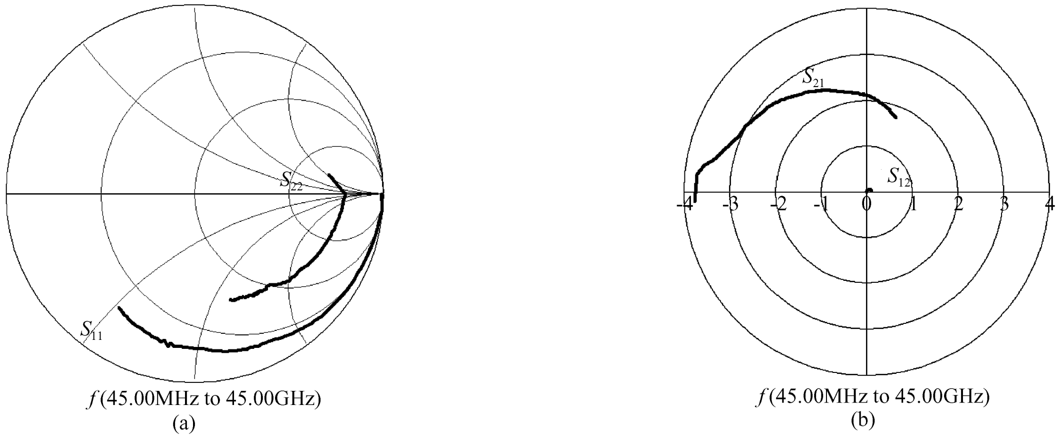


Fig.4 $S$-parameter of the InP HEMT at $V_{ds}=2V$, $V_{gs}=-0.3$ V in a frequency range from 45MHz to 45GHz (a) $S_{11}$ and $S_{22}$; (b) $S_{12}$ and $S_{21}$

## 4 Summary

We have successfully developed lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs with an $f_{max}$ of 183GHz, which is the highest value reported for HEMTs in China. Because of the lengthy device fabrication, the material and devices may have degraded to a certain extent, affecting the DC and high-frequency characteristics of the devices. However, it is justified to expect that InP-based HEMTs with much better characteristics will be fabricated in our laboratory soon.

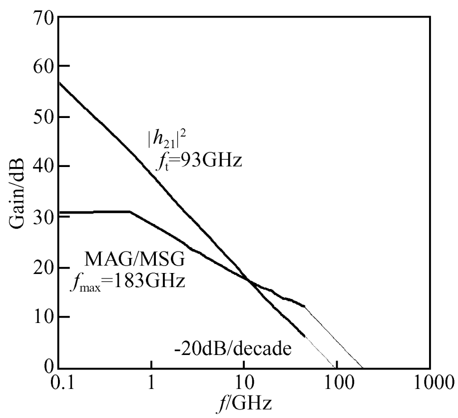


Fig. 5 Frequency dependency of current gain ($|h_{21}|^2$) and maximum available power gain/stable power gain (MAG/MSG) of the InP HEMT biased at $V_{ds}=2V$ and $V_{gs}=-0.3V$

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# 功率增益截止频率为 183GHz 的 $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs*

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**摘要**：通过合理的外延层材料结构设计和改进的器件制备工艺，制备出功率增益截止频率（$f_{max}$）为 183GHz 的晶格匹配 InP 基 $In_{0.53}Ga_{0.47}As$-$In_{0.52}Al_{0.48}As$ HEMT. 该 $f_{max}$ 为国内 HEMT 器件最高值. 还报道了器件的结构、制备工艺以及器件的直流和高频特性.

**关键词**：最大振荡频率/功率增益截止频率；高电子迁移率晶体管；InGaAs/InAlAs；InP

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