# A 12～18GHz Wide Band VCO Based on Quasi-MMIC

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**Abstract**: Using an in-house MMIC and an off-chip, high-quality varactor, a novel wide band VCO covered Ku band is introduced. In contrast to HMIC technology, this method reduces the complexity of microchip assembly. More importantly, it overcomes the constraint that the standard commercial GaAs pHEMT MMIC process is usually not compatible with high-quality varactors for VCO, and it significantly improves the phase noise and frequency tuning linearity performances compared to either MMIC or HMIC implementation. It is a novel and high-quality method to develop microwave and millimeter wave VCO.

**Key words**: MMIC; wide-band; VCO; Ku band; off-chip varactor; bond-wire inductor
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## 1 Introduction

Broadband voltage controlled oscillators (VCOs) are crucial parts in many electronic systems such as communication, radar, or measurement applications. In terms of the integration approaches, VCOs can be implemented in either hybrid or monolithic form. Hybrid integration, which means that discrete active devices, together with other components, e. g. inductors, capacitors, and resisters, are integrated on a ceramic or glass substrate or in a package through micro-assembly process. Monolithic integration means that all the components, both active and passive, are integrated in a single semiconductor substrate through a complicated semiconductor process. Hybrid integrated VCOs have excellent phase noise performance and can conveniently accommodate various requirements and commercial products with the octave frequency band, which is within the 10GHz frequency range. However, the performances of RF components deteriorate as the frequency increases, so it will be more difficult to assemble hybrid microwave circuits than those in lower frequency ranges. Hybrid integrated VCOs using FET as a negative resistance generator usually operate below the K band (18 ～ 26.5GHz). In terms of the millimeter frequency range, most solid-state microwave sources are realized with frequency multiplication or using Gunn diode or avalanche diode devices. Compared with the hybrid process, a monolithic microwave integrated process can realize VCOs easily in higher frequency due to its material characteristics and the special processes involved. MMIC VCOs with frequency reaching 100GHz have been reported in recent years. However, it is difficult to fabricate high quality varactor diodes with the commercially available MMIC process, where the capacitance ratio of Schottky-barrier contact between GaAs epitaxy and metal anode is limited and the parasitic resistance loss leads to a lower $Q$-factor. Therefore, the tuning bandwidth of MMIC VCO is constrained, and most reported MMIC VCOs based on GaAs FET have a relative band width less than 20%. Reference [1] gave a theoretical analysis of VCOs in feedback and reflection configurations and presented a VCO in feedback configuration with a tuning range from 4.60 to 7.28GHz, i.e. a relative tuning bandwidth of about 45%. The $Q$-factor of the varactor in MMICs will degrade as the frequency increases. Meanwhile, the distribution effects of all the elements will be significant, so single diode tuned VCOs with a tuning range over 20% beyond 10GHz are rarely reported. Lower $Q$-factor varactors contribute much of the resistive parasitic of resonant circularity, which not only constrains tuning bandwidth, but also degenerate phase noise performance of VCOs. Much effort has been given to improving the $Q$-factor of resonant circularity. Reference [2] presented a VCO using bond wire instead of a spiral inductor on silicon, which circumvents the complicated parasitic loss in an integrated inductor. The MEMS technique is another choice to improve the $Q$-factor of the resonance tank[3,4]. Reference [5] presented a VCO, called a semi-monolithic VCO by the author, which integrated a microstrip, resistors, and capacitors on $Al_2O_3$ ceramic substrate. Two discrete GaAs FETs served as oscillation and amplification devices.

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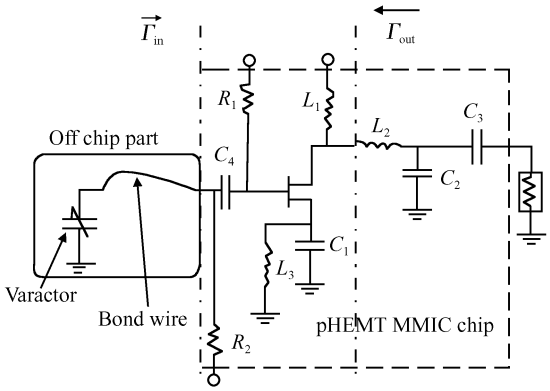


Fig. 1 Topology of the VCO

Two hyperabrupt junction Schottky-barrier diodes tuned at the gate and source of the oscillation FET simultaneously. The VCO gave an extra wide frequency range from the X band to the Ku band. In fact, this VCO is a hybrid integration circuit, and it is not relevant to monolithic circuits.

In this paper, we present a Ku band VCO using a combination of monolithic and hybrid integration techniques, which presents a relative tuning bandwidth of 45% and improves the phase performances. Compared with hybrid integrated VCO, it is easier to assemble and the frequency linearity of the tuning characteristics is improved. Frequency-tuning linearity is determined not only by the varactor, but also by the distribution effects of the integrated components, especially in higher frequency ranges. In order to enhance the linearity of frequency, the matching and feedback components, especially the feedback components at the gate, should approach lumped performances. Components fabricated in MMICs show as good of performances as lumped devices within the Ku band, and bond wire can be treated as a lumped inductor in the broad range up to millimeter wavelengths. The tuning linearity of the frequency of the VCO in this paper is less than 2.

## 2 Principle and design of the circuit

The topology of the circuit is shown in Fig. 1. The MMIC part of the circuit was fabricated by the GaAs pHEMT IC process. On-chip components consist of a negative resistance generator FET device, bias, and matching networks. The off-chip parts consist of a hyperabrupt-junction varactor and a golden bond wire inductor.

### 2.1 Analysis of bond wire inductor

A number of factors, i.e. length, the level of arc, the height off ground, and the distance to other conductors, etc, affect the inductance of bond wire. These

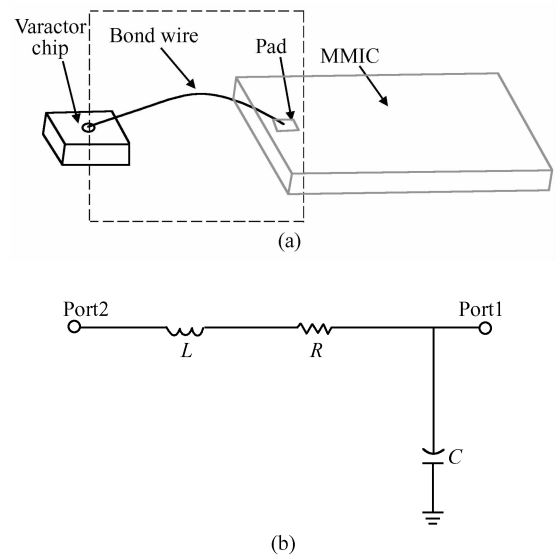


Fig. 2 Realization of off-chip inductor by bond-wire (a) Bond-wire connection partition of the circuit; (b) Equivalent circuit of the bond-wire connection

factors together interfere with the self- or multi-inductance and parasitic coupling capacitance of the bond wire, and make the accurate evaluation of bond wire inductance difficult. Full wave electromagnetic field simulation can model the bond wire more accurately. However, in terms of the bonding process, which is difficult to control as accurately as desired, whether it is necessary to perform time-consuming modeling and calculation procedures is doubtable. In most cases, estimations are adequate in engineering circumstances. In this paper, we use a single bond wire as an inductor, and a simple model suffices for the required accuracy. The inductance is reduced by its level of arc, due to the self-inductance of the segments of the bond wire in the microwave frequency range. For simplicity, we adopt nearly straight and flat bond wire to minimize the self-inductance of our model, as shown in Fig. 2 (a).

The thicknesses of the varactor and MMIC are 130 and 100$\mu$m, respectively, so the height of bond wire varies from 100 to 500$\mu$m above the ground. There is image reflow current due to the ground, which also reduces the total conductance. Reference [6] gave the expression of effective inductance of the bond wire, which takes the effect of the ground into account, that is

$$L_e(\mathrm{nH}) = 2\times10^{-4} l\left[\ln\left(\frac{4h}{d}\right)+\ln\left[\frac{l+\sqrt{l^2+d^2/4}}{l+\sqrt{l^2+4h^2}}\right]+\sqrt{1+\frac{4h^2}{l^2}}-\sqrt{1+\frac{d^2}{4l^2}}-2\frac{h}{l}+\frac{d}{2l}\right] \quad (1)$$

where $h$ is the height above ground, $d$ is the diameter, $l$ is the length, and each is in micrometer ($\mu$m) units. Each point of the bond wire has a different

Table 1　Diameter of the bond wire $\phi = 1$mil (24.5$\mu$m)　Average height above ground is $h = 300\mu$m.

| Length/$\mu$m | 500 | 600 | 700 | 800 | 900 | 1000 | 1100 | 1200 |
|---|---|---|---|---|---|---|---|---|
| Calculated inductance/nH | 0.328 | 0.399 | 0.471 | 0.545 | 0.619 | 0.694 | 0.769 | 0.845 |

height due to the arc shape, so we adopt the mean value of the height. Given $h = 300\mu$m, according to Eq. (1), we have a series values of inductance of bond wires with different lengths $l$. Table 1 shows some values of inductance, where $l$ is from 500 to 1200$\mu$m.

The loss of the bond wire in high frequency can be expressed as

$$R \approx \frac{l}{2\pi r\delta\sigma} \tag{2}$$

where $\delta$ and $\sigma$ are the skin depth and conductivity of the bond wire, respectively.

The connection model of bond wire can be simplified as an equivalent circuit in Fig. 2 (b). $C$ is the equivalent capacitance between the bonding pad and the GaAs substrate. The size of the pad is $80\mu\text{m} \times 80\mu$m, and its capacitance can be calculated using electromagnetic software. We obtained the single port $Y$ parameter using method of momentum (MoM) in Agilent ADS. For $C = \dfrac{\text{Im}(Y_{11})}{2\pi f}$, we have $C = 0.027$pF.

### 2.2　Hyperabrupt junction varactor diode

We selected a GMV9801 from Skyworks for frequency tuning. Figure 3 shows the equivalent circuit of the diode. Here, $R_S$ is the parasitic loss, which can be treated as zero when the varactor is in high quality, i.e. $R_S \approx 0$. The diode should be reverse biased, and the relationship between capacitance and tuning voltage is

$$C_V = \frac{C_{J0}}{\left(1 + \dfrac{V_R}{V_J}\right)^M} + C_P \tag{3}$$

where $C_{J0}$ is the zero-voltage junction capacitance, $V_J$ is the diffusion potential, $V_R$ is the reverse biased junction voltage, $M$ is the $C_V$ slope factor, and $C_p$ is the parasitic capacitance. Table 2 summarizes the model parameters of the Schottky-junction diode.

### 2.3　Circuit design and simulation

The circuit employs a capacitor series-feedback configuration, shown in Fig. 1. The introduction of $C_1$ at the source of the FET makes the real parts of input impedances at the gate and drain negative. In order to ease impedance matching, we determined the proper terminal impedances at the source and drain by

Table 2　Model parameters of the diode

| Parameter | $C_{J0}$/pF | $V_J$/V | $M$ | $C_P$/pF |
|---|---|---|---|---|
| Value | 1.12 | 5.5 | 2.3 | 0.03 |

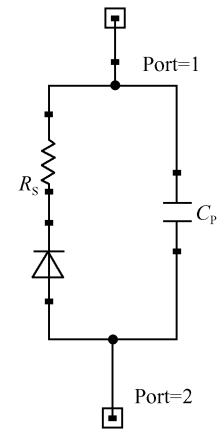


Fig. 3　Equivalent circuit of hyperabrupt-junction varactor diode

sweeping different values of $C_1$ during small signal $S$ parameter analysis. We divide Fig. 1 into 3 parts according to the dashed line. Under the circumstance of steady oscillation, the following relations exist:

$$\Gamma_s = \frac{1}{\Gamma_{in}}, \text{or } \Gamma_L = \frac{1}{\Gamma_{out}} \tag{4}$$

The two formulas in Eq. (4) are proven equivalent. Reflection coefficient $\Gamma$ can be transformed to an impedance parameter using the equation below:

$$Z = \frac{1 + \Gamma}{1 - \Gamma} Z_c \tag{5}$$

where $Z_c$ is the related characteristic impedance. For our capacitor series-feedback configuration, the output-matching network at the drain terminal must satisfy the conditions in Eq. (6) for oscillation startup.

$$R_L < -\text{Re}(Z_{out}), X_L = \text{Im}(Z_{out}) \tag{6}$$

where $R_L$ and $X_L$ are the real part and imaginary part of the terminal port, respectively, and $Z_{out}$ is the input impedance of the device. Therefore, after the introduction of feedback capacitor $C_1$, the terminal matching network to the drain and gate of the FET becomes our major design task.

The drain matching-network consists of on-chip inductors and capacitors ($L_1$, $L_2$, $C_2$ and $C_3$). $C_4$ is a capacitor to couple the RF signal to the off-chip part and isolate bias voltages between the varactor and pHEMT. $R_1$ is the bias resister for the gate of pHEMT, and $R_2$ is the bias resister for varactor. A large signal model of the pHEMT was developed for our circuit; the inductors and capacitors in the MMIC process present good lumped performance because their sizes are relatively small in comparison to the wavelength in the operating frequency, and the resonant circularity composed by varactor and bond-wire inductor has a high $Q$-factor. Harmonic-balance analysis was performed in Agilent's ADS. The length of the bond wire was swept to determinate proper inductance of the tuning network, and the inductance's value is base on Eq. (1). According to our design and

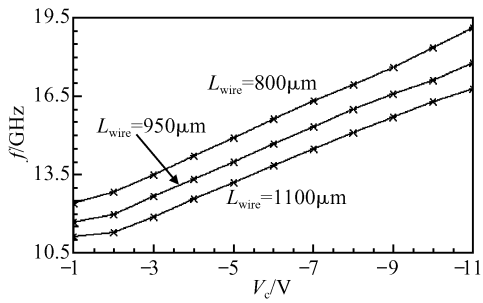


Fig. 4 VCO frequency simulation (Frequency versus tuning voltage and the length of bond-wire)

simulation, $l \approx 1000\mu$m is preferred to constrain the VCO's tuning range in the Ku band. Figure 4 shows the simulation results.

The simulated VCO's tuning characteristic shows quite good linearity, which owes much to the performance of the hyperabrupt junction tuning diode and the matching networks. The distribution effects will increase as operation frequency increases, which complicates the accurate prediction of the characteristic of matching networks in broadband circuits. Moreover, the intrinsic parasitic of the FET will be prominent in higher frequency bands, which aggravate internal feedback. For simplicity, we redraw Fig. 1 into the equivalent form shown in Fig. 5. The part looked into the gate usually has a capacitive impedance written as $C_a$. $C_a$ does not imply that it is equal to a capacitor, for it is frequency dependent. In fact, it represents the total effect of all the elements on right side of the dashed line, i.e., the feedback capacitor at the source, the FET's equivalent components, and the impedance of the output network that feeds back to the gate. The oscillation frequency of the VCO can be expressed as

$$f_{osc} = \frac{1}{2\pi}\sqrt{\frac{1}{L} \times \frac{1}{C_V + C_a}} \tag{7}$$

If the term $\sqrt{\frac{1}{C_V + C_a}}$ changes linearly with the tuning voltage, the output frequencies will also change

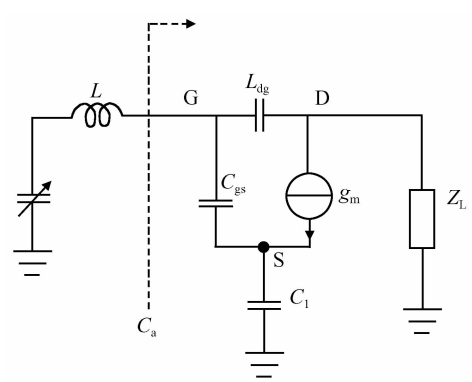


Fig. 5 Simplified equivalent of the VCO

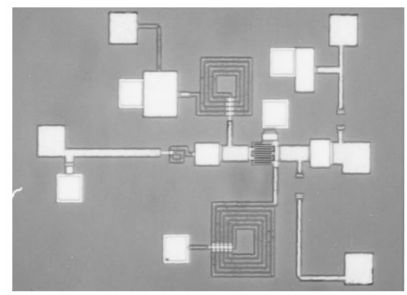

Fig. 6 Photo of the MMIC

linearly with the tuning voltage. The relationship between $C_V$ and the tuning voltage has been described in Eq. (3). The varactor parameter $M$ is 2.3, larger than 2, and can compensate the change of $C_a$, so $\sqrt{1/(C_V + C_a)}$ can change with tuning voltage approximately linearly.

The above discussion assumes that $L$ is constant, i.e., the inductor at the gate terminal is a pure lumped component. If the inductor is realized by an on-chip distributed component, the parasitic product will be more complicated. Therefore, a linear tuning design may be more difficult. Fortunately, the bond wire can be treated as a lumped inductor in our circuit, so the VCO shows linearity without an intentional design.

## 3 Circuit implementation and the VCO module

A 0.5μm pHEMT MMIC process was adopted to fabricate the chip portion of the VCO. The total gate width of the pHEMT is 400μm. The inductor was implemented in a spiral structure and the internal segment conductor is elevated by air bridge to connect to the outer conductor. A metal-isolation-metal (MIM) structure was adopted to realize capacitors. Epitaxy layer was used to realize the resisters, for large sheet resistance was required for bias. The photograph of the MMIC portion of the VCO is shown in Fig. 6, and its size is 1.2mm×0.9mm×0.1mm.

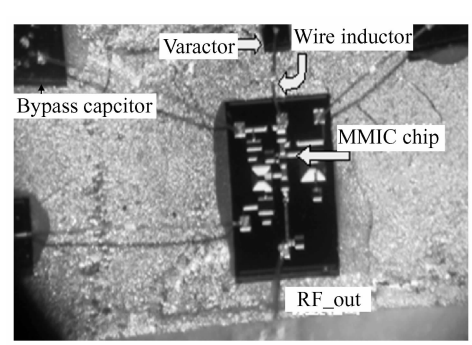


Fig. 7 Photo of the circuit assembly in a package

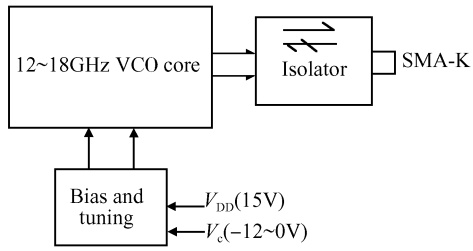


Fig. 8　Test structure of the VCO

The MMIC and varactor were integrated in a surface mount package. 1mil golden bond wire is used to connect the MMIC and varactor, and serves as a resonant inductor. 50pF chip capacitors are used to bypass the RF signal. Figure 7 is the internal photograph of the VCO in a ceramic package.

In order to make the test easier to perform, the VCO package was assembled in a module with a ferrite isolator and power management circuitry. The module connected the testing instrument with the SMA connector. The FET in the VCO was biased at 50mm/5V.

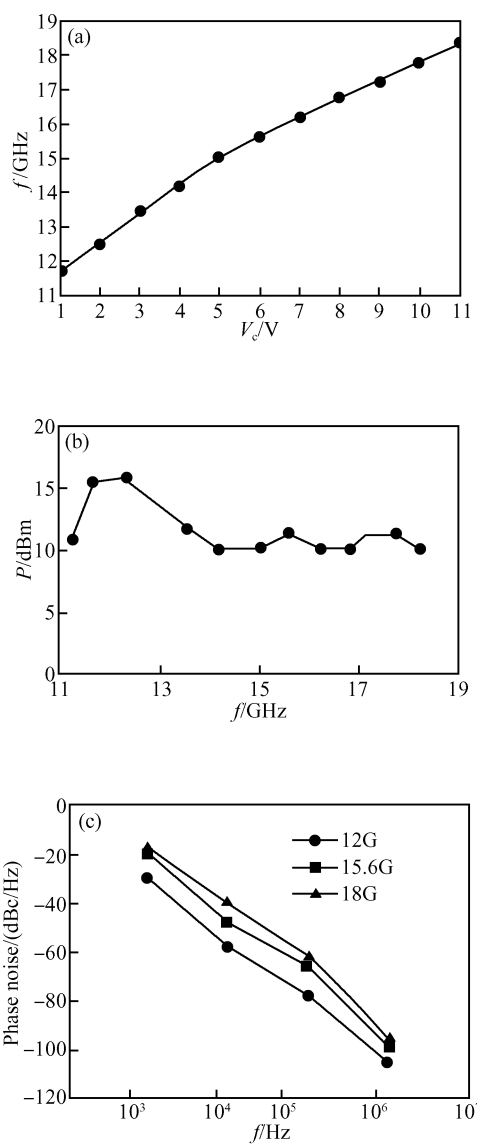


Fig. 9　Test results of the VCO　(a) Output frequency versus tuning voltage; (b) Power versus frequency; (c) Phase noise performance

## 4　Measurement results

The measurement results are shown in Fig. 9. Figure 9 (a) shows that the output frequency covers 12～18GHz with the tuning voltage varying from −11～−1V. Negative voltage is preferred, because the pad of the varactor is the anode and it is connect to the MMIC by bond wire inductor directly. The simulation predicts frequency performance quite well. The frequency linearity of the VCO is less than 2, which is not as good as the simulation, possibly because we did not optimize the matching network of the VCO for linear frequency design. The output power is greater than 10dBm in the frequency range, as shown in Fig. 9 (b). The result of phase noise is shown in Fig. 9 (c). The phase noise performance is better at lower frequency, i.e. −80dBc/100kHz/Hz at 12GHz, and deteriorates at higher frequency. The single-band phase noise is approximately −100dBc/Hz at 1MHz off carrier at all the oscillation frequency points.

## 5　Conclusion

A quasi-MMIC VCO covered Ku band was introduced. This circuit employs a hybrid assembly method to integrate an MMIC chip and a hyperabrupt-junction varactor into a package, which circumvents the on-chip integration high-quality varactor problem for MMIC that is incompatible with the conventional MMIC process. Meanwhile, the bandwidth and phase noise performances of the VCO are improved. In contract with the pure hybrid microwave integrated circuit process, the circuit is easy to implement, and has the merit of high uniformity in performances. The design concept can be used in other frequency bands and circuits easily and flexibly.

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# 基于准 MMIC 技术的 12～18GHz 宽带 VCO

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**摘要**：提出了一种基于准 MMIC 技术的 Ku 波段宽带压控振荡器. 该电路采用 MMIC 芯片和外加高 $Q$ 值的超突变结变容管的方式，实现了覆盖整个 Ku 波段的超宽带的振荡信号输出. 通过将 MMIC 技术与混合集成技术相结合的方法，大大降低了调试难度，更重要的是，克服了通用 pHEMT MMIC 工艺难于兼容高 $Q$ 值的变容管对超宽带设计 VCO 的限制，在相位噪声和调谐频率线性度方面都有较大改善. 该方法为微波、毫米波压控振荡器的设计提供了一个新的途径.

**关键词**：MMIC；宽带；VCO；Ku 波段；片外变容管；键合线电感
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