A CMOS Dynamic Comparator for Pipelined ADCs with Improved Speed/Power Ratio

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Abstract: This paper presents a fully-differential CMOS dynamic comparator for use in high-speed pipelined ADCs with low stage resolution. Because the architecture is based on the coupled current sources and differential input pairs, this comparator's threshold voltage can be adjusted to a desired level. Compared with traditional comparators, this one shows significant improvement in area, power, and speed. Fabricated in 0.35μm CMOS technology, it occupies only 30μm × 70μm. Simulation and measurement results indicate the comparator has a sampling frequency up to 1GHz with 2Vpp differential input signal range and only 181μW power consumption under a 3.3V supply. The speed/power ratio reaches up to 5524GS/J.

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1 Introduction

Wide application in power-sensitive devices makes the power consumption a critical constraint in most circuit designs, where analog-to-digital converters (ADCs) are usually independent components. For high-frequency input signal and high-resolution requirements, the pipelined ADC solution has proven to be a good choice for its speed and power advantages compared to other ADC architectures[1~3]. In most pipelined ADCs, one of the key building-blocks is a low-resolution flash quantizer, whose core is composed of comparators. Because of the repetition in pipelined architecture, this quantizer core has a dominant effect on the speed, accuracy, and power consumption of the whole ADC.

This paper presents a fully-differential CMOS dynamic comparator, whose power consumption, area, and speed characteristics manage a good trade-off. This comparator is based on the traditional resistive divider comparator. By modifying the circuit, this comparator greatly improves in speed and maintains the merits of small area and no static DC power. Considering that this comparator aims to be used in pipelined ADCs, its threshold voltage can be adjusted proportionally with the change of the ADC reference voltage. The ratio between the threshold voltage and the reference voltage can be easily set to a desired level by setting the size of the transistors in the circuit design.

2 Architecture considerations

The first consideration lies in the basic circuit topology. In the design of an ADC, fully differential analog signals are preferred for better power supply rejection and immunity to common mode noise. In line with this, the comparator should be fully differential too. Thus, both the input signal and the reference voltage should be differential.

The second consideration is based on the comparator's application environment. For a high-speed pipelined ADC, the comparator's speed is a critical parameter, whose optimization is of utmost importance. However, when the redundant sign digit (RSD) correction is used, offset tolerance of the comparator is greatly relaxed. For example, in the 1.5bit/stage architecture, an offset within $\pm V_{REF}/4$ is acceptable. Thus, for a desired comparator, use of the pre-amplification stage for high accuracy becomes unnecessary and might even compromise the speed. Consequently, for better speed performance, a comparator with a single stage is desirable, and should also reduce the power and area consumption.

Another important consideration is cost-efficiency. Several circuit topologies have been published in the past, and a major difference among these circuits

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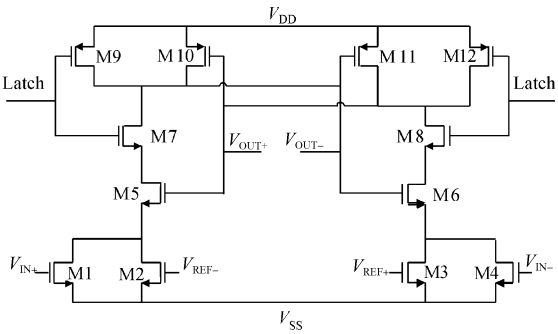

Fig. 1 Traditional dynamic comparator

is the type of latch employed. Some employ a static latch and others make use of a dynamic one. The former has DC power consumption all the time, but the latter only has power consumption when the latch signal is positive. Although the static latches have a smaller amount of kickback noise, the dynamic topologies are favorable after taking into account minimum power consumption.

Based on the above considerations, only the differential dynamic architectures will be focused on in our design. There are two kinds of dynamic topologies: switched capacitor and resistive divider. Due to the small area requirement, the switched capacitor architecture[4,5] is not preferred here.

3 Traditional comparator topologies

A widely-used dynamic comparator in the pipelined ADC is based on a differential sensing amplifier, presented in Fig. 1[1]. The nMOS transistor M1～M4 operate in the triode region, which form equal resistors R_1 (by M1 and M2) and R_2 (by M3 and M4). The conductance of R_1 and R_2 are given by

$$G_1 = \frac{1}{R_1} = kp\left[\frac{W_1}{L}(V_{IN+} - V_{TH}) + \frac{W_2}{L}(V_{REF-} - V_{TH})\right] \tag{1}$$

$$G_2 = \frac{1}{R_2} = kp\left[\frac{W_1}{L}(V_{IN-} - V_{TH}) + \frac{W_2}{L}(V_{REF+} - V_{TH})\right] \tag{2}$$

The comparator threshold voltage is given when G_1 equals to G_2. That is

$$V_{threshold} = V_{IN+} - V_{IN-} = \frac{W_2}{W_1}V_{REF} = \frac{W_2}{W_1}(V_{REF+} - V_{REF-}) \tag{3}$$

This implies that arbitrary thresholds can be set by adjusting the ratio of W_2/W_1. For instance, the comparator threshold levels at $\pm V_{REF}/4$ can be generated by setting the required ratio to 1/4.

No static power consumption and a linearly adjustable threshold are the most distinct advantages of this architecture. However, there is a drawback derived from the mismatch of the transistors. For the transistors M5 and M6, the transconductance can be written as

$$g_{m5,6} = \mu_0 C_{ox}\frac{W_{5,6}}{L}(V_{gs5,6} - V_{TH}) \tag{4}$$

At the beginning of the latching process, the transconductrances g_{m5} and g_{m6} are much larger than the conductance of the left and right input branches. This makes M5 and M6 dominant in determining the latching balance.

Any mismatch between the transistors M5 and M6 causes large offset voltages. Thus a few hundred millivolts offset often occurs when M5 does not match M6 perfectly. M7～M12 are not critical in terms of mismatch, because they are attenuated by M5 and M6. In addition, this comparator is sensitive to the asymmetry of load capacitance, so that extra inverters as buffer stages are needed.

4 Proposed comparator

In order to overcome the drawbacks of the above comparator architecture, a modification is introduced to make the comparator insensitive to mismatches. The basic idea is to keep all the transistors saturated except for those transistors used as switches. To achieve this, the transistors M5 and M6 in Fig. 1 are moved to the bottom of the schematic as current sources. Because these two current sources are switched on and off, there is no static current path between the supplies. Thus, this remains a dynamic topology without static power consumption. The phrase of "all the transistors in saturation region" makes sense only when the latch signal is positive. This fully differential dynamic comparator is shown in Fig. 2.

The following is the operation process of the comparator. In the beginning, the latch signal is low, and there is no current through M5 and M6. At that time, M9 and M12 are switched on. As a result, the outputs are shorted to V_{DD}. At the same time, M7 and M8 conduct all of the drains of the input transistors M1～M4, i. e. nodes A and B in Fig. 2, to V_{DD}. When the latch signal is high, the current sources M5 and M6 are switched on and enter the saturation region to conduct and M1～M4 also enter the saturation region. M5 and M6 determine the bias currents of the two differential pairs M1-M2 and M3-M4. The current division in the differential pairs and between the cross coupled branches determine the threshold voltage.

Suppose $W_1 = W_2$, $W_3 = W_4$ and $L_1 = L_2 = L_3 = L_4 = L$, the currents through M1～M4 and M5～M6 have the relationship given by[6]

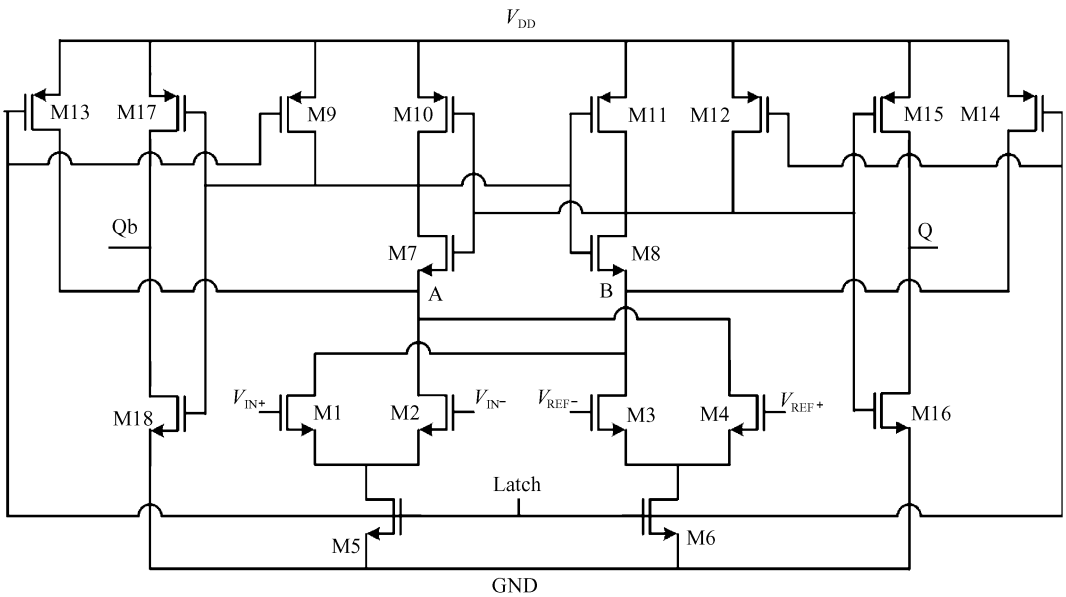

Fig. 2 Schematic of the proposed comparator

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L}(V_{IN+} - V_{IN-}) \times \sqrt{\frac{4I_{D5}}{\mu_n C_{ox}\frac{W_1}{L}} - (V_{IN+} - V_{IN-})^2} \tag{5}$$

$$I_{D4} - I_{D3} = \frac{1}{2}\mu_n C_{ox}\frac{W_3}{L}(V_{REF+} - V_{REF-}) \times \sqrt{\frac{4I_{D6}}{\mu_n C_{ox}\frac{W_3}{L}} - (V_{REF+} - V_{REF-})^2} \tag{6}$$

The flipping point of the comparator occurs when the current I_{D7} equals I_{D8}, for both output branches are equal. This relationship is described in Eq. (7):

$$I_{D7} = I_{D2} + I_{D4} \tag{7}$$

and Eq. (8):

$$I_{D8} = I_{D1} + I_{D3} \tag{8}$$

Thus, Equation (9) can be derived from Eqs. (7) and (8).

$$I_{D2} + I_{D4} = I_{D1} + I_{D3} \tag{9}$$

Substituting Eqs. (5) and (6) into Eq. (9), Equation (10) can be deduced:

$$\frac{W_1}{L}V_{IN}^2\sqrt{\frac{4I_{D5}}{\mu_n C_{ox}\frac{W_1}{L}} - V_{IN}^2} = \frac{W_3}{L}V_{REF}^2\sqrt{\frac{4I_{D6}}{\mu_n C_{ox}\frac{W_3}{L}} - V_{REF}^2} \tag{10}$$

where

$$V_{IN} = V_{IN+} - V_{IN-} \tag{11}$$

and

$$V_{REF} = V_{REF+} - V_{REF-} \tag{12}$$

Given the relationship of V_{IN} with V_{REF} and I_{D5} with I_{D6} separately, the relationship between W_3 and W_1 is fixed. Consequently, an arbitrary threshold point can be obtained by properly setting the values of W_3 and W_1.

In addition, because in Eq. (10), both W_1/L and W_3/L show up in the numerator and denominator, the change of W_1 or W_3 has less effect on the equality of Eq. (10). This implies that the effect of the mismatch is reduced.

These deductions are based on the square law. However, in the operation process of the comparator, the overdrive voltage and drain-source voltage of M5 and M6 could be fairly high. In order to avoid velocity saturation and keep the square law effective, the channel length of M5 and M6 should be long enough. Furthermore, the channel length of M1 ~ M4 should also be relatively long so that they still follow the square law.

In order to improve the comparator's speed performance, two extra transistors, M13 and M14, are added in this improved topology. These two pMOS transistors shorten the delay time when the drains of the four input transistors M1 ~ M4 reach V_{DD}, which greatly reduces the response time. Another important function of these two transistors is to help other transistors work in the saturation region after the rising edge of the latch clock. Simulation results show that this modification improves the comparator's performance. Some concrete analysis combined with experimental and simulation results will be demonstrated in section 5 to explain the improvement in speed performance.

In order to make the two output loads match, two inverters follow as the output buffers. They also greatly reduce the following circuits' effect on latch nodes, which are very sensitive.

The offset of this comparator is mainly determined by the offset of the differential pairs, which

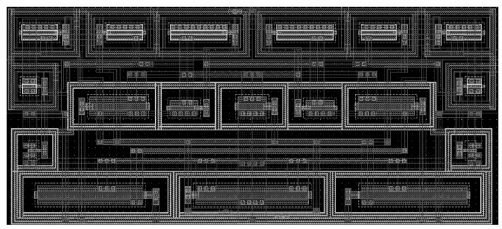

Fig. 3 Layout of the proposed comparator

can be given by

$$V_{os} = \left(\frac{V_{GS} - V_{TH}}{2}\right)^2 \left\{\left(\frac{\Delta R_D}{R_D}\right)^2 + \left[\frac{\Delta\left(\frac{W}{L}\right)}{\frac{W}{L}}\right]^2\right\}^2 + \Delta V_{TH}^2 \tag{13}$$

where ΔV_{TH} is the threshold mismatch, and ΔR_D is the resistance mismatch at the drain of the input transistors. The mismatch for the other transistors is not critical.

5 Experimental results and analysis

The comparator was designed and fabricated in standard 0.35μm 2P4M CMOS technology (Charted Semiconductor, Singapore). The layout of the circuit and the microphotograph of the chip are shown in Figs. 3 and 4, respectively. It should be noted that an internal buffer is added to drive the capacitive load introduced by the pads and probes.

The comparator's functional performance was tested under a 3.3V supply with a clock of 10MHz. Figure 5 shows the measured output waveforms when $V_{IN-} = 1.65$V and V_{IN+} is a sine wave with an amplitude of 300mV modulated on 1.65V DC voltage. For convenience, the threshold voltage is set to 0V. The input frequencies are 1, 2, 4MHz respectively and are shown in Figs. 5 (a), 5 (b), and 5 (c). The upper parts are the output signals of the comparator and the lower parts are the latch signals.

The comparator is expected to work for a clock frequency higher than 100MHz and an input signal frequency up to 50MHz. Figure 6 is the simulation results of the time response with 100MHz, 400MHz,

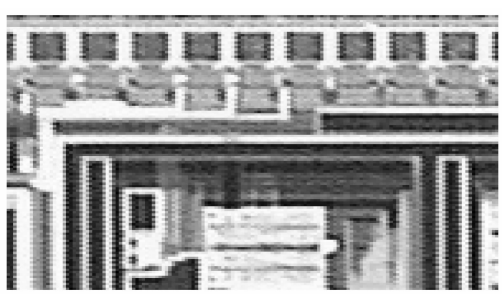

Fig. 4 Microphotograph of the chip (partial)

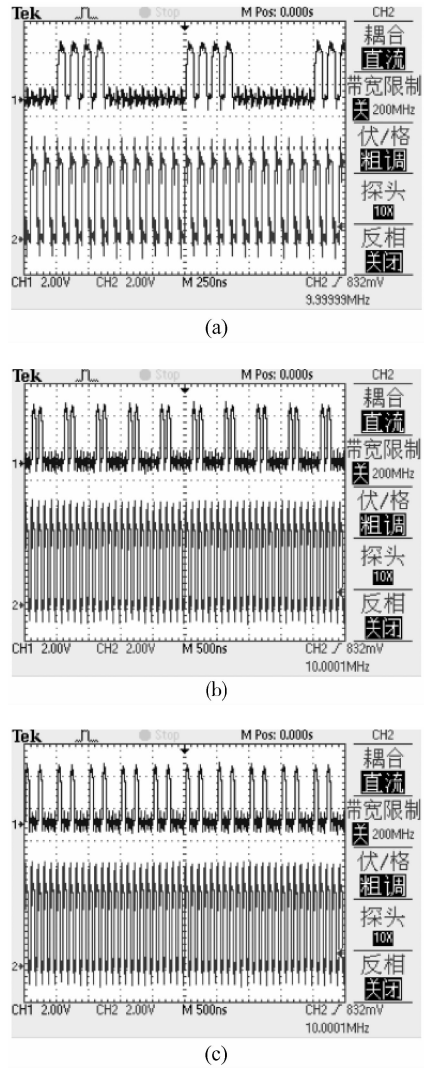

Fig. 5 Transient waveforms (a) Input signal frequency is 1MHz; (b) Input signal frequency is 2MHz; (c) Input signal frequency is 4MHz

700MHz and 1GHz latch clock signals. The figure implies that the comparator with M13 and M14 should have a sampling frequency of up to 1GHz, while without M13 and M14 the comparator fails to operate properly above 400MHz. The reason for the improvement in speed is that these two transistors switched on so quickly that the drains of the four input transistors reach V_{DD} immediately after the rising edge of the latch signal. This greatly reduced the impact of the parasitic capacitors related to nodes A and B.

In addition to optimization of the circuit architecture, the optimized regeneration time constant also needs to be considered to improve the speed performance. The regeneration time constant τ can be given by

$$\tau \propto \frac{C_D}{g_m} \tag{14}$$

where g_m is the initial transconductance of nMOS transistors. C_D is the total capacitance in A and B. In

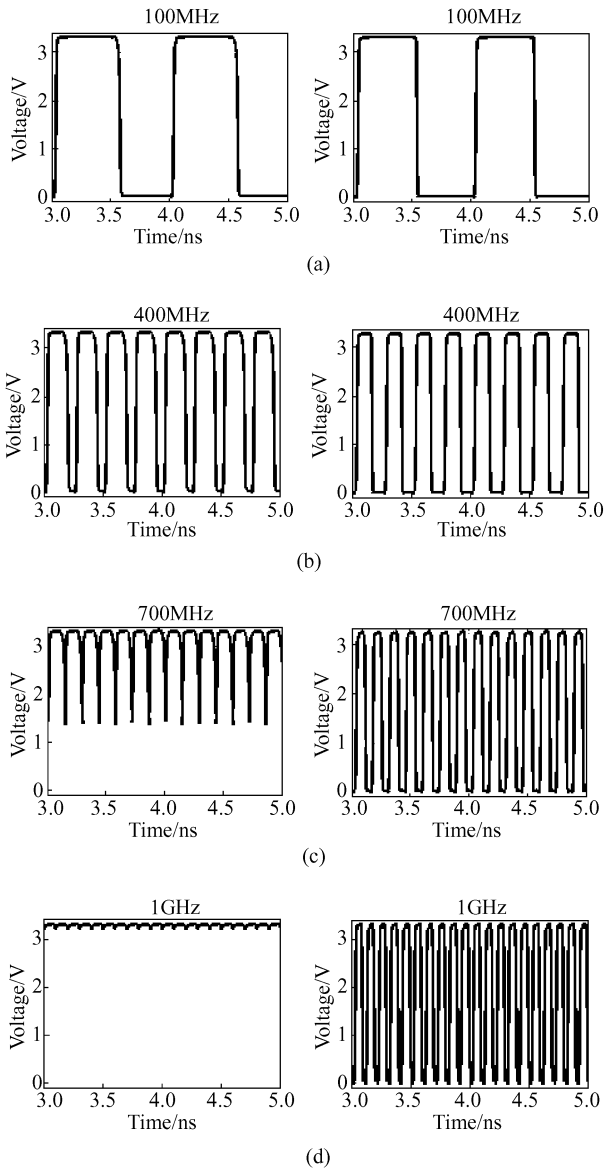

Fig. 6　Transient response of the comparator　In these figures, the former is without M13 and M14 and the latter is with M13 and M14.

order to obtain a speed as high as possible, C_D should be larger and g_m should be smaller. In terms of a fixed ratio of W_1 and W_3, the currents are decided by M5 and M6. In order to maximize the g_m in Eq. (14), the currents through M 5 and M 6 should be larger. This

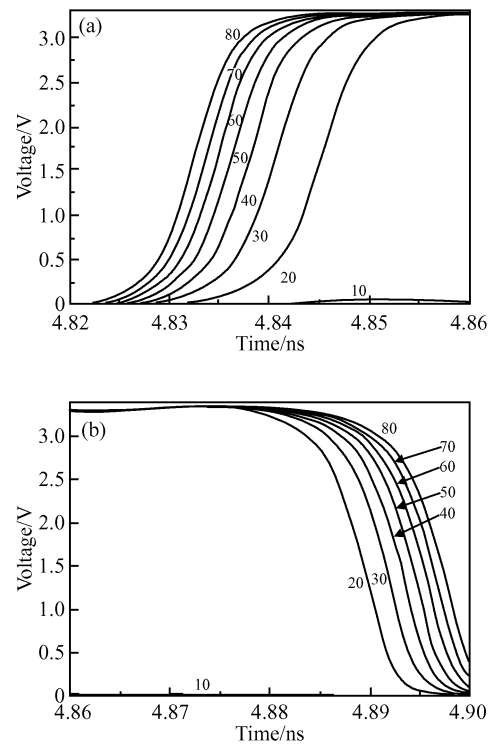

Fig. 7　Relationship between the regeneration time and ratio of $(W/L)_{M5}/(W/L)_{M6}$ with 1GHz latch clock　(a) Rising edge; (b) Falling edge

can be realized by adjusting the value of W/L.

Simulation results show the regeneration time has little relation with the absolute value of $(W/L)_{M6}$, but changes with the ratio of $(W/L)_{M5}/(W/L)_{M6}$. The simulation result is shown in Fig. 7, which illustrates the regeneration time's variations with the transistors ratio of W/L.

Offset was tested under the assumption that this comparator was used in a 2Vpp input range and 1.5bit/stage pipelined ADC, i.e., the threshold voltage is 250mV. A fully-differential signal was added as the input signal, with its common-mode voltage level varying from 1.15 to 2.15V. The measurement results are shown in Table 1 and Fig. 8. The optimum common mode voltage with the smallest offset occurs at 1.4V.

Table 1　Measured offset

Input CM voltage/V	Input signal when comparator flips /V			Offset /mV	Input CM voltage/V	Input signal when comparator flips /V			Offset /mV
	V_{IN+}	V_{IN-}	$V_{IN}=V_{IN+}-V_{IN-}$			V_{IN+}	V_{IN-}	$V_{IN}=V_{IN+}-V_{IN-}$	
1.20	1.388	1.012	0.376	126	1.70	1.780	1.620	0.160	−90
1.25	1.414	1.086	0.328	78	1.75	1.826	1.674	0.152	−98
1.30	1.446	1.154	0.292	42	1.80	1.874	1.726	0.148	−102
1.35	1.482	1.218	0.264	14	1.85	1.922	1.778	0.144	−106
1.40	1.520	1.280	0.240	−10	1.90	1.970	1.830	0.140	−110
1.45	1.560	1.340	0.220	−30	1.95	2.018	1.882	0.136	−114
1.50	1.602	1.398	0.204	−46	2.00	2.066	1.934	0.132	−118
1.55	1.644	1.454	0.190	−60	2.05	2.116	1.984	0.132	−118
1.60	1.688	1.512	0.176	−74	2.10	2.166	2.034	0.132	−118
1.65	1.734	1.566	0.168	−82	2.15	2.214	2.086	0.128	−122

Table 2 Performance comparison of the proposed comparators

Performance	Ref.[7]	Ref.[8]	Ref.[9]	Ref.[9]	This design
Architecture	Preamp	Improved preamp	Capacitive differential pair	Resistive divider	Differential pair
Technology	0.35μm CMOS	0.35μm CMOS	0.35μm BiCMOS	0.35μm BiCMOS	0.35μm CMOS
Supply voltage/V	3.3	1.5	3	3	3.3
Input range/Vpp	2	3	—	—	2
Offset/mV	50	35	75	290	$<$200
Sampling frequency/GHz	1.0	$<$0.2	$>$0.1	$>$0.1	1
Area/μm^2	—	—	2800	1200	2100
Power consumption/μW	2000	69	810 @100Msample	320 @100Msample	181 @100Msample
(Speed/Power)/(GS/J)	500	2896	—	—	5524

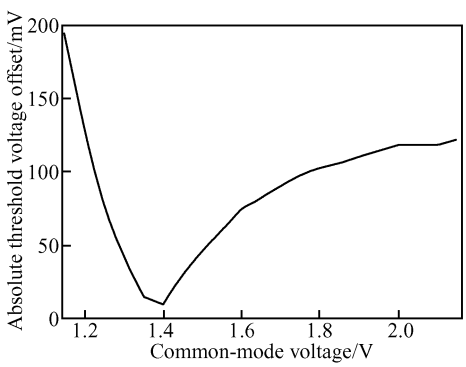

Fig.8 Offset under different common-mode input voltages

6 Performance summary and comparison

The performance results are listed in Table 2. A comparison between the proposed comparator and those in literature is also summarized in Table 2. Besides the characteristics mentioned above, the ratio of the speed to power consumption can be used as a performance metric of the comparator. The Speed/Power metric for the proposed comparator is 5524GS/J. Compared with the commonly used static comparators, our design has a significantly improved speed/power ratio.

7 Conclusion

In this paper, a dynamic comparator architecture suitable for high-speed applications is presented. It consists of two cross coupled, switched current sourced differential pairs loaded with a latch. The threshold voltage of the comparator can be adjusted with the dimensions of the input and current source transistors. The comparator was fabricated in 0.35μm standard CMOS technology. The results demonstrate that the proposed comparator has a good speed characteristic and uses low power and small area. It is inherently suitable for high-speed and power sensitive pipelined ADCs.

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一种用于流水线结构 ADC 中改进速度/功耗比的 CMOS 动态比较器

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摘要：提出了一种适用于高速、单级低分辨率流水线结构 ADC 的全差分动态比较器.由于采用了电流源耦合和差分对输入结构，比较器的翻转阈值电压可以设计为任意值.与传统的比较器相比，该比较器较好地兼顾了面积、功耗以及速度等方面，在这些方面有了较大的改进.该比较器在 0.35μm CMOS 工艺下完成流片，面积为 30μm×70μm.仿真和测试结果表明，该比较器可以在 2Vpp 的输入信号和 1GHz 的时钟频率下工作，在 3.3V 的电源电压下，功耗仅为 181μW.速度/功耗比达到了 5524GS/J.

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