An 80dB Dynamic Range ΣΔ Modulator for Low-IF GSM Receivers

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Abstract: A high-resolution, 200kHz signal bandwidth, third-order single-loop single-bit ΣΔ modulator used in low-IF GSM receivers is presented. The modulator is implemented with fully differential switched capacitor circuits in standard 0.6μm 2P2M CMOS technology. The modulator uses two balanced reference voltages of ±1V, and is driven by a single 26MHz clock signal. The measurement results show that, with an oversampling ratio of 64, the modulator achieves an 80.6dB dynamic range, a 71.8dB peak SNDR, and a 73.9dB peak SNR in the signal bandwidth of 200kHz. The modulator dissipates 15mW static power from a single 5V supply.

Key words: sigma-delta modulator; analog-to-digital conversion; switched-capacitor; operational amplifiers
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1 Introduction

With the development of CMOS technology and wireless communications, it has become a general trend to integrate a whole RF communication system on an SOC[1] to further reduce the cost. Data converters, as the bridge between the analog and digital world, are necessary for wireless SOC. ΣΔ ADC, with the over-sampling and noise-shaping techniques, can achieve high resolution while relaxing the requirement for analog circuits, which is very suitable for SOC design in sub-micron CMOS technology. This paper presents a ΣΔ modulator design for GSM receivers with low-IF structure, which requires more than an 80dB dynamic range (DR) within the signal bandwidth of 200kHz.

According to the implementation method of integrator in modulators, ΣΔ modulator can be classified in two categories: discrete-time[2] and continuous-time[3]. Continuous-time ΣΔ modulators, relaxing the speed requirement of OPA, can be designed with higher sampling frequencies and thus handle higher signal bandwidth. But, they are sensitive to non-idealities of the CMOS circuits, such as jitter[4], excess loop delay[4] and process variation[5]. In contrast, discrete-time ΣΔ modulators, using switched-capacitor integrators whose accuracy is insensitive to these non-idealities of the circuit, can achieve high resolution[6]. This paper proposes a discrete-time ΣΔ modulator for a low-IF GSM receiver, which has an 80dB dynamic range with a 200kHz signal bandwidth.

2 System design and considerations

2.1 Structure and loop filter design

There are two structures for building high-order ΣΔ modulators: a single-loop[7] and a cascade (MASH)[8]. For a MASH structure, two or three low-order loops are cascaded. The stability of MASH is superior to single-loop structures, but the matching requirement between the coefficients of analog and digital integrators forces the operational amplifiers (OPA) used in an analog integrator to have a high open-loop gain, which is more difficult to implement in sub-micron technology. Furthermore, the low-order loop in MASH structures may induce idle tone, which will greatly raise the noise floor of the modulator. Therefore, the single-loop structure is adopted in the proposed ΣΔ modulator for its low sensitivity to OPA's open loop gain. The sampling frequency is set to 26MHz and the oversampling ratio is 64.

Figure 1 shows the third-order, single-loop feedback structure of the proposed ΣΔ modulator. This architecture is a general version for all of the third-order feedback structures without signal scaling. The coefficient of the last integrator, b_3, does not affect the whole SNR performance if the offset of the quantizer can be ignored since the offset has very little influence on SNDR. Thus, only b_1 and b_2 are independent variables when choosing a set of proper NTF coefficients, which almost determine the whole performance of the modulator.

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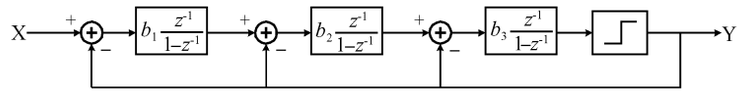

Fig. 1　Third-order single-loop feedback structure

The coefficients were determined by experimenting with all possible numbers from {1/6, 1/5, 1/4, 1/3, 1/2, 0.8, 1}. We chose $b_1 = 1/4$, $b_2 = 1/3$ and b_3 is set to 1/3 in order to limit the output swing of the last integrator to less than ±1.5V.

The MATLAB simulation results are illustrated in Fig. 2. The peak SNDR is 86dB and overload level is −3dBFs. When the input signal reaches overload level, the output swing of each integrator is less than ±1.5V, which is easy to implement with a 5V power supply. Thus, the signal scaling process is unnecessary.

2.2　Allocation of capacitors and noise

The noise generated by the ΣΔ modulator includes quantization noise and circuit noise. The quantization noise can be calculated by HSPICE or MATLAB simulation. Circuit noise, containing sampling capacitor noise and active device noise, should be estimated before designing circuits.

According to the transfer function for the modulator derived by Mathematica, input referred noise is dominated by:

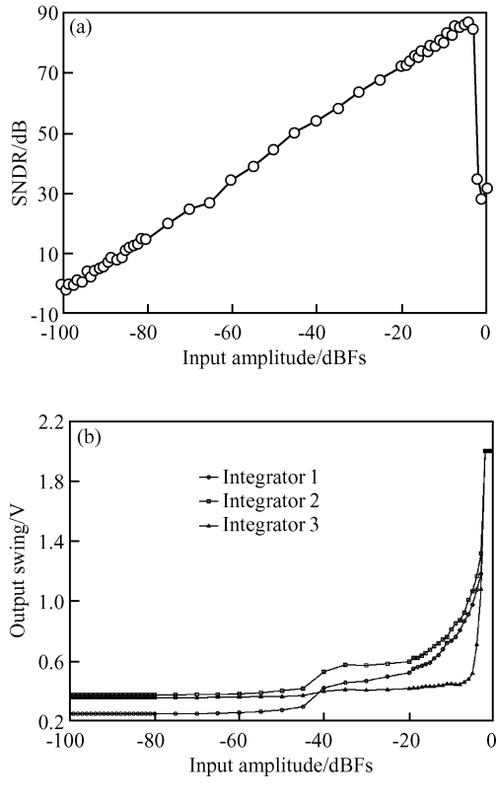

Fig. 2　MATLAB simulation results　(a) SNDR versus input amplitude; (b) Output swing of each integrator

$$N_{in}(z) = N_1(z) + \frac{1}{b_1}(1 - z^{-1})N_2(z) + \frac{1}{b_1 b_2}(1 - z^{-1})^2 N_3(z) \quad (1)$$

where N_1 represents the input referred noise of the first integrator, N_2 is that of the second integrator, and N_3 is that of the third. Furthermore, the contribution of each noise source can be derived:

$$S_{N_{in}} = \frac{1}{M} S_{N_1} + \frac{1}{b_1^2} \times \frac{\pi^2}{3M^3} S_{N_2} + \frac{1}{b_1^2 b_2^2} \times \frac{\pi^4}{5M^5} S_{N_3} \quad (2)$$

With $M = 64$, $b_1 = 1/4$, $b_2 = 1/3$, the noise power of the 2nd and 3rd integrators is attenuated by 1.3×10^{-2} and 1.7×10^{-4}, respectively, relative to the noise introduced by the 1st integrator.

The value of the sampling capacitor can be determined as follows. Considering the −3dBFs overload level, to guarantee the modulator's dynamic range is more than 80dB, the noise floor is estimated to be −85dBFs. The quantization noise floor estimated by simulation is −92dBFs, which requires the sum of sampling noise and amplifier noise to be less than −86dBFs. If it is assumed that sampling noise and amplifier noise are equal, the sampling noise must be less than −89dB. According to the equation of sampling noise power in an integrator[9]:

$$\overline{v_{ns}^2} = \frac{kT}{C_s}\left(1 + \frac{p_A}{p_s}\right) \times 2 \quad (3)$$

where p_A is the bandwidth of OTA and p_s is the time constant of the switch. If $p_A/p_s = 0.5$ is adopted, C_{s1} must be greater than 0.16pF. To guarantee the noise power due to the 2nd and 3rd integrators is less than 1/10 and 1/100 of noise from the 1st integrator, C_{s2} must be greater than 20fF and C_{s3} must be at least 3fF.

Finally, to ensure enough margins for noise and matching, sampling capacitors are set to:

$$C_{s1} = 0.5\text{pF}$$
$$C_{s2} = 0.2\text{pF}$$
$$C_{s3} = 0.2\text{pF}$$

3　Circuit design and implementation

3.1　Integrator design

Integrators are the main block building loop filter of the ΣΔ modulator. A switched capacitor integrator, whose structure is illustrated in Fig. 3, is adopted due to its advantages of high accuracy and low sen-

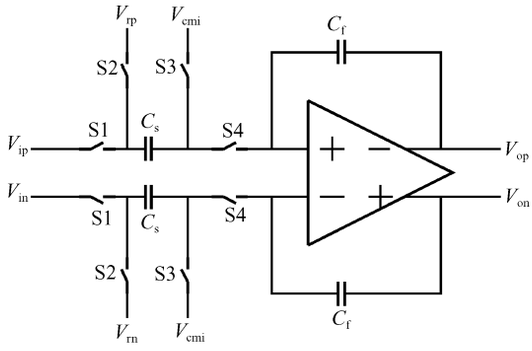

Fig. 3 Structure of the switched-capacitor integrator

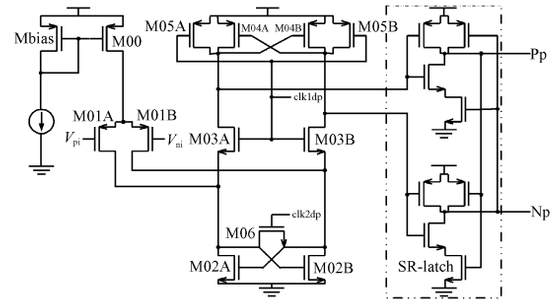

Fig. 4 Schematic of the comparator

sitivity to clock jitter. As shown in Fig. 3, the sampling capacitor of DAC is combined with the signal capacitor to save area because the feedback factor of DAC is the same as the signal gain of the integrator. To eliminate the charge injection and clock feed-through effect, a non-overlapped clock and bottom-plate sampling are employed.

The operational transconductance amplifier (OTA) is very important to the integrator. The requirement of OTA's output swing and open-loop gain are derived from MATLAB simulation. An output swing over ±1.5V and an open-loop gain of 60dB are needed. From the simulation results in Ref. [10], the closed-loop bandwidth is set to 6 times the sampling frequency. Based on these specifications, the folded-cascode structure and a switched capacitor common mode feedback circuit are chosen for OTA design.

The simulation results of the OTA are listed in Table 1, where the circuit is verified in 3 different corners.

3.2 Switch design

There are two kinds of switches used in the modulator, a CMOS switch and an nMOS switch, which are connected with variable signals and fixed voltages, respectively. The sampling switch in front of the ΣΔ modulator, the most important switch in limiting the system's performance, also uses a CMOS switch. Although the bootstrapped switch used in some references[11] has better linearity, a CMOS switch saves area and it has been verified by simulation that the performance will not be degraded if the frequency of the input signal is far below the clock frequency. The size of each switch is determined by resistance simulation to guarantee the time constant of the switch and sampling capacitor are less than 1/15 of a sampling period.

Table 1 AC simulation results of the OTA

Corner	Temperature /℃	Open-loop gain/dB	GBW /MHz	Phase margin /(°)
TT	50	64	326	68
SS	120	66	257	65
FF	0	61	411	69

3.3 Comparator design

The comparator used in the modulator is shown in Fig. 4. The function of differential input pairs, M01, is to isolate the following digital circuits and reduce the kickback effect to the third integrator. M02 and M03, forming a positive regenerative loop, amplify the small signal to full voltage swing. The following RS flip-flop, made up of two NAND gates, prevents mistaken actions of the comparator from inflecting the DAC.

3.4 HSPICE simulation result

The proposed modulator is designed in CSMC 0.6μm 2P2M CMOS technology. The power supply is 5V. The circuit of whole modulator is verified by HSPICE transient simulation and the results are illustrated in Fig. 5. Figure 5 (b) shows that the peak SNDR achieves 86dB and the overload level is −3dBFs, which are identical to MATLAB simulation results.

3.5 Layout design

The modulator's layout is shown in Fig. 6. To keep the environment of differential signals identical, a fully symmetrical floorplan is used. The digital power supply and analog power supply are isolated in the chip and connected to individual supplies outside the chip. The protection ground, located between analog circuits and digital circuits, is also connected separately outside the chip. The core area of the modulator is 0.9mm × 2mm and the total area including pads is 2mm × 2mm.

4 Measurement results

The modulator was fabricated in CSMC with 0.6μm 2P2M CMOS technology. The test PCB and its block diagram are illustrated in Figs. 7 and 8, respectively. The chip in the middle of the PCB is the test

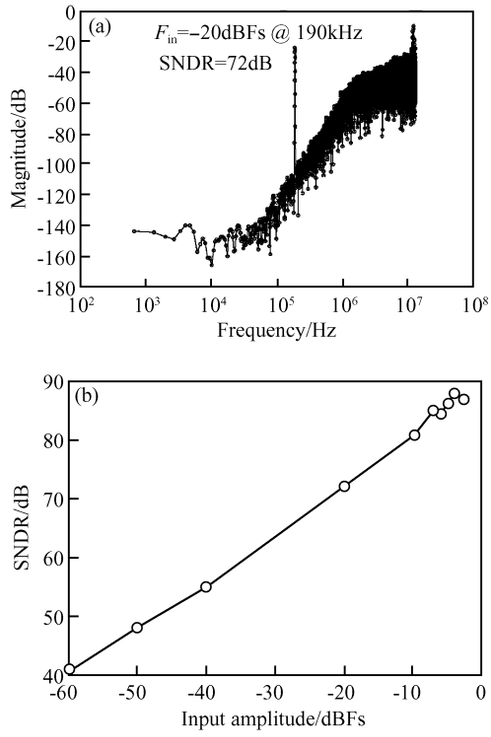

Fig. 5　HSPICE simulation results　(a) Output spectrum from a −20dBFs sinusoidal signal input; (b) SNDR versus input amplitude

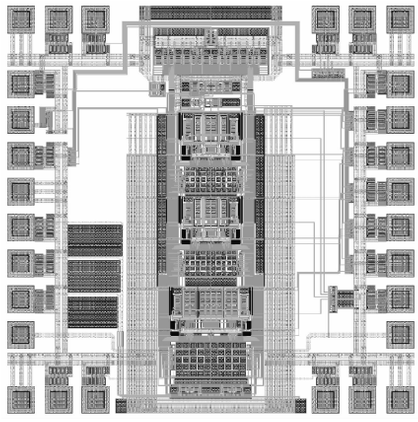

Fig. 6　Layout of the modulator

modulator. The 1bit digital output is collected by an Agilent logic analyzer and sent to MATLAB to perform FFT. The modulator works at 26MHz clock frequency under a 5V supply. The analog circuit consumes 15mW.

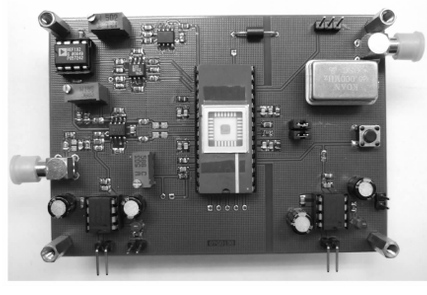

Fig. 7　Photograph of the test board

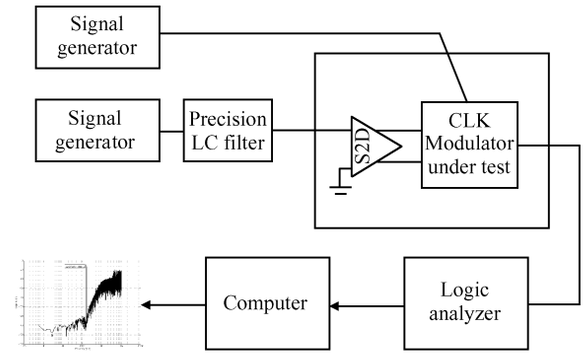

Fig. 8　Block diagram of the test circuit

Figure 9 illustrates the measurement results. When no signal is fed to the modulator, the output spectrum shows that the noise floor of the modulator is −84.2dBFs. The overload level is −3.6dBFs under

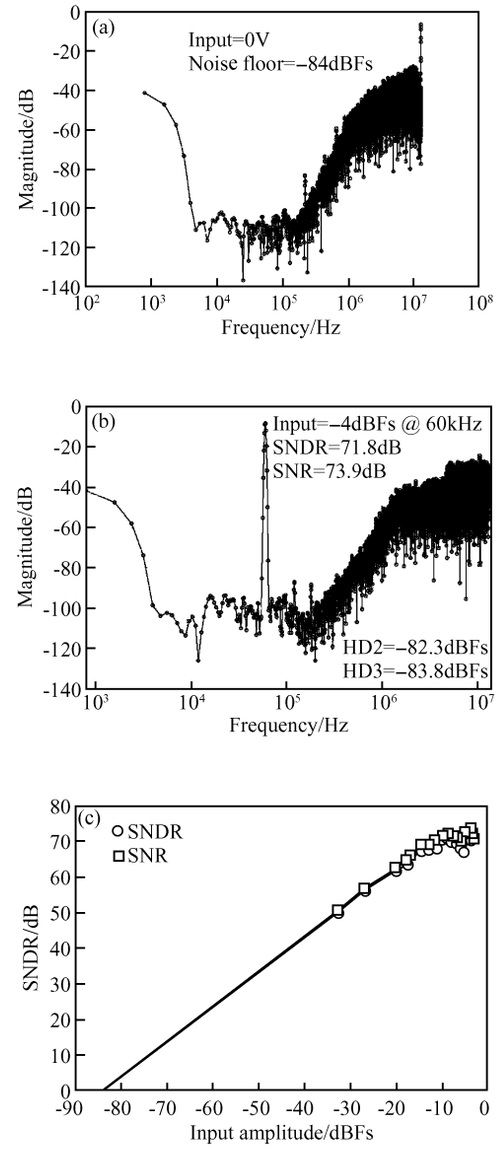

Fig. 9　Measurement results　(a) Noise floor; (b) Output spectrum from a −4dBFs sinusoidal signal input; (c) SNDR versus input amplitude

Table 2 Performance of the modulator

Specification	Measurement result
Power supply	5V
Reference voltage	±1V(diff)
Signal bandwidth	200kHz
Sampling frequency	26MHz
Overload level	−3.6dBFs
Dynamic range	80.6dB
Peak SNR	73.9dB
Peak SNDR	71.8dB
Static power consumption	15mW

a 60kHz sinusoidal test signal and hence the dynamic range of the modulator is 80.6dB. The peak SNDR and SNR achieve 71.8dB and 73.9dB when the amplitude of input signal is −4dBFs where the full scale voltage is ±1V. The frequency of the test signal is chosen as 60kHz to guarantee the third-order harmonic distortion falls into the 200kHz signal band, which makes the measurement more accurate. An abstract of the measured performance of the modulator is listed in Table 2.

Table 3 compares the performance of the proposed modulator with the modulators reported by mainland research organizations.

Table 3 Performance comparison

Author	Publication	Technology	Signal bandwidth /kHz	Power supply /V	Current consumption /mA	Dynamic range /dB
Li Luosheng	Doctor Thesis (2005)	0.18μm	1000	1.8	60	82
Chen Jianqiu, *et al*.	CJS(2007.02)	0.18μm	250	1.8	9.3	85
Cao Ying, *et al*.	CJS(2007.08)	0.18μm	96	1.8	5.4	92
This work		0.6μm	200	5	3	80.6

5 Conclusion

A third-order, single-loop single-bit feedback ΣΔ modulator for low-IF GSM receivers is described. The modulator can handle a signal of 200kHz bandwidth under a 26MHz sampling frequency, with an oversampling ratio of 64. The circuits are constituted by fully differential switched capacitor integrators, a dynamic comparator, and some assistant digital circuits. The test chip was fabricated in CSMC with 0.6μm 2P2M CMOS technology and occupies 2mm×2mm. The chip was tested and the measurement results show that the modulator consumes 15mW static power and its dynamic range reaches 80.6dB. The peak SNDR and SNR achieve 71.8dB and 73.9dB, respectively.

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80dB 动态范围，用于低中频结构 GSM 接收机的 ΣΔ 调制器

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摘要：介绍了一个 200kHz 信号带宽、用于低中频结构 GSM 射频接收机的高精度 ΣΔ 调制器.该调制器采用 3 阶单环单比特的结构，电路使用全差分开关电容结构实现，并在 0.6μm 2P2M CMOS 工艺下流片验证.调制器使用全差分 ±1V 参考电压，工作在 26MHz 采样频率，过采样率为 64.测试结果表明，在 200kHz 信号带宽内，调制器达到 80.6dB 动态范围，峰值 SNDR 达到 71.8dB，峰值 SNR 达到 73.9dB.整个调制器电源电压为 5V，静态功耗为 15mW.

关键词：ΣΔ 调制器；模数转换；开关电容；运算放大器

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