Design of a 4.224GHz Quadrature LC-VCO*

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Abstract: A 4.224GHz quadrature voltage-controlled oscillator (QVCO) applied in MB-OFDM UWB synthesizers is implemented in 0.18μm RF-CMOS technology. An improved structure of the QVCO is presented for better phase noise. A novel configuration of a MOS varactor is designed for good linearity of K_{vco}, as well as a new digital capacitor controlled array topology with lower parasitic capacitance and lower R_{on}. Measurement results show a phase noise of -90.4dBc/Hz at 100kHz offset and -116.7dBc/Hz at 1MHz offset from a carrier close to 4.224GHz. The power dissipation is 10.55mW from a 1.8V supply.

Key words: UWB; quadrature VCO; phase noise; varactor; DCCA; quadrature performance
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1 Introduction

The quadrature voltage-controlled oscillator (QVCO) designed in this paper is applied in UWB[1] synthesizers, which should work at 4.224GHz. The performance of the QVCO is one of the key factors determining the performance of the synthesizer, and the QVCO is also one of the more complicated modules to design in the synthesizer.

A great deal of research has been done on QVCO design. References [2~4], among others, presented their own topology of QVCO with a detail analysis of the QVCO. Comparing QVCO with differential VCO, one disadvantage of the QVCO is that there are two more MOSFETs with noise sources in QVCO, so the phase noise performance is worse than the differential VCO. This raises a challenging design issue of how to improve the phase noise of QVCO.

The basic topology of the QVCO presented here can be found in Ref. [5], but modifications are applied in order to improve phase noise performance. A novel configuration for the MOS varactor is designed for good linearity of K_{vco}, as well as a new digitally controlled capital array topology with lower parasitic capacitance and lower R_{on}. This QVCO has better phase noise performance than traditional QVCOs. By changing the connection of the MOS varactor, better linearity of K_{vco} is obtained. Furthermore, a new digitally controlled capital array (DCCA) topology with lower parasitic capacitance and lower R_{on} is designed, which will not degrade the Q of the LC-tank distinctly.

A comparison between the QVCO in this paper with the classical QVCO in Ref. [2] is carried out. Finally, the design of the 4.224GHz QVCO is presented.

2 Comparison of different QVCOs

As introduced in section 1, since the existence of coupling MOSFETs, the phase noise of QVCO has been worse than that of differential VCO. Therefore, improving the phase noise of QVCO is a great design challenge.

The advantage of the QVCO used in this paper is demonstrated by comparing it with the classical QVCO[2]. The two QVCO topologies are shown in Fig. 1, in which Figure 1 (a) is a classical QVCO, while Figure 1 (b) is the QVCO used in this paper. The difference between the two QVCOs is that the cross-coupled MOSFETs and coupling MOSFETs of a differential VCO M1, M2, M3, M4 and M5, M6, M7, M8 in the QVCO use a common current source in Fig. 1 (a), while Figure 1 (b) is derived from Fig. 1 (a) by simply connecting the cross-coupled M2, M3, M6, M7 and the coupling M1, M3, M5, M8 of the QVCO, respectively.

For the comparability, all the parameters are the same in the two QVCOs, except the current distributed to each current source. The current of QVCO in Fig. 1 (a) is averaged between the two current sources, while the QVCO in Fig. 1(b) is not, but the total current of the two QVCOs is equivalent. In one signal period, assuming that the switching effect of

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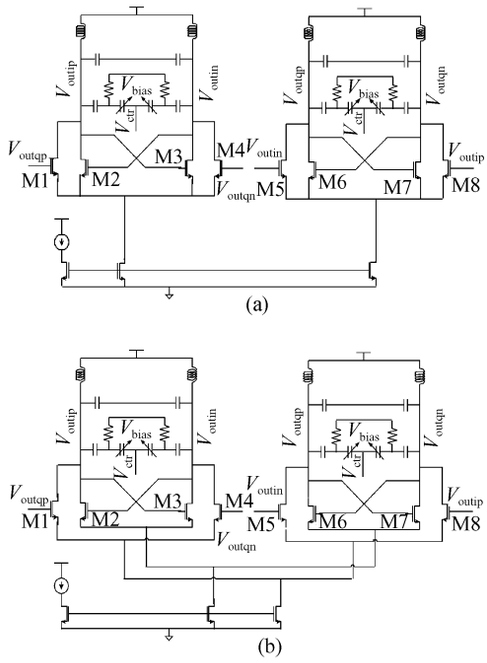

Fig. 1 Topology of the two QVCOs (a) Classical QVCO; (b) QVCO used in this paper

the coupling and cross-coupled MOSFETs is ideal, the MOSFETs working state in the two QVCOs is shown in Fig. 2. According to the characteristics of current source common mode node, the voltage waveforms are the same in phases 1 and 3, and 2 and 4. Therefore, the analysis will emphasize phases 1 and 2. In Fig. 2, the upper-left is the switch-on status of QVCO in Fig. 1(a), and the lower-left is the switch-on status of QVCO in Fig. 1(b), in which the solid line denotes the switch-on of MOSFETs while the dashed line denotes the cut-off of MOSFETs. The assumed waveforms of the four outputs are on the right.

As shown in Fig. 2, when the MOSFET is on and the trend of the gate waveform is increasing (defined as V_r), the non-linear transfer function of the cross-coupled MOSFETs and coupling MOSFETs to the current common point is given by H_{r1} and H_{r2}, respectively. If the gate waveform is decreasing (defined as V_f), the non-linear transfer function is given by H_{f1} and H_{f2}, respectively. The waveform of the current common mode node in phases 1 and 2 satisfies the following equations, respectively:

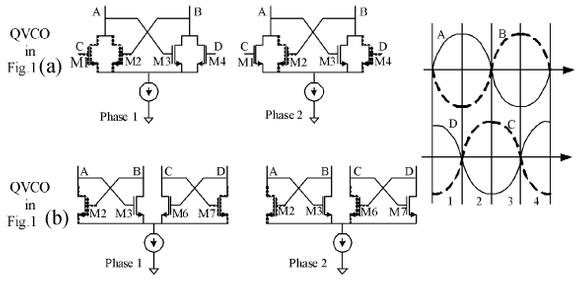

Fig. 2 MOSFETs working states in two half-QVCOs

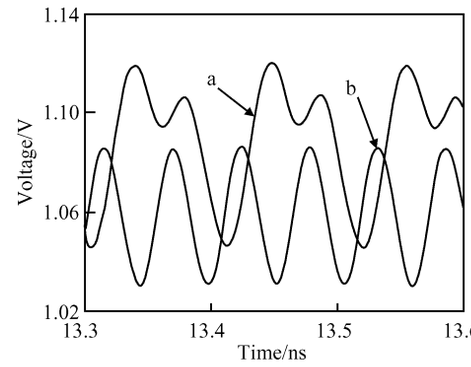

Fig. 3 Voltage of current common mode node

$$V_1 = H_{r1}(V_r) + H_{f2}(V_f) \quad (1)$$

$$V_2 = H_{r2}(V_r) + H_{f1}(V_f) \quad (2)$$

The waveforms of the current common mode node in Fig. 1(b) in phases 1 and 2 are the same. The waveforms of current common mode nodes of cross-coupled MOSFETs and coupling MOSFETs satisfy the following equations, respectively:

$$V_c = H_{r1}(V_r) + H_{f1}(V_f) \quad (3)$$

$$V_q = H_{r2}(V_r) + H_{f2}(V_f) \quad (4)$$

The simulated waveforms of the current common mode node of the cross-coupled MOSFETs in Figs. 1 (a) and 1 (b) are shown in Fig. 3.

According to Hijimiri's phase-noise theory[6,7], the noise of the current source would up-convert into phase noise by the mixing effect, which is proportional to the impulse sensitivity function (ISF), which can be expressed as:

$$\Gamma(\omega_0 t) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 t + \theta_n) \quad (5)$$

in which, c_n is declining. As shown above, the frequency of current common mode node in Fig. 1(a) is $2\omega_0$, while in Fig. 1(b) it is $4\omega_0$, which indicates that c_2 in ISF of Fig. 1(b) is much smaller than Fig. 1(a). Furthermore, the up-conversion gain of the current source noise to the phase noise in Fig. 1(b) is lower than in Fig. 1(a) because of the higher common mode node frequency. At the same time, the harmonics of the current common mode node in Fig. 1(b) is less than in Fig. 1(a), which reduces the channel-length modulation and, thus, makes the output waveform in Fig. 1(b) more symmetric than in Fig. 1(a). Thus, c_0 in ISF of Fig. 1(a) is greater than that in Fig. 1(b). This analysis demonstrates that the phase noise of Fig. 1(b) is better than Fig. 1(a). Figure 4 shows the simulated phase noise difference between Fig. 1 (a) and Fig. 1(b).

The phase noise at very low frequency offsets is quite different from the maximum value of more than 10dB. The noise contribution of current source dominates in the $1/f^3$ region. Therefore, the difference on-

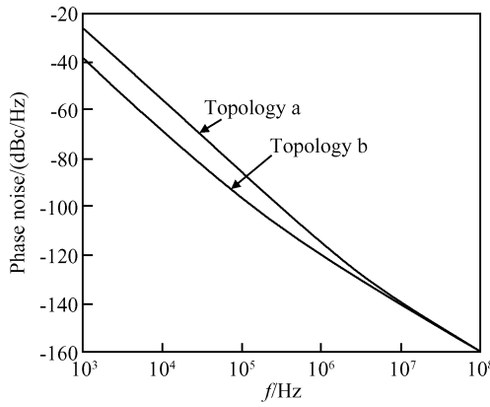

Fig. 4　Comparison of phase noise between two QVCOs

ly exists in the $1/f^3$ region. This result agrees with the analysis. When two QVCOs consume the same current, the phase noise of Fig. 1(b) is better than Fig. 1(a).

3　Circuit design of 4.224GHz QVCO

The optimization of power and noise in VCO design has been analyzed in detail in many papers[3,8~10], so this paper does not intend to repeat them. Instead, the designs of the varactors and the digital capacitor controlled array (DCCA) used in the QVCO will be emphasized.

The varactor used in this QVCO is an A-MOS varactor, the DC voltage-capacitance curve of which is shown in Fig. 5(a). The traditional connection of the varactor pair is back-to-back connected to the V_{ctr}, while the differential nodes are connected to the outputs of the VCO directly, the DC voltage of which is 1.8V. In this case, the capacitance of varactors does not vary with the maximum value of V_{ctr}, resulting in a linear degradation of K_{vco}. In order to improve the linearity of K_{vco}, a new topology is used, as shown in Fig. 5(b). Two capacitances are in series with the varactors, and a voltage of about 0.7V is set to the series-wound node. The variation is shown in the dashed

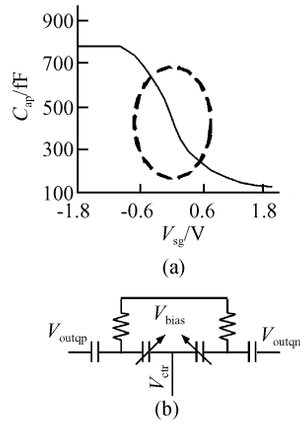

Fig. 5　Connection of varactors

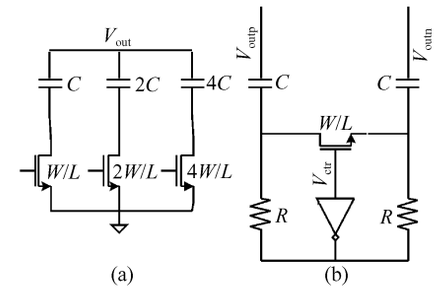

Fig. 6　Two topologies of DCCA　(a) Topology of the classical DCCA; (b) A new DCCA topology

circle in Fig. 5(a), which is more linear. The simulation results indicate that the variation of K_{vco} is 28～63MHz with the V_{ctr} varying between 0.4～1.4V, while the frequency of the QVCO can cover 4.224GHz. These results are feasible and can be accepted in the design of the PLL.

In order to compensate the frequency variation, DCCA is used. The topology of the classical DCCA is shown in Fig. 6(a). When the nMOS is cut-off, the inverted voltage of the pn junction of drain-substrate in nMOS is 0V, and the junction capacitances are still somewhat large. The parasitic capacitances would reduce the exactitude of DCCA and reduce the frequency tuning range. Therefore, a new DCCA topology, shown in Fig. 6(b), is used in this paper. When the nMOS is cut-off, the inverted voltage of the pn junction of drain-substrate in nMOS is 1.8V, and the depletion region is thicker than the traditional one, so smaller junction capacitances can be obtained. Meanwhile, when nMOS is on, the resistance of nMOS R_{on} distributed to every output node is $R_{on}/2$, which is only half of that in the traditional case. In this way, it degrades the value of Q for LC-tank less, and eases the design of low power and low phase noise.

4　Measurements and analysis

This QVCO is implemented in a JAZZ 0.18μm RF-CMOS process, and the power supply is 1.8V. The circuit simulation was done using a Cadence SpectreRF™. The chip micrograph is shown in Fig. 7.

The tested current consumption is 5.86mA. The QVCO output frequency can be tuned within 3.999～4.255GHz with 4bit DCCA control and 0.3～1.5V

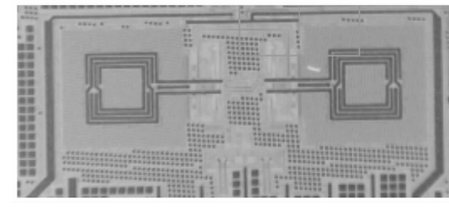

Fig. 7　Chip micrograph

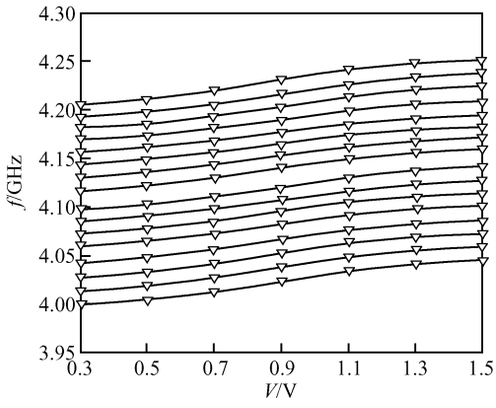

Fig. 8 Measured frequency tuning range

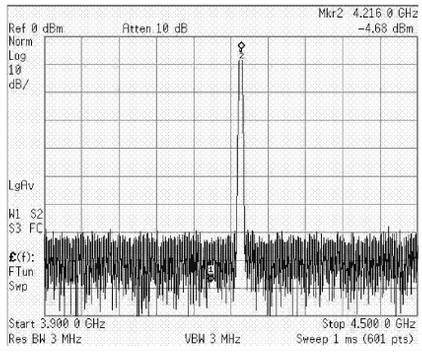

Fig. 9 Output spectrum of QVCO close to 4.224GHz

controlled voltage, as illustrated in Fig. 8. The overlay of the adjacent tuning curves is about 0.4V. The K_{vco} is about 60MHz/V when the QVCO output frequency is 4.224GHz, which agrees with simulations. The output signal spectrum at around 4.224GHz is shown in Fig. 9. Due to the fact that a buffer with 7dB attenuation is applied at the output of the QVCO, the actual output power of the QVCO is 2.32dBm, which meets the specification of a UWB synthesizer. The phase noise performance of QVCO is shown in Fig. 10 and the test results are summarized in Table 1.

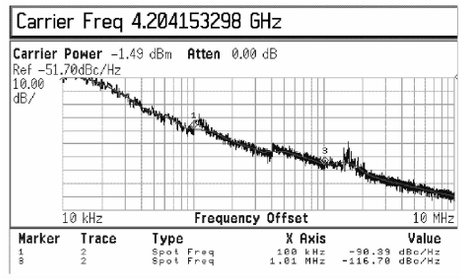

Fig. 10 Phase noise of QVCO

Table 1 Summary of measurement results

Frequency tuning range	4～4.25GHz
Output power@4.224GHz	2.32dBm
Phase noise@100kHz	-90.4dBc/Hz
Phase noise@1MHz	-116.7dBc/Hz
Power consumption	10.55mW
Phase error for I/Q	6°

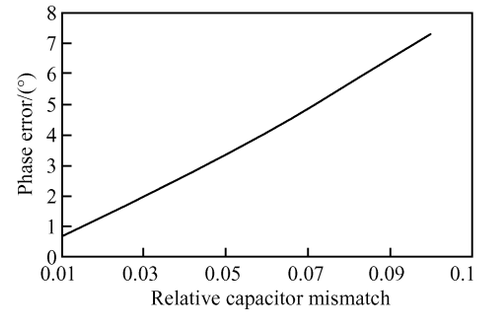

Fig. 11 Relationship of capacitor mismatch and phase error

As shown in Table 1, the phase noise performance and output power of QVCO meet the specifications of the synthesizer; however, the phase error is 6°. Due to the large area of the LC-tanks, it is difficult to match the two LC-tanks well, so the mismatch problem of the two oscillators will be serious, wherein the mismatch of the capacitances is the most serious. Furthermore, the bias current of the coupling MOSFETs is not large enough, making it difficult for the QVCO to maintain a quadrature phase. According to the simulated results shown in Fig. 11, an 8% capacitance mismatch can cause 6° of phase error.

Some recently published QVCOs are listed in Table 2. A normalized phase noise has been defined as a figure of merit (FOM) for oscillators:

$$\mathrm{FOM} = 10\lg\left(\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{L\{\Delta\omega\}P}\right) \tag{6}$$

This equation shows that this design presents excellent phase noise performance with moderate power consumption at carrier frequency as high as 4GHz. This performance is comparable with that found in recent research from a top-level IEEE publisher.

5 Conclusion

This paper presents the design of a 4.224GHz QVCO applied in an MB-OFDM UWB RF front-end synthesizer. Some practical design considerations are used in order to obtain a better phase-noise performance. Measurement results show that this QVCO can cover the frequency of 4.224GHz, and the phase-noise performance can meet the requirement of a UWB synthesizer. However, the phase match still needs improvement.

Table 2 Performance comparison of the CMOS QVCOs

CMOS QVCO	Process /μm	Frequency /GHz	Power /mW	Phase noise /(dBc/Hz)	FOM /dBc
Ref.[11]	0.13	5.5	5.28	-117@1MHz	-184.6
Ref.[12]	0.18	2.01	2.2	-124@1MHz	-186.7
Ref.[13]	0.13	10	12	-95@1MHz	-164.2
Ref.[14]	0.18	2.0	11.05	-120@1MHz	-176.0
Ref.[15]	0.35	1.8	50	-140@1MHz	-179.0
This work	0.18	4.224	10.55	-116.7@1MHz	-179.0

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一种 4.224GHz 正交压控振荡器的设计*

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摘要：设计了一种应用于 MB-OFDM UWB 射频频率综合器的工作于 4.224GHz 的正交压控振荡器(QVCO)，并采用 0.18μm RF-CMOS 工艺进行了设计实现.该 QVCO 通过改进结构能够得到更好的相位噪声.通过改变 MOS 变容管的接入方法实现了更好的压控增益线性度，并采用了新的低寄生电容、低导通电阻的数控电容阵列结构来补偿工艺变化带来的频率变化.测试结果表明，该 QVCO 在 4.224GHz 附近的 100kHz 频偏处的相位噪声为 -90.4dBc/Hz，1MHz 频偏处的相位噪声为 -116.7dBc/Hz，整个 QVCO 电路功耗为 10.55mW，电源电压为 1.8V.

关键词：UWB；正交压控振荡器；相位噪声；变容管；数控电容阵列；正交匹配性

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