A High Linearity, 13bit Pipelined CMOS ADC*

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Abstract: A 13bit, pipelined analog-to-digital converter (ADC) designed to achieve high linearity is described. The high linearity is realized by using the passive capacitor error-averaging technique to calibrate the capacitor mismatch error, a gain-boosting opamp to minimize the finite gain error and gain nonlinearity, a bootstrapping switch to reduce the switch on-resistor nonlinearity, and an anti-disturb design to reduce the noise from the digital supply. This ADC is implemented in 0.18μm CMOS technology and occupies a die area of 3.2mm^2, including pads. Measured performance includes −0.18/0.15LSB of differential nonlinearity, −0.35/0.5LSB of integral nonlinearity, 75.7dB of signal-to-noise plus distortion ratio (SNDR) and 90.5 dBc of spurious-free dynamic range (SFDR) for 2.4MHz input at 2.5MS/s. At full speed conversion (5MS/s) and for the same 2.4MHz input, the measured SNDR and SFDR are 73.7dB and 83.9 dBc, respectively. The power dissipation including output pad drivers is 21mW at 2.5MS/s and 34mW at 5MS/s, both at 2.7V supply.

Key words: analog-to-digital converter; high linearity; capacitor error-averaging; gain-boosting; bootstrapping switch; anti-disturb

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1 Introduction

With the rapid development of digital VLSI technology, wide applications of digital signal processing in wireless communications, asynchronous digital subscriber loops (ADSL), and high-speed imaging require high integral linearity, high-speed analog-to-digital converters (ADCs) fabricated in a standard CMOS technology. Pipelined ADCs present advantages over flash or successive approximation ADCs because they provide high potential resolution and a high conversion rate. In real designs, the overall linearity of pipelined ADCs is limited by circuit non-idealities such as capacitor mismatch, finite and voltage-related opamp gain, signal dependent on-resistance of switches, and crosstalk noise from digital circuits, etc. Some form of calibration, analog[1,2] or digital[3,4], is usually needed to achieve an integral linearity of more than 12bit.

In this paper, A CMOS pipelined ADC with measured integral linearity more than 13bit is presented in three main parts. Circuit design approaches, such as passive capacitor error-averaging (PCEA), a gain-boosting opamp, a bootstrapping switch, and an anti-disturb design, are used to reduce the effect of the circuit non-idealities described above to achieve high linearity. The overall architecture of the prototype is given. The circuit design approaches for high linearity are also described.

2 ADC architecture

The proposed pipelined ADC architecture designed to obtain more than 13bit level linearity is shown in Fig. 1. The ADC consists of the first 6 PCEA stages, the following 7bit backend ADCs, a clock generator, digital correction logic, an on-chip I/V references, and supporting circuit blocks. The resolution of the PCEA stages is designed to be 1.5bit, which allows a large correction range for comparator offsets. This large error correction range is used to eliminate the dedicated input sample and hold amplifier (SHA), which means a reduction in the total power consumption and thermal noise. The 7bit backend ADC is a conventional 1.5bit/stage pipelined ADC, which consists of five 1.5bit pipelined stages and the final 2bit flash ADC. Moreover, no calibration is applied to the backend ADC for the relaxed accuracy re-

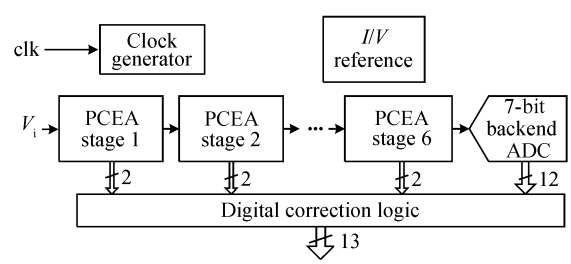

Fig. 1 Architecture diagram of the prototype ADC

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quirement of the later stages in the pipelined ADC.

In addition to the uncorrectable noise, circuit non-idealities related errors also degrade the resolution of the ADC. The dominant sources of these errors in a pipelined ADC are capacitor mismatch, finite and voltage-related opamp gain, signal dependent on-resistance of switches, and crosstalk noise from digital circuits. They increase the static nonlinearity and the dynamic disturbance, and eventually degrade the resolution of the ADC. In this paper, in order to achieve 13bit linearity, we combined the PCEA stage, the gain-boosting opamp, the bootstrapping switch, and an anti-disturb design to reduce the effects of these errors below the 13bit level.

3 Circuit design

As noted in section 2, design approaches such as a PCEA stage, a gain-boosting opamp, a bootstrapping switch, and an anti-disturb design have been used in the prototype to achieve 13bit linearity. In this section, a detailed description of each design approach is presented.

3.1 PCEA stage

In a pipelined ADC, capacitor mismatch results in an interstage amplifier gain error for the 1.5bit/stage architecture. Gain error in the interstage amplifier causes the output to be either larger or smaller than the conversion range of the following stage depending on whether the gain is larger or smaller, respectively, than the ideal gain. For the overall A/D conversion characteristic, this results in missing decision levels in the case of positive gain error and missing codes in the case of negative gain error. In a fully optimized pipelined ADC, random capacitor mismatch is the most important error source of nonlinearity. In the absence of a post-fabrication component trimming or calibration, the conversion accuracy is usually limited to 10～12bits.

Many design approaches, which can be analog circuit techniques[1,2] or digital calibration techniques[3,4], can be used to reduce capacitor mismatch error. In this paper, the PCEA[1] technique is used in the design of the first 6 stages in the pipelined core. For a 1.5bit PCEA stage, double transfer phases are used to generate two residue voltages with complementary errors by interchanging the roles of two sampling capacitors, and double sampling phases are used to sample the complementary residues from the last stage on each half of the sampling capacitors. By sharing the sampled charge across the sampling capacitors, the first order interstage gain error due to capacitor mismatch is removed. Therefore, the requirement of capacitor match is relaxed in the first 6 PCEA stages, and the capacitor size is scaled down to that of the KT/C limit to save power consumption and chip size. Although the power consumption and chip size can be further optimized using scaling down techniques though the PCEA stages, capacitors and opamps of equal size are used in the first 6 PCEA stages for layout simplicity.

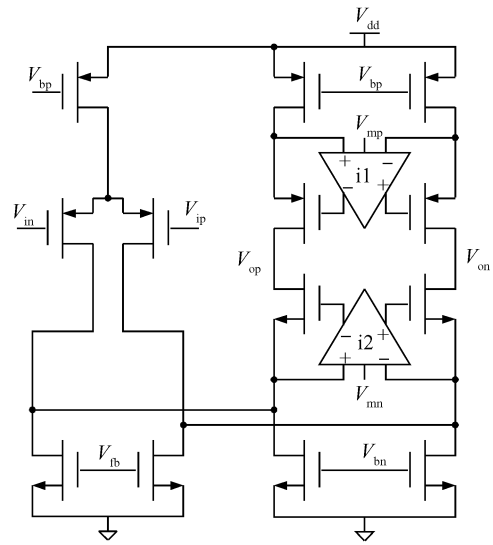

Fig. 2 Schematic diagram of the adopted opamp

3.2 Gain-boosting opamp

The opamp is a key building block in analog circuit design. In a pipelined ADC, the opamp's finite gain and voltage-related gain result in interstage amplifier gain error and nonlinearity, which eventually degrade the overall linearity of the pipelined ADC. This is true not only for conventional pipelined ADCs, but also for pipelined ADC with PCEA stages.

An opamp with large DC gain and high swing can reduce the effect of its finite gain and nonlinearity. The schematic shown in Fig. 2 meets this requirement, which is a high gain folded cascode opamp with gain-boosting applied to its cascode transistors to enhance gain further. Besides high DC gain, the design has the advantages of wider input common-mode range and output swing range. The design achieves a DC gain of more than 100dB and an output swing range larger than 2Vp-p for a 2.7V supply. This specification can be maintained over a large range of the bias current by fixing the bias voltage V_{mp} and V_{mn} to 2.4 and 0.3V, which is useful for the tradeoff between power consumption and conversion speed while retaining high accuracy.

3.3 Bootstrapping switch

For the input sampling network of a pipelined

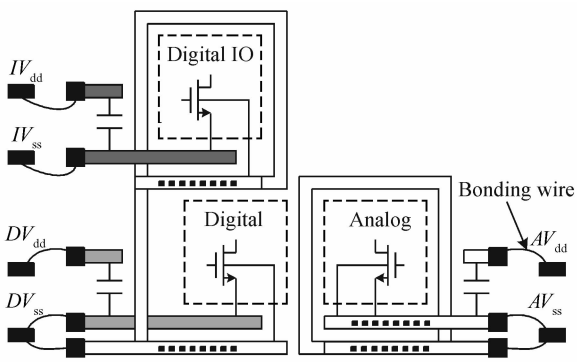

Fig. 3　Power layout of the prototype ADC

stage，the signal-dependent charge injection and on-resistance variations of switches result in static nonlinearity at low input frequencies and even more distortion at high input frequencies. It is not enough to keep the nonlinearity below the 13bit level with the conventional CMOS switches and bottom-plate sampling.

In this paper，the first 2 stages are the most critical parts in the pipelined core and their input switches are bootstrapped to achieve more than 13bit linearity. For the following stages in the pipelined core，only CMOS switches are used to save power and area.

3.4　Anti-disturb design

For the design of the pipelined ADC，which is a typical mixed-signal system，the disturbance from the digital signal to the sensitive analog signal always is a concern. Thus，the power supply layout must be done carefully to ensure good dynamic performance of the ADC.

As shown in Fig. 3，three design approaches are used to alleviate the problem of the disturbance from digital supply. One design approach is to use isolated power supplies for the analog part，the digital part，and the I/O driving buffers. Another way of minimizing disturbance is to keep the common substrate as clean as possible，which is realized by connecting the bulk of analog nMOS transistors to the analog ground and connecting the bulk of digital nMOS transistors to a clean ground instead of the noisy digital ground. Finally，large on-chip MOS capacitors are used to decouple high frequency noise between the three pairs of power and ground. These decoupling capacitors occupy the otherwise vacant area on the die.

4　Measured results

The prototype ADC was implemented in 0.18μm n-well single-poly six-metal CMOS mixed-signal technology. The prototype，shown in Fig. 4，occupies a die area of 1.6mm × 2mm，including its pads.

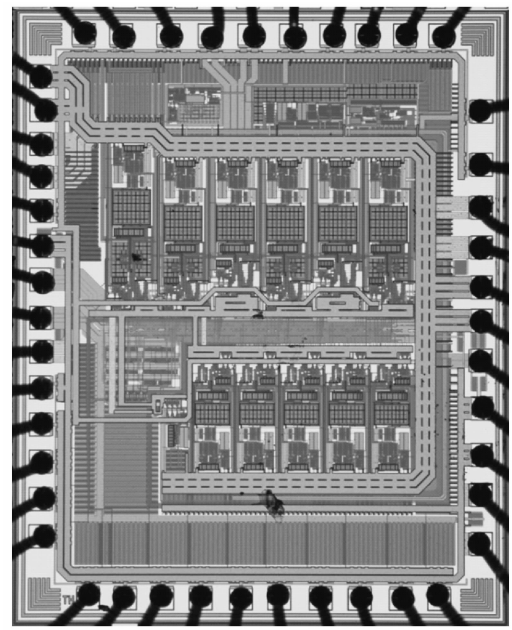

Fig. 4　Die photograph of the prototype ADC

The differential nonlinearity（DNL）and the integral nonlinearity（INL）were measured using a code-density test with a 2.4MHz full-scale sinusoidal input. At 2.5MS/s，four million samples were collected. The measured linearity profiles are shown in Fig. 5. The measured DNL and INL are −0.18/0.15 LSB and −0.35/0.5LSB for the output codes from 22 to 8170，respectively.

The dynamic linearity of the ADC was characterized by analyzing a fast Fourier transform（FFT）of the 16k output codes with a single-tone input. First，the measurement was done at a sampling rate of 2.5MS/s，and Figure 6 shows the measured FFT spectrum with a −0.153dBFS 2.4MHz input. The corresponding peak SNDR is 75.7dB，equivalent to 12.28

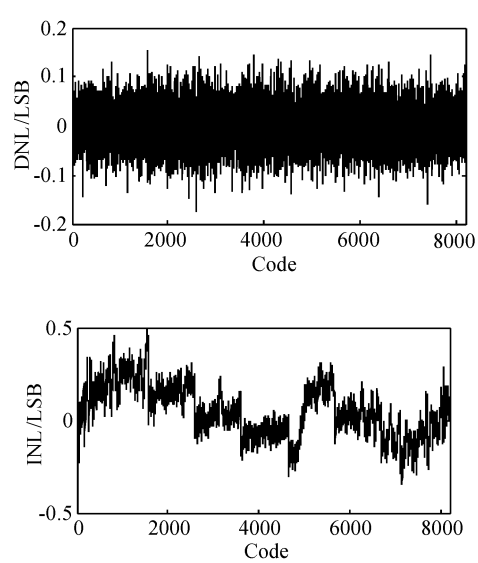

Fig. 5　Measured linearity（f_s = 2.5MS/s，f_{in} = 2.4MHz）

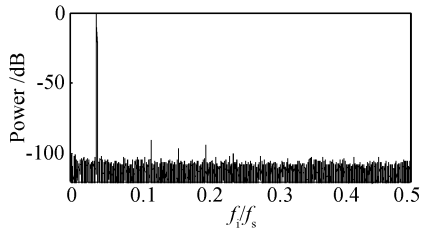

Fig. 6 Measured FFT spectrum (f_s = 2.5MS/s, f_{in} = 2.4MHz)

effective number of bits (ENOB). In this case, the total harmonic distortion (THD) and the spurious-free dynamic range (SFDR) are −87.5dB and 90.5dBc, respectively (the THD figure corresponds to the power sum of the first 9 harmonics). Second, the measurement was done at a higher sampling rate of 5MS/s, and Fig. 7 shows the measured FFT spectrum with a −1.09dBFS 2.4MHz input. The corresponding SNDR, THD, and SFDR are 73.7dB, −82.4, and 83.9dBc, respectively. With the larger input signal level, the third harmonic becomes even higher due to incomplete settling, which degrades the measured dynamic performance. This means that the bandwidth of opamps is not adequate to support the sampling rate of 5MS/s at full-scale input. The peak SNDR and SFDR can be improved further by increasing the bias current of the opamps (unfortunately, the largest bias current is fixed inside the chip in this design).

All measurements were performed with a 2.7V supply at room temperature (27℃). Table 1 summarizes the measurement results of the prototype ADC. As a reference, Table 2 shows a comparison of this work and several previously reported high-resolution ADCs with 13bit or 14bit resolution. With emphasis on conversion accuracy and the figure of merit (FOM) defined as Power/($2^{ENOB} f_s$), the comparison shows that the prototype ADC achieves a comparable conversion accuracy and FOM to the ADC reported in Ref. [1], which has the outstanding linearity and the lowest FOM in the reported 12bit or higher resolution ADCs dating from 1988 to 2004. Considering that no scaling down through the capacitor error-averaging stages and no opamp-sharing between the adjacent stages

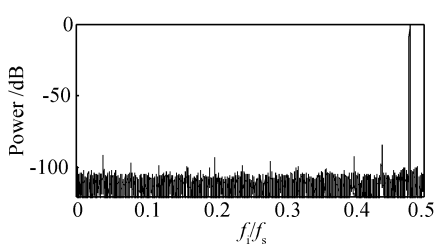

Fig. 7 Measured FFT spectrum (f_s = 5MS/s, f_{in} = 2.4MHz)

Table 1 Measured performances at 2.4MHz input

Technology	0.18μm CMOS	
Resolution/bit	13	
Reference voltage/V	1 and 2	
Sampling rate/(MS/s)	2.5	5
DNL/LSB	−0.18/0.15	
INL/LSB	−0.35/0.50	
Peak SNDR/dB	75.7	73.7
Peak SFDR/dBc	90.5	83.9
Power/mW	21	34

Table 2 Comparison with some previous works

	Resolution /bit	Conversion rate /MHz	SNDR /dB	Power /mW	FOM
Ref. [1]	14	12	75.5	98	1.7
Ref. [5]	13	10	68	360	17.5
Ref. [6]	13	40	67	268	3.7
This work	13	2.5	75.7	21	1.7
	13	5	73.7	34	1.7

have been used for layout simplicity, a better FOM can be expected if scaling down and opamp-sharing are used to lower power.

5 Conclusion

This paper describes a high linearity, 13bit pipelined ADC in 0.18μm CMOS technology, and its performance is summarized in Table 1. The key feature of this converter is that a capacitor error-averaging stage, a gain-boosting opamp, a bootstrapping clock, and an anti-disturb design are combined to improve the overall linearity. The measured results show that the ADC has achieved an integral linearity of more than 13bit and an outstanding FOM compared with the previously reported designs.

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一个高线性 13 位流水线 CMOS A/D 转换器*

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摘要：介绍了一个采用多种电路设计技术来实现高线性 13 位流水线 A/D 转换器.这些设计技术包括采用无源电容误差平均来校准电容失配误差、增益增强(gain-boosting)运放来降低有限增益误差和增益非线性、自举(bootstrapping)开关来减小开关导通电阻的非线性以及抗干扰设计来减弱来自数字供电的噪声.电路采用 0.18μm CMOS 工艺实现，包括焊盘在内的面积为 3.2mm^2.在 2.5MHz 采样时钟和 2.4MHz 输入信号下测试，得到的微分非线性为 -0.18/0.15LSB，积分非线性为 -0.35/0.5LSB，信号与噪声加失真比(SNDR)为 75.7dB，无杂散动态范围(SFDR)为 90.5dBc；在 5MHz 采样时钟和 2.4MHz 输入信号下测试，得到的 SNDR 和 SFDR 分别为 73.7dB 和 83.9dBc.所有测试均在 2.7V 电源下进行，对应于采样率为 2.5MS/s 和 5MS/s 的功耗(包括焊盘驱动电路)分别为 21mW 和 34mW.

关键词：模数转换器；高线性；电容误差平均；增益增强；自举开关；抗干扰

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