Deep Level Transient Fourier Spectroscopy and Photoluminescence of Vanadium Acceptor Level in n-Type 4H-SiC*

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Abstract: Deep level transient Fourier spectroscopy (DLTFS) measurements are used to characterize the deep impurity levels in n-type 4H-SiC by vanadium ions implantation. Two acceptor levels of vanadium at $E_C - 0.81$ and $E_C - 1.02$eV with the electron capture cross section of 7.0×10^{-16} and 6.0×10^{-16} cm^2 are observed, respectively. Low-temperature photoluminescence measurements in the range of 1.4~3.4eV are also performed on the sample, which reveals the formation of two electron traps at 0.80 and 1.16eV below the conduction band. These traps indicate that vanadium doping leads to the formation of two deep acceptor levels in 4H-SiC, with the location of 0.8 ± 0.01 and 1.1 ± 0.08eV below the conduction band.

Key words: 4H-SiC; vanadium doping; acceptor level
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1 Introduction

Semi-insulating silicon carbide (SiC) substrates are important for next-generation high temperature, high power, and high density microwave integrated circuits, which are based on large band gap semiconductors such as gallium nitride and SiC[1]. Semi-insulating SiC can be obtained by doping vanadium[2,3]. As an electrically amphoteric impurity, vanadium substitutes for silicon site (V_{Si}) and produces two levels within the SiC bandgap, i.e., the deep donor V^{4+}/V^{5+} and the acceptor V^{3+}/V^{4+} in p- and n-type SiC[4,5]. Therefore, semi-insulating properties in SiC can be achieved by compensating all the principal residual shallow donor or acceptor impurities with the vanadium deep levels.

It is generally recognized that the vanadium donor level is located at 1.6eV below the conduction band in 4H-SiC[6,7]. However, there are still issues determining the location of the vanadium acceptor level in 4H-SiC. It is possible to determine the deep levels of impurities in SiC by using deep level transient spectroscopy (DLTS) measurements. Several DLTS studies indicate that the vanadium acceptor level is located at 0.8eV below the conduction band[8,9]. However, the temperature of these DLTS measurements is around 450K, which is not high enough to detect deeper levels of vanadium in SiC. Furthermore, temperature-dependent Hall or resistivity measurements of V-doped 4H-SiC often yield a level in the vicinity of 1.1eV[10,11]. Zvanut *et al*[12] detected the level by performing photo-induced electron paramagnetic resonance (EPR) measurements, and assumed that the vanadium acceptor level may be located at 1.1eV below the conduction band.

In this paper, a sample with a semi-insulating layer in n-type 4H-SiC is prepared by vanadium ion implantation. The vanadium acceptor level in 4H-SiC is comprehensively studied using DLTS and low-temperature photoluminescence (PL). In particular, the DLTS is not based on rate window or lock-in techniques but, rather, on Fourier analysis. This technique is also called deep level transient Fourier spectroscopy (DLTFS).

2 Experiment

The experiments were performed on a 4.9μm-thick n-type ($N_d = 5.2 \times 10^{15}$ cm^{-3}) 4H-SiC epitaxial layer grown on Si face, (0001) oriented (8° off), n-doped substrate from Cree Research, Inc. V ions were implanted with a 1.4×10^{13} cm^{-2} dose at 2100keV. Post-implantation annealing was performed in argon

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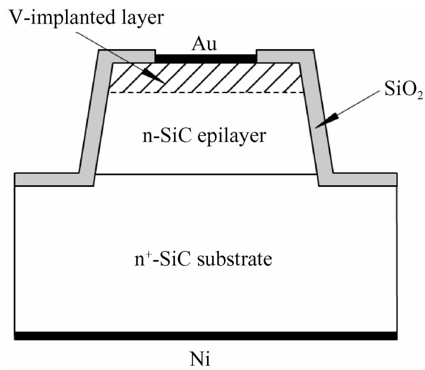

Fig. 1 DLTFS measurement structure for the vanadium implanted n-type 4H-SiC

atmosphere at 1650℃ for 30min. This process is necessary to electrically activate more vanadium ions for compensation[11]. To minimize Si evaporation from the sample surface, the samples were encased in a SiC-coated graphite crucible during annealing.

Samples were processed into a mesa structure with a 160μm diameter by reactive ion etching with CF_4 and O_2 gases, and surfaces were passivated with thermal oxides to reduce leakage current during DLTFS measurements. Ni was deposited on the backside of the samples and then annealed at 1050℃ for 10 min in forming gas (90% N_2, 10% H_2) in order to form an ohmic contact. Schottky diodes were fabricated by evaporating Au dots on the top-side through a shadow mask in a high vacuum chamber ($\leqslant 10^6$ Torr base pressure). The schematic cross section of the sample is shown in Fig. 1.

C-V measurements were carried out on Schottky diodes with a Bio-Rad DL 8000 system. The signal frequency for capacitance measurements is 1MHz, and the magnitude of the applied differential voltage is 30mV. The DLTFS measurements in the temperature range from 80 to 550K were carried out using a deep level transient Fourier spectroscopy Bio-Rad DL 8000 system, which can be used for tests of high sensitivity samples $[10^{-7}(N_D - N_A) < N_T < 10^{-5}(N_D - N_A)]$. During the DLTFS measurements, the reverse bias was set at different voltages and periodically pulsed to 0 V for trap filling. DLTFS, a digital DLTS based on Fourier analysis of the transient collected as a function of temperature, was first described by Weiss and Kassing[13]. It has significant advantages over both rate window and lock-in amplifier type systems in terms of high sensitivity and good energy resolution.

Low temperature PL spectra were measured under excitation with a KIMMON HeCd laser operating at a wavelength of 325nm. The sample was cooled to 10K using a closed-cycle helium cryosystem during the measurements.

3 Results and discussion

3.1 DLFTS measurements

The DLTFS measurements were conducted using a digital DLTS system with a 1MHz Boonton bridge. A transient recorder was used to measure values from a capacitance transient. From these values discrete Fourier coefficients were formed, providing a basis for the immediate calculation of the time constant and the amplitude for each transient. The time constant τ can thus be derived as[13]:

$$\tau = T_W b_n / 2\pi n a_n \tag{1}$$

where a_n, b_n are the cosine and sine coefficients of the nth order, n is the order of the coefficients, and T_W is the period width.

If transient data $C(t)$ have been collected, a Fourier transform of $f(t)$ can be done by using[13]

$$C(t) = f(t) = a_0/2 + \sum_{n=1}^{N-1} a_n(2\pi nt/T_W) + \sum_{n=1}^{N-1} b_n(2\pi nt/T_W) \tag{2}$$

where $n = 0, 1, 2, \cdots\cdots N$, N is the number of measured data points for the transient, t is the time, and $a_0/2$ is the offset.

The b_1 coefficient denotes the first sine coefficient in the Fourier transformation of the digitized transient using different orders of both sine and cosine waves. According to Eq. (1), it is comparable to the conventional DLTS signal with a time constant of about 64ms.

A representative DLTFS spectra obtained on unimplanted and V-implanted n-type 4H-SiC Schottky diode are presented in Figs. 2 (a) and 2 (b), respectively. No peaks are observed in the n-type 4H-SiC sample under various reverse bias conditions (V_r = −1, −2, and −4V), as shown in Fig. 2(a). However, Figure 2 (b) shows that two electron emission peaks, subsequently named E1 and E2, are clearly observed in the V-implanted 4H-SiC sample under various reverse bias conditions (V_r = −1, −2, and −4V). These peaks are attributed to two deep electron traps produced by the vanadium acceptor level. The measured temperatures for E1 and E2 are about 415 and 520K, respectively. The activation energies of the traps evaluated from Arrhenius plots are 0.81 and 1.02eV below the conduction band, respectively. The results confirm that the implanted vanadium atoms act as deep levels to trap electrons, and the two vanadium acceptor levels are located at 0.81 and 1.02eV below the conduction band, respectively.

From the dependence of $1/C^2$ on V for the V-

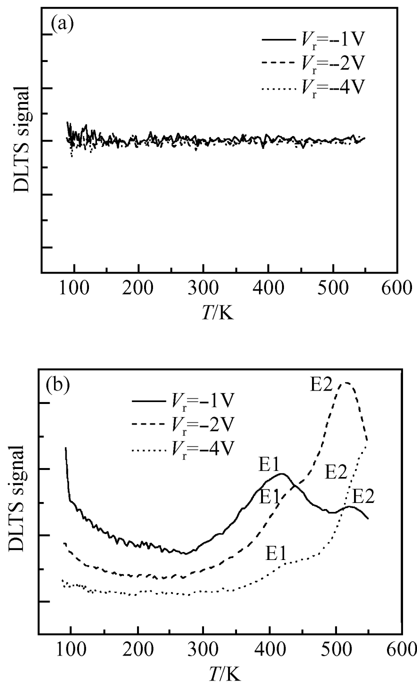

Fig.2 DLTFS spectra of n-type 4H-SiC (a) and V-implanted n-type 4H-SiC (b) with 100 ms/pulse width and various biases V_r

implanted sample, an average net donor concentration ($N_D - N_A$) value of 4.09×10^{15} cm^{-3} is obtained. According to our previous studies of the redistribution of vanadium implanted in n-type 4H-SiC after 1650℃ annealing[11,14], the concentration of vanadium in the surface region of SiC is about 2×10^{15} cm^{-3}. Considering the incomplete ionization effect, the activated vanadium ions concentration is below 10^{15} cm^{-3}. As a result, the carrier concentration remains unchanged due to lack of compensation of vanadium in the surface region. The DLTFS measurements indicate that the concentration of vanadium (N_T) in the surface region is about 2×10^{14} cm^{-3}. The values of $N_D - N_A$ for V-implanted 4H-SiC samples and DLTFS parameters for $E1$ and $E2$ traps in the samples are listed in Table 1. Although the concentration ratio of traps $E1$ and $E2$ to the net donors ($N_T/(N_D - N_A)$) is relatively low (about 2%), the activated vanadium ions have produced two acceptor levels to trap the free electrons in n-type 4H-SiC.

Table 1 Net donor concentration, $N_D - N_A$, and DLTFS parameters for E1 and E2 traps in V-implanted 4H-SiC samples

V_R /V	$N_D - N_A$ /10^{15} cm^{-3}	$E_C - E_T$ /eV	Temperature /K	N_T /10^{14} cm^{-3}	σ_n /10^{-16} cm^2	($N_T/(N_D - N_A)$)/%
-1	4.09	$E1=0.81$	415	2.33	7.0	2.88
		$E2=1.02$	520	1.67	6.0	2.06
-2	4.09	$E1=0.81$	415	2.30	7.0	2.84
		$E2=1.0$	510	4.25	6.0	5.25
-4	4.09	$E1=0.80$	410	0.89	7.0	1.10
		$E2=1.02$	520	3.25	6.0	4.02

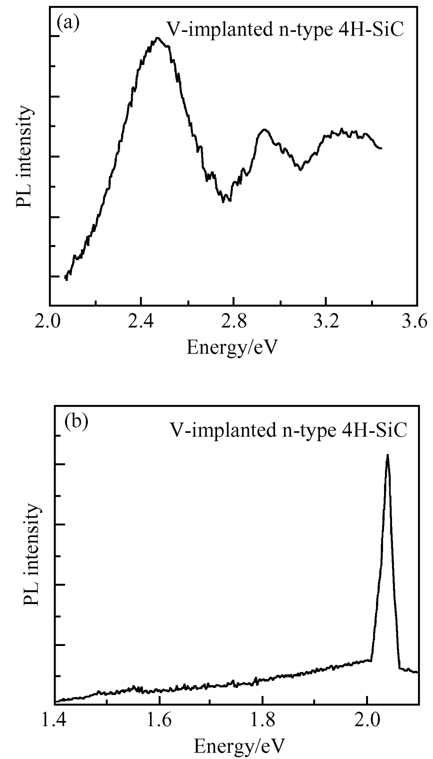

Fig.3 PL spectra of 2.07～3.44eV (a) and 1.60～2.07eV (b) for V-implanted n-type 4H-SiC sample under 325nm excitation at 10K

3.2 PL results

To verify the locations of vanadium induced deep levels in SiC, typical PL spectra of V-implanted n-type 4H-SiC samples are measured at 10K, as shown in Fig.3. Figure 3 (a) shows a dominated peak together with two broad peaks between 2.1 and 3.4eV. The broad peak at 3.2eV is dominated by recombination processes of the band edge emission. The broad structured emission band near 3.0eV is also found in the sample, which is attributed to a recombination process involving photoneutralized n-donors and photoneutralized acceptors[15]. In particular, a dominated peak at 2.4eV is observed, which is related to the vanadium acceptor level in 4H-SiC. This means that a vanadium acceptor level is located at 0.8eV below the conduction band, a result consonant with the DLTFS measurements discussed above.

To investigate deeper levels of vanadium in SiC, PL spectra between 1.4 and 2.1eV were also measured, as shown in Fig.3(b). An obvious peak is observed at 2.04eV, which means that another vanadium acceptor level is located at 1.16eV below the conduction band. Considering the 1.02eV determined by DLTFS measurements, the 1.16eV level is in agreement with the level in the vicinity of 1.1eV reported by many studies[11,12].

4 Conclusion

The DLTFS technique is used to characterize the deep electron traps in vanadium implanted n-type 4H-SiC samples. The common determined vanadium acceptor level located at $E_C - 0.81eV$ is observed at 415K, which has an electron capture cross section of 7.0×10^{-16} cm^2. When the temperature is increased to 520K, a deeper level located at $E_C - 1.02eV$ is detected with an electron capture cross section of 6.0×10^{-16} cm^2. PL studies also reveal that the implanted vanadium atoms form two radiative deep traps located at $E_C - 0.8$ and $E_C - 1.16eV$. The results give further evidence that doping with vanadium can produce two acceptor levels, $E_C - 0.8\pm0.01$ and $E_C - 1.1\pm0.08eV$ in n-type 4H-SiC.

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钒受主能级在 n 型 4H-SiC 中的深能级瞬态傅里叶谱和光致发光*

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摘要：借助深能级瞬态傅里叶谱研究了钒离子注入在 SiC 中引入的深能级陷阱.掺入的钒在 4H-SiC 中形成两个深受主能级,分别位于导带下 0.81 和 1.02eV 处,其电子俘获截面分别为 7.0×10^{-16} 和 6.0×10^{-16} cm^2.对钒离子注入 4H-SiC 样品进行低温光致发光测量,同样发现两个电子陷阱,分别位于导带下 0.80 和 1.16eV 处。结果表明,在 n 型 4H-SiC 掺入杂质钒可以同时形成两个深的钒受主能级,分别位于导带下 0.8 ± 0.01 和 1.1 ± 0.08eV 处.

关键词：4H-SiC；钒掺杂；受主能级

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