A 0.5mV High Sensitivity 200Mbps CMOS Limiting Amplifier with RSSI for Optical Receivers

Wang Rong[1,†], Wang Zhigong[1], Xu Jian[2], and Guan Zhiqiang[2]

(1 *Institute of RF- & OE-ICs, Southeast University, Nanjing* 210096, *China*)
(2 *Sino-Chip OEIC Jiangsu Co. Ltd, Nanjing* 210016, *China*)

Abstract: A 0.5mV high sensitivity, 200Mbps CMOS limiting amplifier (LA) with 72dB ultra wide dynamic range is described. A novel active DC offset cancellation loop is elaborately analyzed and designed to achieve this performance. Using a signal path, a received signal strength indicator (RSSI), based on the piecewise-linear approximation, is realized with a ±2dB logarithmic accuracy in a 60dB indicating range. The architecture of the LA and RSSI employed is determined by the optimal sensitivity and RSSI accuracy for a specified speed, gain, and power consumption. It consumes 60mW from a single 5V supply. The active area is 1.05mm^2 using standard 5V 0.6μm CMOS technology.

Key words: LA; RSSI; optical receivers; piecewise-linear approximation
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1 Introduction

Due to the blossoming of optical access networks, optical receivers working at up to 200Mbp are gaining commercial importance and are demanded in many different system applications, such as 125Mbps fiber distributed data interface (FDDI) receivers, 155Mbps synchronous optical network (SONET) transceivers, and 200Mbps enterprise system connections (ESCON). But, the widespread commercial use of optical receivers depends largely on the availability of low-cost components. From this perspective, mature, standard CMOS technology is extremely attractive since it offers the high yield and high level of integration that is needed to reduce the manufacturing cost[1].

A limiting amplifier (LA) with high sensitivity is required because commercial transimpedance amplifiers (TIA) achieve sensitivity as high as −40dBm in this frequency range. Including the link loss of TIA and LA, the LA will receive a very weak signal, perhaps only several mV_{pp}.

An RSSI, which detects system faults that will result in excessive bit errors, is normally required to monitor the output signal amplitude from the TIA[2]. The RSSI is generally realized in logarithmic form because the wide dynamic variation of the received signal can be represented within a limited indication range[3]. Successive-detection architecture is adopted for realizing the logarithmic amplifier, which uses the LA the in data path.

We realize a high sensitivity LA and an RSSI based on a low-cost CSMC 0.6μm 2P2M CMOS process in this paper. We also describe general considerations, including sensitivity and RSSI considerations.

2 General considerations

2.1 Sensitivity considerations

Usually the sensitivity of optical receivers is dominated by TIA, but the LA must also achieve relatively high sensitivity so as not to limit the overall receiver sensitivity, especially for high performance TIAs. The LA sensitivity is dominated by two main factors, i.e., the noise and the offset voltage. Generally, more attention is paid to noise, but LA noise should be small compared to the TIA noise. Moreover, the high gain of TIA makes the noise contribution of the LA insignificant because the input-referred noise voltage is scaled by the transimpedance gain when referred to the receiver input. A fully-differential LA architecture can minimize noise coupling and supply noise. But, electrical properties of identically designed devices have a certain amount of variation due to the non-uniformities in fabrication process and operating environment, such as operating temperature. As device size decreases, the matching properties of a pair of devices degrades[4]. Therefore, this una-

† Corresponding author. Email: wangrong@seu.edu.cn
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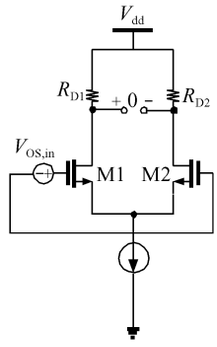

Fig. 1　Resistor loaded differential pair

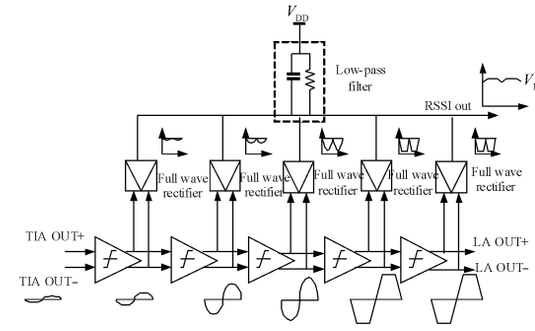

Fig. 2　Block diagram of RSSI

voidable offset voltage will result in the slicing level being in a non-optimal position and, thereby, degrading the sensitivity. It also reduces the RSSI accuracy, degrades noise rejection, and leads to pulse width distortion (PWD). Thus, offset voltage must be reduced as much as possible. The input-referred offset voltage $V_{OS.in}$ is defined as the input voltage that forces the output voltage to become zero. The offset in a resistor loaded differential pair, as shown in Fig. 1, can be written as

$$V_{OS.in} = \frac{V_{GS} - V_{TH}}{2}\left[\frac{\Delta R_D}{R_D} + \frac{\Delta(W/L)}{(W/L)}\right] - \Delta V_{TH} \tag{1}$$

$\Delta(W/L)$ and ΔV_{TH} are the mismatches between the two transistors' W/L ratio and the threshold voltage, respectively. ΔR_D is the mismatch between the two loaded resistors. For simplicity, $\lambda = \gamma = 0$, and mismatches in $\mu_n C_{OX}$ are neglected.

Equation (1) shows that $\Delta(W/L)$, ΔV_{TH}, and ΔR_D must be minimized. All the mismatches decrease as the area of the transistor, WL, increases.

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \tag{2}$$

$$\Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}} \tag{3}$$

where A_{VTH} and A_K are the proportionality factors[5]. CSMC resistor characterization reports also show that larger devices exhibit smaller mismatches. Equation (1) reveals that the threshold voltage mismatch is directly referred to the input, while the contribution of the device dimension mismatch increases with the equilibrium overdrive. Thus, it is desirable to minimize $V_{GS} - V_{TH}$ by lowering the tail current or increasing the dimensions of the transistor and resistor.

Therefore, the offset voltage can be minimized from two aspects: design and layout. The dimension of devices, whose matches are important, must be as large as possible, especially their areas. However, large dimensions limit the speed. At the same time, lowering the tail current by reducing $V_{GS} - V_{TH}$ is restricted by the gain, which is proportional to I_D. Therefore, offset voltage involves a trade-off of speed, gain, and power dissipation, making the choices of devices a multi-dimensional optimization. All available matching means should be implemented in layout, such as placing matched devices close to each other, surrounding them with dummies, cross-quading them, and matching the parasites on wiring[6]. Overall, a typical CMOS amplifier has an offset voltage of several mV, which is too large for a LA with high gain. Therefore, an offset compensation scheme must be employed.

In addition, the bandwidth decided by lower and higher cutoff frequencies must be sufficiently high to avoid intersymbol interferences (ISI), which also degrade sensitivity.

2.2　RSSI consideration

A logarithmic amplifier is widely used in RSSIs, since a wide dynamic variation of signal power can be represented within a limited voltage range. Unlike BJT, MOSFET no longer derives a logarithmic characteristic from the pn junction I-V characteristic. Thus successive detection, as shown in Fig. 2, based on piecewise-linear approximation is used instead[3,7,8]. Its core is a cascaded chain of amplifiers. As the signal progresses down the gain chain, it will, at some stage, begin to clip. The signal at the output of each amplifier is fed into a full wave rectifier (FWR). When the signal limits the fourth stage of the amplifier chain as shown, the FWR after this stage source has almost no current and the FWRs before this stage source have variable current according the I-V curve of the FWR. The outputs of these rectifiers are summed and applied to a low-pass filter, removing the ripple of the full-wave rectified signal. This pseudo-log, DC-like voltage indicates the input AC signal strength. The total sourcing current and the resistor determine the output RSSI voltage. This pseudo-log RSSI is appropriate because it uses the LA in the data path of the optical receiver, which saves chip area and power dissipation.

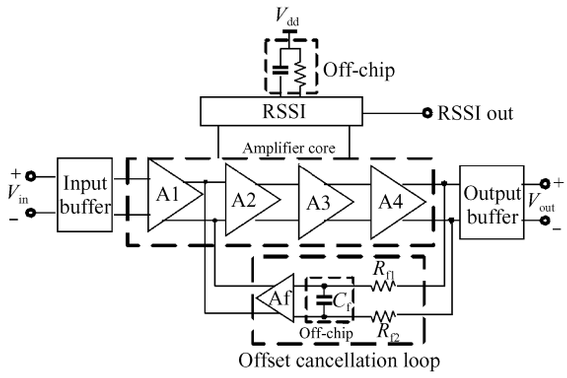

Fig. 3 Limiting amplifier architecture

3 Architecture and circuits design

3.1 System architecture

Figure 3 shows the designed architecture of the limiting amplifier, which consists of an input buffer, four identical gain stages comprising the LA core, an offset cancellation loop, an output buffer, and a RSSI circuit.

3.2 Building blocks

(1) Input buffer and current-mode logic (CML) output buffer: Normally the length between TIA and LA is much less than the signal wavelengths when operating below 200Mbps. Therefore, the transmission line effect is not important. Moreover, the input signals from the TIA need to be AC-coupled using external capacitors. Thus, an input buffer is required for internal DC-bias, not for the matching network. Illustrated in Fig. 4, R_3 and R_4 consist of voltage dividers. The same resistors, R_1 and R_2, connect biased point B to two input ends to supply DC bias for the internal circuits. Considering V_{in} as a differential input signal, the point B can be regarded as a virtual ground so R_1 and R_2 are AC input resistors. $R_{1,2}$ and $C_{in1,2}$, coupled capacitors, construct one lower cutoff frequency. Due to the lack of a matching requirement, $R_{1,2}$ values are set high to avoid large capacitor values.

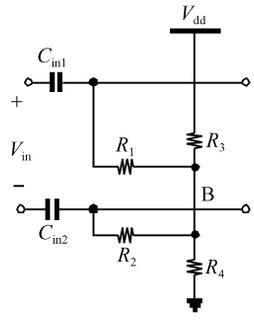

Fig. 4 Input buffer

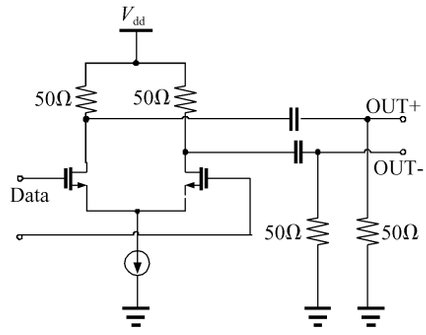

Fig. 5 CML output buffer

The CML output consists of a differential pair with 50Ω collector resistors, as shown in Fig. 5. The signal swing is supplied by switching the current in a differential pair. In order to keep the signal swing within the CML requirement, 640～1000mV$_{pp}$, a negative temperature coefficient resistor is employed to compensate the proportional to absolute temperature (PTAT) current.

(2) Amplifier core: The design for the amplifier core is particularly important, not only for the data path, bus also for RSSI circuits. Thus, its choice must be a trade-off between sensitivity, bandwidth, gain, and RSSI accuracy. For less than 1mV sensitivity, the amplifier core must provide a gain higher than 60dB while exhibiting sufficiently wide bandwidth, approaching 200MHz, to introduce negligible ISI. This results in an astounding gain-bandwidth product (GBW) of 200GHz, normally $\gg f_T$. As a result, a cascade multiple stages design, as shown in Fig. 3, which can boost the GBW beyond that of a single stage, must be adopted. For a total gain of A_{tot}, such as 60dB, the required cell gain-bandwidth product GBW$_C$ can be written as

$$\mathrm{GBW_C} = \frac{\mathrm{GBW_{tot}}}{A_{tot}^{1-1/n} \times \sqrt[m]{2^{1/n}-1}} \tag{4}$$

where $\mathrm{GBW_{tot}} = A_{tot} \times \mathrm{BW_{tot}}$, $\mathrm{GBW_C} = A_{tot}^{1/n} \times \mathrm{BW_C}$ and m equals 2 for first-order stages and 4 for second-order stages[9,10]. Due to the large dynamic range of TIA output, the RSSI must indicate a voltage range from 1mV$_{pp}$～1V$_{pp}$. The upper limit is restricted by the first stage amplifier, which cannot clip when the signal input is 1V$_{pp}$. This can be written as

$$\sqrt{2}(V_{GSQ} - V_{TH}) = \sqrt{\frac{2I_{SS}}{\mu_n C_{OX}\dfrac{W}{L}}} > 1 \tag{5}$$

The accuracy of the RSSI primarily determines the gain of each stage. The maximum error compared with an ideal logarithmic curve can be derived as[3]

$$\mathrm{Error_{max}(dB)} = \frac{10\left[(-1+\sqrt{A_s}+A_s)\lg A_s-(A_s-1)\lg\left(A^{(3A_s-1)/(2A_s-2)}\right)\right]}{A_s-1} \tag{6}$$

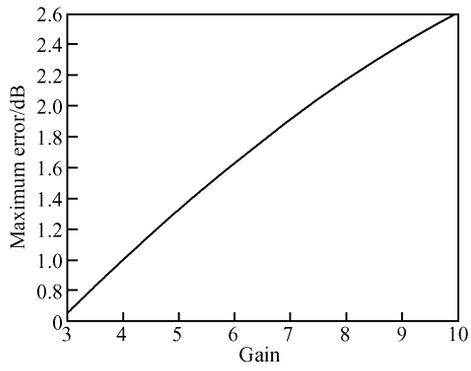

Fig. 6　RSSI maximum error versus each stage gain

where A_s is the gain of each stage. Each stage gain versus maximum error is illustrated in Fig. 6.

Equations (4) and (6) show the assumed 60dB total gain, the number of stages n bigger, the least requirement of GBW_C, the least cell gain, and the most accurate precision. But the gain per stage is small, making the noise contributed by all of the stages significant. For these reasons, typical high-gain LA employ no more than five gain stages[11].

According to the analyses above, four directly coupled gain stages are employed in this work. Each gain cell is a basic resistor loaded with a differential amplifier, followed by a source follower, as shown in Fig. 7, supplying the gain of 6.8 (16.7dB). As illustrated in Fig. 6, the relative error in RSSI is smaller than 2dB, which is satisfactory in optical communication applications. In order to acquire a gain insensitive to process and thermal variations, several papers introduced MOS as loads[3,8]. However, MOS loaded cells sacrifice linearity and consequently degrade PWD and sensitivity. In this work, a PTAT current source is used to compensate the drop of g_m with the increase of temperature. Simulation indicates that the change of total gain is optimized within 5dB in all process, voltage, and temperature (PVT) cases. In Fig. 7, M1～M3 and R_1, R_2 consist of a differential amplifier. While M 4 ～ M 7 consists of a source follower, which

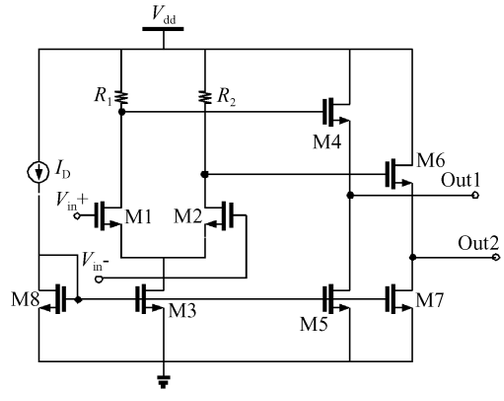

Fig. 7　Gain cell circuits

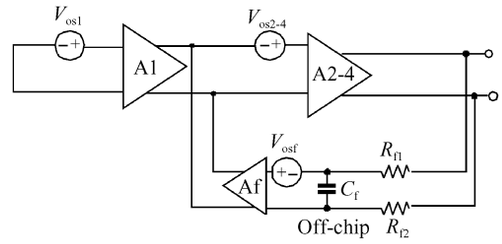

Fig. 8　Simplified offset cancellation circuit

functions as a level shift to keep the input and output common-mode levels of each cell the same.

(3) DC offset cancellation loop: As illustrated in section 2, an offset cancellation scheme must be adopted to improve the sensitivity and RSSI accuracy. Thus, as shown in Fig. 3, a low-frequency feedback loop is introduced. Figure 3 is simplified as Fig. 8 to derive $V_{os,in}$. A_{2-4} is the total gain of the last three cells. V_{os1}, V_{os2-4}, and V_{osf} are the input-referred offset voltages of the first stage, the last three stages, and the feedback stage, respectively. The total output offset voltage $V_{os,out}$ is derived as

$$V_{os,out} = \frac{A_1 V_{os1} + A_f V_{osf} + V_{os2-4}}{1 + A_{2-4} A_f} A_{2-4} \tag{7}$$

The offset voltage referred to the input is therefore given by

$$V_{os,in} = \frac{V_{os,out}}{A_1 A_{2-4}} = \frac{A_1 V_{os1} + A_f V_{osf} + V_{os2-4}}{(1 + A_{2-4} A_f) A_1} \approx \frac{V_{os1}}{A_{2-4} A_f} \times \frac{V_{osf}}{A} \times \frac{V_{os2-4}}{A A_f} \tag{8}$$

Since the feedback amplifier does not need to be fast, large transistors with good matching properties can be used to make V_{osf} very small. This circuit also exhibits another low frequency cutoff of

$$f_c \propto \frac{A_f A_{2-4}}{R_f C_f} \tag{9}$$

It will result in low-frequency pattern-dependent jitter (PDJ) when NRZ data contain long strings of identical 1's or 0's. To minimize this effect, f_c must be carefully chosen according to operating speed and consecutive '1's or '0's. Equations (8) and (9) reveal that the choice of A_f must be a trade-off between $V_{os,in}$ and f_c. In this work, in order to ensure f_c falls in the range of several kHz, several MΩ high poly resistors served as R_F and a 0.1μF off-chip capacitor as C_F.

(4) RSSI circuits: The RSSI in Fig. 2 is an architecture of piecewise linear approximation. Cascaded gain cells are already existent in the data path. Therefore, only full-wave rectifiers (FWRs) and a low-pass filter that ties all the FWR outputs are required.

Considering coherence and power dissipation, unbalanced source coupled differential pairs FWR is employed in this work, shown in Fig. 9[12]. The FWR

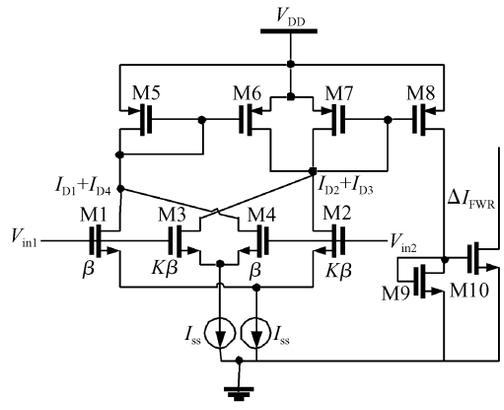

Fig. 9 Unbalanced source coupled differential pairs FWR

consists of two identical unbalanced source-coupled pairs M1～M4, with different gate W/L ratios of K, whose input electrodes are connected cross-coupled and whose output electrodes are connected in parallel. M5-M6, M7-M8, and M9-M10 form current mirrors, respectively. The current of M10 is the output current of the rectifier. When input voltage is small, most of the current flows through the larger transistors (M2-M3). Therefore, the current flow of M5 and M6 is small. M8 obtains a large current by mirroring M7, and so does M10. As input voltage increases, the smaller size transistors (M1 and M4) start to contribute to the current flow in the left side current mirror (M5 and M6), which causes the current of the right side current mirror (M7 and M8) to decrease, and M10 also decreases. Thus, the output current of the rectifier depends on the input voltage. The output current ΔI_{FWR} is expressed in Eq. (10), where K is the W/L ratio of the two input transistor pairs, as shown in Fig. 9.

$$\Delta I_{FWR} = (I_{D2} + I_{D3}) - (I_{D1} + I_{D4}) = \Delta I_1 - \Delta I_2$$

$$= \begin{cases} 2\dfrac{K-1}{K+1} I_{SS} - 4\dfrac{K(K-1)\beta}{(K+1)^2} V_{ID}^2, & |V_{ID}| \leqslant \sqrt{\dfrac{I_{SS}}{K\beta}} \\ -2(K-1)K\beta V_{ID}^2 - 4K\beta |V_{ID}| \sqrt{(K+1)\dfrac{I_{SS}}{\beta} - KV_{ID}^2} + \dfrac{2KI_{SS}}{K+1}, & \sqrt{\dfrac{I_{SS}}{K\beta}} \leqslant |V_{ID}| \leqslant \sqrt{\dfrac{I_{SS}}{\beta}} \\ 0, & |V_{ID}| \geqslant \sqrt{\dfrac{I_{SS}}{\beta}} \end{cases} \quad (10)$$

where $\beta = 1/2 u_n C_{OX} W/L$, and V_{ID} is the differential input voltage.

4 Measured results

The LA with RSSI has been fabricated in 0.6μm CMOS 2P2M technology and the packaged chip is bonded to a PCB surrounded with the required external components. Figure 10 is the die photo. The active area is 1.5mm×0.7mm. Power consumption is 60mW using a 5V single supply voltage. The LA exhibits a high sensitivity of 0.5mV for BER = 10^{-12}. Figure 11 shows the LA output eye-diagrams for a $2^{23}-1$ 200Mbps pseudorandom bit pattern at various input amplitudes.

For a $2^{23}-1$ 200Mbps pseudorandom bit pattern, the performance of RSSI is obtained with 1 to 1000mV differential input amplitudes, shown in Fig. 12. The RSSI output voltage is approximated by:

$$V_{RSSI}(\mathrm{V}) = 1.3\mathrm{V} + 0.36\lg V_{IN} \quad (11)$$

where V_{IN} is the differential input signal in millivolts. The slope is 18mV/dB. The indication range is as wide as 60dB within 2dB linearity error. Table 1 summarizes the key measured performances of the proposed LA and RSSI.

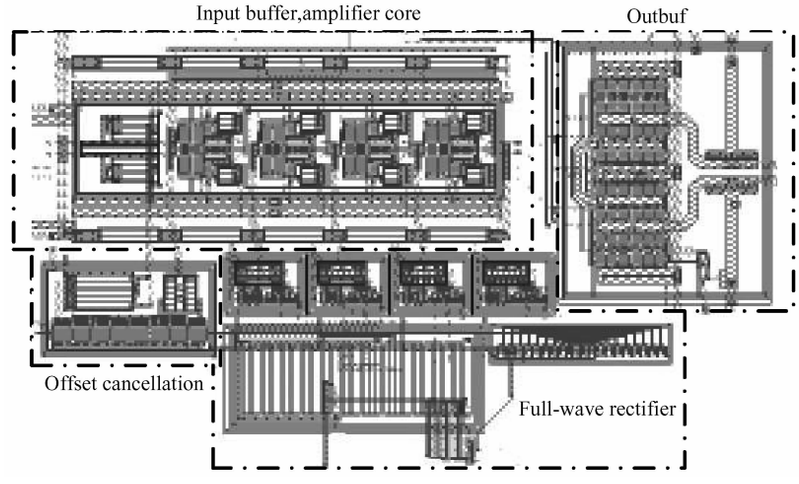

Fig. 10 Die photo

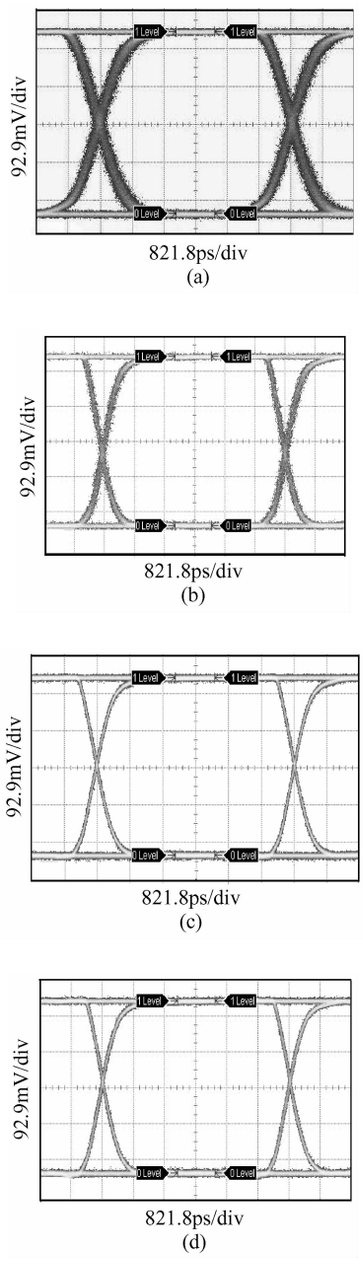

Fig. 11　Measured LA single-end output for input level of 0.5mV (a), 2mV (b), 50mV (c), and 2000mV (d) (Horizontal scale: 821.8ps/div, vertical scale: 92.9mV/div)

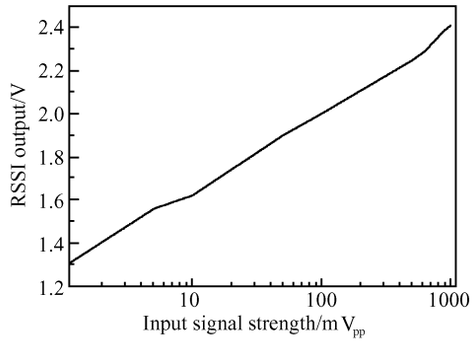

Fig. 12　RSSI output

Table 1　Summary of key measured chip performance

Technology	0.6μm 2P2M CMOS
Supply voltage	5V
Power consumption	60mW
Active chip area	1.05mm^2
RSSI	
Indicating range	60dB (1～1000mV)
Slope	18mV/dB
Logarithmic linearity error	$<\pm$2dB
LA	
Sensitivity	1mV$_{pp}$
Dynamic range	72dB (0.5～2000mV)
Jitter (PP)	380ps (0.5mV input)
Jitter (RMS)	66ps (0.5mV input)
Rise/Fall time (10%～90%)	1.0ns (0.5mV input)

5　Conclusion

This work successfully implements a high-performance LA and RSSI, fabricated by using a low-cost CSMC 0.6μm 2P2M CMOS process. The chip exhibits 200Mbps operation with a 0.5mV high sensitivity and 72dB ultra wide dynamic range. An indication range of 60dB within $\pm$2dB logarithmic accuracy is measured. With an active area of 1.05mm^2, it consumes 60 mW from a 5V power supply. Its excellent performance and cost-effective CMOS process demonstrate that it has commercial applications in the foreseeable future.

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光接收机用 0.5mV 高灵敏度带有接收信号强度指示的 200Mbps CMOS 限幅放大器

王 蓉[1,†] 王志功[1] 徐 建[2] 管志强[2]

(1 东南大学射频与光电集成电路研究所，南京 210096)
(2 江苏新志光电有限公司，南京 210016)

摘要：采用 CSMC 0.6μm 2P2M CMOS 工艺设计并实现了 0.5mV 高灵敏度，72dB 超宽动态范围的 200Mbps CMOS 限幅放大器.该电路详细分析和设计了一种新型的有源直流漂移消除环路获得这一性能.利用信号通路中的限幅放大器，实现了基于分段线性近似的接收信号强度指示电路.信号检测的动态范围高达 60dB，对数精度小于 2dB.整个电路在 5V 单电源下工作，功耗为 60mW.芯片有效面积为 1.05mm^2.

关键词：限幅放大器；接收信号强度指示电路；光接收机；分段线性近似
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† 通信作者.Email:wangrong@seu.edu.cn
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